Mask Set Errata 2

68HC708AS48 8-Bit Microcontroller Unit

INTRODUCTION

This mask set errata provides information pertaining to the ADC, BDLC, EPROM/OTPROM, LVI, MON08, SCI, SIM, SPI, and TIM modules applicable to this 68HC708AS48 MCU mask set device:

- 2G62K

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0G62K. Slight variations to the mask set identification code may result in an altered version number, for example 1G62K.

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The data is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code “9115” indicates the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an SC or XC prefix. An SC prefix denotes special/custom device. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC prefix.

When contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

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ANALOG-TO-DIGITAL CONVERTER (ADC)

Because multiple DC paths exist, the ADC draws 1–10 mA when it is disabled.

BYTE DATA LINK CONTROLLER (BDLC)

Refer to these six items regarding the BDLC.

Item #1 The BDLC does not function properly after a J1850 bus short is detected. The BDLC should:

1. Detect the bus short
2. Stop driving the bus
3. Set the invalid symbol flag
4. Return to the idle state
5. Resume normal operation

Instead, normal operation does not resume until after an end-of-frame (EOF) message is received. Wait for an EOF ($04) interrupt in the BDLC State Vector Register (BSVR), and then clear it with a BSVR read. Also, clear any other interrupt flags that stacked during the bus short before loading the message into the BDLC Data Register (BDR).

Item #2 On a loss-of-arbitration (LOA) in a type II in-frame response (IFR), the BDLC should retransmit the byte in the BDR when it can gain access to the J1850 bus. However, if LOA occurred on the last bit of the byte in the BDR, then an incomplete shift occurs, and the byte transmitted is incorrect.

Item #3 Setting the WCM bit stops the BDLC clocks when the BDLC subsequently is put into wait mode. However, when the CPU executes the WAIT to the BDLC, the BDLC goes to an improper state and cannot correctly receive the message that woke it up. The BDLC will, however, correctly receive the second message after it sees an EOF.

Item #4 When an LOA occurs while using an IFR, the BDLC will be incapable of responding to the IFR. The BDLC must see an EOF to be able to transmit the IFR byte.

Item #5 A CPU read of the BDLC State Vector Register (BSVR) allows the BSVR to display its highest priority stacked flag. Reading also clears the same BSVR flag, making the next priority flag available.

This read can occur only if the BSVR value is read at the exact moment that the BDLC writes a new flag to into the BSVR. This happens because the clearing mechanism for flags in the BSVR becomes active before the source of the flag can be reflected in the BSVR. If this read does occur, the flag which was being set at the time the BSVR was read will not appear and will be cleared. If any other flags are already pending in the BSVR, the existing flag with the highest priority will be read instead. Additionally, although a BSVR read normally starts the clear process for the highest priority flag, it won't in this instance. The highest priority flag, resident prior to the incoming new flag, will be read on the bus but will not clear.

Therefore, do not poll the BSVR for status bits I3 – I0. Instead, use CPU interrupts to process the BDLC flags.

Item #6 If a short-to-ground occurs on the SAE J1850 bus while a message is being transmitted, the BDLC can enter a state in which it is unable to transmit any more messages until it is reset to a known state. For this error to occur, the short-to-ground of the SAE J1850 bus must meet these strict conditions:

- The start of the J1850 bus short must occur after the bit or symbol preceding a message byte has been recognized as valid but before the rising edge of the second bit in the message byte (first active bit) has occurred. For the first byte of a message, this means that the short must occur after the start of frame (SOF) symbol has been recognized as valid and before the second bit of the byte has started. For any following message bytes, the short must start after the last bit of the previous byte has been recognized as a valid bit and before the second bit of the byte has started.
- The J1850 bus short must then short the bus long enough to prevent the second bit in the message byte from being recognized as a valid symbol. This means that if a long high symbol is being transmitted as the second bit of a byte and it is shorted to the length of a short high bit, this error will not occur. This error will manifest itself only if the second bit is shorted to a length less than that defined for a valid active symbol.

If the short-to-ground of the SAE J1850 bus does not meet the above conditions, the BDLC will not enter the state where it is unable to transmit.

If a short happens as described above, these events will occur:

- The invalid symbol flag ($1C), which is the highest priority, will be set in the BSVR.
- The loss of arbitration (LOA) flag ($14) may be set in the BSVR.
- The CRC flag ($18) will be set in the BSVR after an end of data (EOD) symbol has been recognized on the bus.

- Once the short is cleared, the BDLC may transmit an active symbol onto the SAE J1850 bus before halting transmission. Or if this active symbol is transmitted, it will be interpreted as an invalid symbol by any other node on the network.
- The BDLC will then enter a lockup state (unable to transmit) and will remain in this state until either another message is received from the SAE J1850 bus or until a WAIT instruction is executed.

To remedy a short temporarily, use either of these steps. Using both steps is not necessary.

- Receive another message. When another message is received, the rising edge of the SOF symbol will reset the BDLC to its initial state, resolving the problem. The message which resets the BDLC will be received correctly.
- Execute a WAIT instruction. This instruction will place the BDLC into its reset state. Exit from wait mode can be achieved by the reception of a message from the SAE J1850 bus or through a timer or hardware interrupt.

EPROM/OTPROM

EPROM data accesses are incorrect at higher bus frequencies and elevated temperatures. In particular, one or more bits are read as a 1 instead of a 0.

To ensure correct EPROM operation at a maximum bus frequency of 4.2 MHz, OTPROM samples have EPROM test code programmed in locations $3E00 – $3FFF.

LOW-VOLTAGE INHIBIT (LVI)

If the LVISTOP bit is clear (equal to 0), the clear state disables the LVI module in stop mode.

If the LVISTOP bit is set (equal to 1), the set state can enable or disable the LVI module in stop mode (or any other mode) based on the state of the LVIPWRD bit in the CONFIG register.

MONITOR ROM (MON08)

Refer to these two items regarding the MON08.

Item #1 The PA0 data bit is not initialized prior to the security routine in the monitor ROM.

The first eight bytes of data may not be echoed correctly when executing the security routine. A logical low may actually drive the pin to V_{DD} instead of V_{SS} in the wired-OR configuration.

NOTE

The input data is still correctly interpreted. Subsequent data is echoed properly since PA0 is initialized after the security routine.

Item #2 The monitor code does not provide the intended level of user EPROM security. An unauthorized user can breach security by sending a break signal to the MCU during the time in which the security code expects to receive eight authorization bits. This break signal would cause the security routine to fall out of the loop, where the eight authorization bytes are compared. The security code would then jump straight into monitor mode and leave the 48 K EPROM memory space open for accessing.

SERIAL COMMUNICATIONS INTERFACE (SCI)

The SCI does not handle the receiver data overwrite condition correctly. When the SCI data register contains unread received data and the SCI receives more data from another reception, the SCI data register writes over the old data in the receiver data register with the newly received data and sets the receiver overrun bit in the SCI status register 1.

SYSTEM INTEGRATION MODULE (SIM)

The $9E/$8E byte (pre-byte for stack pointer (SP) instructions/stop instruction) should be an illegal opcode; however, the byte does not generate an illegal opcode reset. Instead, it generates a stop mode recovery reset.

The SIM clocks may freeze while the 68HC708AS48 recovers from a brown out condition.

An illegal address reset is generated when data is accessed in an unimplemented address using indexed addressing mode instructions and PUL/PSH.

SERIAL PERIPHERAL INTERFACE (SPI)

The shift data register contents may be corrupted if the SPI data register is written just before the start of a transfer initiated by a master SPI.

Timer input captures are not synchronized with the timer counter stop function or break mode entry, possibly causing extraneous values to be loaded in the TCHxH:TCHxL registers.

The hysteresis buffer input capture circuitry causes slow rise/fall input capture signals on port bits that are channels of the 6-channel timer to generate multiple captures of the TIM.

Additional mask set erratas can be found on the World Wide Web at http://Design-NET.com/csic/TECHSPRT/TechSprt.htm.