Mask Set Errata 1

68HC908AS60 8-Bit Microcontroller Unit

INTRODUCTION

This mask set errata provides information pertaining to the BDLC, SPI, and TIM modules and the flash memory programming time applicable to this 68HC908AS60 MCU mask set device:

- 3H62A

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 3H62A. Slight variations to the mask set identification code may result in an altered version number, for example 4H62A.

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code “9115” indicates the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an SC or XC prefix. An SC prefix denotes special/custom device. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC prefix.

When contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

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BYTE DATA LINK CONTROLLER (BDLC) SHORT-TO-GROUND

If a short-to-ground occurs on the SAE J1850 bus while a message is being transmitted, the BDLC can enter a state in which it is unable to transmit any more messages until it is reset to a known state. For this error to occur, the short-to-ground of the SAE J1850 bus must meet these strict conditions:

- The start of the J1850 bus short must occur after the bit or symbol preceding a message byte has been recognized as valid but before the rising edge of the second bit in the message byte (first active bit) has occurred. For the first byte of a message, this means that the short must occur after the start of frame (SOF) symbol has been recognized as valid and before the second bit of the byte has started. For any following message bytes, the short must start after the last bit of the previous byte has been recognized as a valid bit and before the second bit of the byte has started.
- The J1850 bus short must then short the bus long enough to prevent the second bit in the message byte from being recognized as a valid symbol. This means that if a long high symbol is being transmitted as the second bit of a byte and it is shorted to the length of a short high bit, this error will not occur. This error will manifest itself only if the second bit is shorted to a length less than that defined for a valid active symbol.

If the short-to-ground of the SAE J1850 bus does not meet the above conditions, the BDLC will not enter the state where it is unable to transmit.

If a short happens as described above, these events will occur:

- The invalid symbol flag ($1C), which is the highest priority, will be set in the BSVR.
- The loss of arbitration (LOA) flag ($14) may be set in the BSVR.
- The CRC flag ($18) will be set in the BSVR after an end of data (EOD) symbol has been recognized on the bus.
- Once the short is cleared, the BDLC may transmit an active symbol onto the SAE J1850 bus before halting transmission. Or if this active symbol is transmitted, it will be interpreted as an invalid symbol by any other node on the network.
- The BDLC will then enter a lockup state (unable to transmit) and will remain in this state until either another message is received from the SAE J1850 bus or until a WAIT instruction is executed.

To remedy a short temporarily, use either of these steps. Using both steps is not necessary.

- Receive another message. When another message is received, the rising edge of the SOF symbol will reset the BDLC to its initial state, resolving the problem. The message which resets the BDLC will be received correctly.

- Execute a WAIT instruction. This instruction will place the BDLC into its reset state. Exit from wait mode can be achieved by the reception of a message from the SAE J1850 bus or through a timer or hardware interrupt.

SERIAL PERIPHERAL INTERFACE (SPI)

Clearing the SPE bit to disable the SPI can cause an error when transmitting in slave mode. In this situation, a race condition occurs, allowing an invalid mode fault to occur.

Mode faults occur on the SPI when the slave select ($\overline{SS}$) pin is toggled during a transmission. Mode faults also occur if $\overline{SS}$ is selected and then unselected before SPSCK returns to its idle level after the shift of the eighth data bit when CPHA = 0 while in slave mode.

When the SPI is disabled, the special port function associated with $\overline{SS}$ is also disabled and returns to a logic 1. In slave mode, $\overline{SS}$ must remain a logic 0 during a transmission. Thus, disabling the SPI causes the $\overline{SS}$ signal to go high internally, which sets up a race for the port logic to send in a logic 1 and the SPI to shut down mode fault detection internally.

This condition can be avoided easily in software if mode faults are disabled by clearing the MODFEN bit of the SPSCR register before disabling the SPI in slave mode.

TIMER INTERFACE MODULE (TIM)

When the toggle on overflow (TOV) bit is set, writing to a TCHxH register at the point of an overflow inhibits the associated pin from toggling until the TCHxL register is written. The pin then toggles at the next overflow. Even though a toggle can be completely missed, the TOF flag will be set and an interrupt can be generated. The only way to inhibit a toggle on overflow and set the TOF bit is to write to the TMODH register until the TMODL register is written. Similarly, in buffered PWM mode, writing to the inactive registers (TCH0H:l, TCH2H:L, TCH4H:L) at this overflow point produces the same problem. Writing to the odd channels (TCH1H:L, TCH3H:L, TCH5H:L) produces no faults.

Avoid this problem by using the overflow routine instead of writing to inactive channel registers within the output compare routine. Each output compare event occurs as a result of the last channel register written to prior to the last overflow.

Make sure that both odd and even timer channel registers are initialized. Write to the odd channels last, because the active channel register on startup is the even channel. If the inactive channel register is not written to last, then the next PWM pulse width will be exactly the same as the first, reflecting the value written to the even channel register.

FLASH MEMORY PROGRAMMING TIME

The minimum flash bus clock period (t_{CYC}) is 119 ns (8.4MHz).

The minimum flash erase time (t_{ERASE}) is 100 ms. The maximum is 110 ms.

Verify mode is now known as margin read mode.

When using the iterative program/margin read technique, a maximum of five programming pulses is allowed. The nominal duration of the programming pulse (t_{STEP}) is 1 ms. The t_{STEP} duration is defined as the amount of time during one program cycle that HVEN is held high. The minimum t_{STEP} is 0.8 ms and the maximum t_{STEP} is 1.2 ms. Therefore, the maximum cumulative program time (t_{PROG}) per page is 6 ms.

The minimum program time (t_{PROG}) is 0.8 ms. The maximum program time is 6 ms.

Cumulative program time exceeding 6 ms may cause unintentional programming of erased bits. This condition is known as program disturb.

The maximum program time per row between erase cycles is 48 ms. Program time greater than 48 ms per row may cause program disturb.

The minimum flash endurance is 100 erase/program cycles.

The minimum flash block endurance is 100 cycles.

FLASH MEMORY MAXIMUM FREQUENCY

Characterization of the flash memory across the full temperature/voltage/frequency specification has detected a fault which prevents reads of the flash memory at high temperatures. The maximum frequency versus temperature is defined as:

Temperature	Maximum Frequency
– 40 °C	8.4 MHz
25 °C	8.4 MHz
85 °C	6.0 MHz
125 °C	5.0 MHz

Additional mask set erratas can be found on the World Wide Web at http://Design-NET.com/csic/TECHSPRT/TechSprt.htm.