Mask Set Errata 1

68HC08AS20 8-Bit Microcontroller Unit

INTRODUCTION

This mask set errata provides information pertaining to the ADC, BDLC, CGM, EEPROM, LVI, and SIM modules and the electrical specifications applicable to this 68HC08AS20 MCU mask set device:

- 0G39Y

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0G39Y. Slight variations to the mask set identification code may result in an altered version number, for example 1G39Y.

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The data is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code “9115” indicates the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an SC or XC prefix. An SC prefix denotes special/custom device. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC prefix.

When contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

Specifications and information herein are subject to change without notice.

© Motorola, Inc., 1997
MSE Published Date: 7/10/97

ANALOG-TO-DIGITAL CONVERTER (ADC)

All analog input voltages convert to $00.

BYTE DATA LINK CONTROLLER (BDLC)

Refer to these two items regarding the BDLC.

Item #1 A CPU read of the BDLC State Vector Register (BSVR) allows the BSVR to display its highest priority stacked flag. Reading also clears the same BSVR flag, making the next priority flag available.

This read can occur only if the BSVR value is read at the exact moment that the BDLC writes a new flag to into the BSVR. This happens because the clearing mechanism for flags in the BSVR becomes active before the source of the flag can be reflected in the BSVR. If this read does occur, the flag which was being set at the time the BSVR was read will not appear and will be cleared. If any other flags are already pending in the BSVR, the existing flag with the highest priority will be read instead. Additionally, although a BSVR read normally starts the clear process for the highest priority flag, it won't in this instance. The highest priority flag, resident prior to the incoming new flag, will be read on the bus but will not clear.

Therefore, do not poll the BSVR for status bits I3 – I0. Instead, use CPU interrupts to process the BDLC flags.

Item #2 If a short-to-ground occurs on the SAE J1850 bus while a message is being transmitted, the BDLC can enter a state in which it is unable to transmit any more messages until it is reset to a known state. For this error to occur, the short-to-ground of the SAE J1850 bus must meet these strict conditions:

- The start of the J1850 bus short must occur after the bit or symbol preceding a message byte has been recognized as valid but before the rising edge of the second bit in the message byte (first active bit) has occurred. For the first byte of a message, this means that the short must occur after the start of frame (SOF) symbol has been recognized as valid and before the second bit of the byte has started. For any following message bytes, the short must start after the last bit of the previous byte has been recognized as a valid bit and before the second bit of the byte has started.
- The J1850 bus short must then short the bus long enough to prevent the second bit in the message byte from being recognized as a valid symbol. This means that if a long high symbol is being transmitted as the second bit of a byte and it is shorted to the length of a short high bit, this error will not occur. This error will manifest itself only if the second bit is shorted to a length less than that defined for a valid active symbol.

If the short-to-ground of the SAE J1850 bus does not meet the above conditions, the BDLC will not enter the state where it is unable to transmit.

If a short happens as described above, these events will occur:

- The invalid symbol flag ($1C), which is the highest priority, will be set in the BSVR.
- The loss of arbitration (LOA) flag ($14) may be set in the BSVR.
- The CRC flag ($18) will be set in the BSVR after an end of data (EOD) symbol has been recognized on the bus.
- Once the short is cleared, the BDLC may transmit an active symbol onto the SAE J1850 bus before halting transmission. Or if this active symbol is transmitted, it will be interpreted as an invalid symbol by any other node on the network.
- The BDLC will then enter a lockup state (unable to transmit) and will remain in this state until either another message is received from the SAE J1850 bus or until a WAIT instruction is executed.

To remedy a short temporarily, use either of these steps. Using both steps is not necessary.

- Receive another message. When another message is received, the rising edge of the SOF symbol will reset the BDLC to its initial state, resolving the problem. The message which resets the BDLC will be received correctly.
- Execute a WAIT instruction. This instruction will place the BDLC into its reset state. Exit from wait mode can be achieved by the reception of a message from the SAE J1850 bus or through a timer or hardware interrupt.

CLOCK GENERATOR MODULE (CGM)

There is no clock output from the phase-locked loop (PLL). Therefore, do not use the PLL in this revision of the 68HC08AS20.

EEPROM

The EEPROM cannot be accessed in the MMDS08 unless the EEPROM is enabled first. To enable the EEPROM in the MMDS08, the data $08 must be written to location $FE03.

NOTE

This is not a problem in user mode, just when using the 68HC08AS20 in the MMDS08.

ELECTRICAL SPECIFICATIONS

The digital and analog supply I_{DD}'s are both approximately 10 mA higher than expected for all modes of operation (run, wait, and stop).

LOW-VOLTAGE INHIBIT (LVI)

The LVI trip points are approximately 1 V below the design target of 4 V. In addition, the LVI trip point hysteresis is much lower than the minimum specified 100 mV.

SYSTEM INTEGRATION MODULE (SIM)

The SIM clocks may freeze while the 68HC08AS20 recovers from a brown out condition.

An illegal address reset is generated when data is accessed in an unimplemented address using indexed addressing mode instructions and PUL/PSH.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

Additional mask set erratas can be found on the World Wide Web at http://Design-NET.com/csic/TECHSPRT/TechSprt.htm.