XC68HC711K4 DEVICE INFORMATION
(Rev. 0 -3/28/94)
1D67F Mask Set

The following contains information and errata that pertains to the 1D67F mask set devices.

ERRATA:

1) tDSR is much greater than the 20ns target spec due to the re-layout of Port C for PROG Mode. Test spec is 60ns.

2) The PWM on this mask set was meant to be an improvement, however, while some problems were fixed others were introduced. Below are the problem cases we found:

a) When going from a duty=0 to any other value, the first PWM cycle after the new duty has taken affect has the incorrect polarity for 1 E clock cycle. After this first E clock cycle, everything works correctly.

b) Disabling a channel when the counter is one cycle away from meeting the duty value causes the output to be incorrect when the channel is re-enabled. The output after re-enabling does not complete the duty before changing polarity. It behaves as though actual duty=duty-1.

c) When a channel is first enabled, the actual duty = duty+1. The output is 1 E clock cycle longer than it should be before changing polarity.

The above problems where all caused by the method selected to fix the original PWM problem on the K4's. This method delayed the PWM output by 1 E clock cycle, but the enable/disable signals were not delayed thus causing the new problems. A solution to both the original and new PWM problems has been found and will be incorporated on all future mask sets.

3) The PWM is disabled during WAIT.

4) Chip selects remain active during STOP and WAIT if enabled.

5) Normally E clock is low during STOP or WAIT, but in clock stretch mode E clock will be high. This is not a problem, but is included as information only. All future mask sets will behave in the same way.

6) PROG Mode is not completely functional. A change has been identified and will be corrected on all future mask sets.

7) CONFIG register will only program at room temperature.

8) EPROM is marginally functional at low temperatures.

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