68HC711P2 DEVICE INFORMATION
D99H Mask Set

Timer double clock:

When BCS=1 and MCS=0 in the PLLCR register, the bus clock is derived from the PLL (Phase Locked Loop) and the Module clock is derived from the crystal. In this state, the timer clock gets an extra pulse and causes the timer to run at two times expected rate.

MI-Bus transmit inverse polarity:

When PT2(3)=1 in the S2(3)CR1 register, the inverse transmit data is compared to non-inverse receive data and causes a bit error.

SCI receive sync multiple interrupts:

When BCS=1 and MCS=0 in the PLLCR register, the receive byte flag may not clear after first read.

SCI baud rate counter reset:

Baud counter may be accidentally cleared if bit five in the S2BDL register is set from a previous access to SDB (Sub Data Bus for serial section).

EPROM:

PROG mode is not functional

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