MC68HC811A2 DEVICE INFORMATION
A75H mask set

ERRATA:

An EEPROM array supply impedance problem does not allow program execution out of on-board EEPROM at above 1 MHz bus frequency. Normal data accesses to the EEPROM work correctly over the entire temperature, frequency, and voltage ranges. Multiple consecutive accesses in program code execution from EEPROM may not work under all conditions.

Use of slow edges on signals feeding the the timer input capture or pulse accumulator inputs is not recommended. Use of buffers with edges faster than 100 nsec will prevent system noise generating false captures. In conjunction with faster edges, we have re-specified the timer input pulse width to be slightly longer than a system clock period to properly capture transitions. See section 11 of the MC68HC11A8 data sheet for details.

A spurious write signal can occur if the Reset pin is pulled low while LIR is low. Since MODA and LIR share the same pin, the above condition causes the internal MDA signal to indicate single chip mode for a short time. This in turn causes the STRB/Read/Write pin to switch from the R/W function (logic 1 - read) to the STRB function (logic 0) which appears to be a write signal to an expanded system. Suggested gating to prevent inadvertent writes to RAM is detailed below. An alternate solution, which will increase system power consumption, is to connect a 1K ohm pullup resistor to the LIR pin.

A TAP (Transfer Accumulator A to the Condition Code Register) instruction may affect the next instruction if certain conditions exist. When the overflow (V) and carry (C) bits in the condition code register are both zero, and TAP is executed to force either bit or both bits to a one, then the high order address of the second cycle of the next instruction may be $FF. The user can avoid these conditions by setting the V and C bits using the SEV and SEC commands if the bits are clear. This problem will not occur if the bits are already set.

The Computer Operating Properly (COP) circuit will time out early under certain conditions. At the divide by 1 rate, if the $55/AA write sequence is performed during the first half of the cycle, the COP clearing sequence will be ignored. At the divide by 4 rate, the clearing sequence is ignored during the first 1/8 of the COP cycle. Similarly, the clear does not occur if the sequence is written during the first 1/32 of the cycle at the divide by 16 rate; and during the first 1/128 of the cycle at the divide by 64 rate. Since it is difficult to determine which part of the cycle the user is in at the time, the user can perform the watchdog timer clearing sequence at twice the specified rate to effectively avoid the COP time out. For example, with a 2.0 MHz system clock and the divide by 4 rate selected, a write during the first 8.2 ms of the COP cycle will be ignored. A write at approximately every 56 ms (65.5 ms less one eighth of the COP period) should be appropriate to prevent a reset.

A Computer Operating Properly (COP) generated reset holds the reset line low for three cycles instead of the specified four cycles. This would only affect users who have external devices that require four clock cycles of reset to reinitialize.

The timer output compare flags can remain set even after a clear attempt is made at slow timer clock rates. The signal that sets the timer compare flag remains active for a whole timer clock cycle rather than one E clock cycle. If an attempt is made to clear a compare flag before the end of the timer clock, it is unsuccessful and the flag remains set. Normally, this is not the case, but at the slowest timer clock rate (E/16), the time between the flag setting and actual clearing of the flag is 16 E cycles, and a clear attempt can be made in this time. We recommend that the clearing routine for OC flags be placed later in the interrupt service routine to guarantee at least 16 E clock cycles if the E/16 timer clock rate is selected.

An inadvertent Serial Peripheral Interface (SPI) write collision can occur in a dual 68HC11 (Master/Slave) system if the slave's SS (Slave Select) line is held low during reset. The error occurs because SCK floats high after reset in the slave. This high on SCK and the low on the slave SS line tells the slave that a transmission has started when it really has not. An external hardware solution would be to hold the slave SCK line low during reset.

When the SPI is operating as a slave with CPHA = 1, and the SCK input is asynchronous to the E clock, SPI transfers can fail such that SPIF is not set. Occasionally, the next transfer after such a failure will result in an improperly received data character.

User updates of the SCI Baud Rate Control Register (BAUD) with the same data during serial data transfers may cause errors on the byte being transmitted/received.

Multiple IRQ pin interrupts are caused when the IRQ pin is configured as an edge sensitive input, IRQ is held low, and EEPROM programming or erasure is in progress. Regular level sensitive IRQ operation is not affected by this problem.

The EEPROM takes priority over Boot ROM in the special modes when the EEPROM is mapped to $B800.

The CPU will not exit STOP mode correctly when interrupted by IRQ or XIRQ if the instruction immediately preceding STOP is a column 4 or 5 accumulator inherent (opcodes $4X and $5X) instruction, such as NEGA, NEGB, COMA, COMB, etc. These single byte, two cycle instructions must be followed by a NOP, then the STOP command. If reset is used to exit STOP mode, the CPU will respond correctly.

USER INFORMATION:

A new data sheet for the MC68HC11 series is now available. The 1987 data sheet can be ordered from your local Motorola sales office. The document was completely re-written to correct various errors, add information, and provide better functional descriptions. This errata sheet is to be used as a supplement to the data sheet and any 68HC811A2 information that the user may already have.

Multiple reset sequences can occur on slow rising reset edges. Buffering of the external POR signal to achieve a fast rise time is recommended if multiple reset sequences are viewed as a problem. Multiple reset sequences do not affect device operation.

An inadvertent write or erase of EEPROM can be caused by a program runaway. Specifically, if the system has a slow power-down and the reset signal tracks the VDD line, the CPU will eventually stop executing code properly, and the program can jump to a section of code that may write or erase EEPROM. The only way to absolutely protect EEPROM data during power-up and power-down is to have the device securely in reset. Two examples of low voltage inhibit (LVI) circuits that can be used for system reset are presented in the new data sheet. See section 9 in the new data sheet for more information.

The on-chip RC oscillator should be enabled (by setting the CSEL bit in the OPTION register) to program or erase the EEPROM when the operating frequency is below 2MHz. Alternatively, the user may elect to increase the programming time to 15ms when the operating frequency is between 1MHz and 2MHz. See section 3.5 and table 11.10 in the new data sheet for more information.

A new feature, VSTBY, is shared with the MODB pin to retain RAM contents during powerdown. This feature requires special voltage level precautions on the A75H mask to prevent latch-up, so it should not be used. Subsequent mask sets will allow 4V RAM retention in the power-down condition.

The 68HC811A2 comes from Motorola with the CONFIG register programmed to $FF to enable on board EEPROM, place the EEPROM at $F800, and disable the COP feature.

MC68HC811A2 Errata & Information

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