About This Book

The primary objective of this user's manual is to define the functionality of the MCF5272 processors for use by software and hardware developers.

The information in this book is subject to change without notice, as described in the disclaimers on the title page of this book. As with any technical documentation, it is the readers' responsibility to be sure he is using the most recent version of the documentation.

To locate any published errata or updates for this document, refer to the world-wide web at http://www.motorola.com/coldfire.

Audience

This manual is intended for system software and hardware developers and applications programmers who want to develop products with the MCF5272. It is assumed that the reader understands operating systems, microprocessor system design, basic principles of software and hardware, and basic details of the ColdFire® architecture.

Organization

Following is a summary and brief description of the major sections of this manual:

- Chapter 1, "Overview," includes general descriptions of the modules and features incorporated in the MCF5272, focussing in particular on new features.
- Chapter 2, "ColdFire Core," provides an overview of the microprocessor core of the MCF5272. The chapter describes the organization of the Version 2 (V2) ColdFire 5200 processor core and an overview of the program-visible registers (the programming model) as they are implemented on the MCF5272. It also includes a full description of exception handling and a table of instruction timings.
- Chapter 3, "Hardware Multiply/Accumulate (MAC) Unit," describes the MCF5272 multiply/accumulate unit, which executes integer multiply, multiply-accumulate, and miscellaneous register instructions. The MAC is integrated into the operand execution pipeline (OEP).
- Chapter 4, "Local Memory." This chapter describes the MCF5272 implementation of the ColdFire V2 local memory specification. It consists of three major sections, as follows.

  - — Section 4.3, “SRAM Overview,” describes the MCF5272 on-chip static RAM (SRAM) implementation. It covers general operations, configuration, and initialization. It also provides information and examples of how to minimize power consumption when using the SRAM.
  - — Section 4.4, “ROM Overview,” describes the MCF5272 on-chip static ROM. The ROM module contains tabular data that the ColdFire core can access in a single cycle.
  - — Section 4.5, “Instruction Cache Overview,” describes the MCF5272 cache implementation, including organization, configuration, and coherency. It describes cache operations and how the cache interacts with other memory structures.
- Chapter 5, “Debug Support,” describes the Revision A hardware debug support in the MCF5272.
- Chapter 6, “System Integration Module (SIM),” describes the SIM programming model, bus arbitration, power management, and system-protection functions for the MCF5272.
- Chapter 7, “Interrupt Controller,” describes operation of the interrupt controller portion of the SIM. Includes descriptions of the registers in the interrupt controller memory map and the interrupt priority scheme.
- Chapter 8, “Chip Select Module,” describes the MCF5272 chip-select implementation, including the operation and programming model, which includes the chip-select address, mask, and control registers.
- Chapter 9, “SDRAM Controller,” describes configuration and operation of the synchronous DRAM controller component of the SIM, including a general description of signals involved in SDRAM operations. It provides interface information for memory configurations using most common SDRAM devices for both 16- and 32-bit-wide data buses. The chapter concludes with signal timing diagrams.
- Chapter 10, “DMA Controller,” provides an overview of the MCF5272’s one-channel DMA controller intended for memory-to-memory block data transfers. This chapter describes in detail its signals, registers, and operating modes.
- Chapter 11, “Ethernet Module,” describes the MCF5272 fast Ethernet media access controller (MAC). This chapter begins with a feature-set overview, a functional block diagram, and transceiver connection information for both MII and seven-wire serial interfaces. The chapter concludes with detailed descriptions of operation and the programming model.
- Chapter 12, “Universal Serial Bus (USB),” provides an overview of the USB module of the MCF5272, including detailed operation information and the USB programming model. Connection examples and circuit board layout considerations are also provided.

The *USB Specification, Revision 1.1* is a recommended supplement to this chapter. It can be downloaded from http://www.usb.org. Chapter 2 of this specification, *Terms and Abbreviations*, provides definitions of many of the words found here.

- Chapter 13, “Physical Layer Interface Controller (PLIC),” provides detailed information about the MCF5272’s physical layer interface controller, a module intended to support ISDN applications. The chapter begins with a description of operation and a series of related block diagrams starting with a high-level overview. Each successive diagram depicts progressively more internal detail. The chapter then describes timing generation and the programming model and concludes with three application examples.
- Chapter 14, “Queued Serial Peripheral Interface (QSPI) Module,” provides a feature-set overview and description of operation, including details of the QSPI’s internal RAM organization. The chapter concludes with the programming model and a timing diagram.
- Chapter 15, “Timer Module,” describes configuration and operation of the four general-purpose timer modules, timer 0, 1, 2 and 3.
- Chapter 16, “UART Modules,” describes the use of the universal asynchronous/synchronous receiver/transmitters (UARTs) implemented on the MCF5272, including example register values for typical configurations.
- Chapter 17, “General Purpose I/O Module,” describes the operation and programming model of the three general purpose I/O (GPIO) ports on the MCF5272. The chapter details pin assignment, direction-control, and data registers.
- Chapter 18, “Pulse Width Modulation (PWM) Module,” describes the configuration and operation of the pulse width modulation (PWM) module. It includes a block diagram, programming model, and timing diagram.
- Chapter 19, “Signal Descriptions,” provides a listing and brief description of all the MCF5272 signals. Specifically, it shows which are inputs or outputs, how they are multiplexed, and the state of each signal at reset. The first listing is organized by function, with signals appearing alphabetically within each functional group. This is followed by a second listing sorted by pin number.
- Chapter 20, “Bus Operation,” describes the functioning of the bus for data-transfer operations, error conditions, bus arbitration, and reset operations. It includes detailed timing diagrams showing signal interaction. Operation of the bus is defined for transfers initiated by the MCF5272 as a bus master. The MCF5272 does not support external bus masters. Note that Chapter 9, “SDRAM Controller,” describes DRAM cycles.

- Chapter 21, “IEEE 1149.1 Test Access Port (JTAG),” describes configuration and operation of the MCF5272 Joint Test Action Group (JTAG) implementation. It describes those items required by the IEEE 1149.1 standard and provides additional information specific to the MCF5272. For internal details and sample applications, see the IEEE 1149.1 document.
- Chapter 22, “Mechanical Data,” provides a functional pin listing and package diagram for the MCF5272.
- Chapter 23, “Electrical Characteristics,” describes AC and DC electrical specifications and thermal characteristics for the MCF5272. Because additional speeds may have become available since the publication of this book, consult Motorola’s ColdFire web page, http://www.motorola.com/coldfire, to confirm that this is the latest information.

This manual includes the following two appendixes:

- Appendix A, “List of Memory Maps,” provides the entire address-map for MCF5272 memory-mapped registers.
- Appendix B, “Buffering and Impedance Matching,” provides some suggestions regarding interface circuitry between the MCF5272 and SDRAMs.

This manual also includes an index.

Suggested Reading

This section lists additional reading that provides background for the information in this manual as well as general information about the ColdFire architecture.

General Information

The following documentation provides useful information about the ColdFire architecture and computer architecture in general:

ColdFire Documentation

The ColdFire documentation is available from the sources listed on the back cover of this manual. Document order numbers are included in parentheses for ease in ordering.

- *ColdFire Programmers Reference Manual, R1.0* (MCF5200PRM/AD)
- User’s manuals—These books provide details about individual ColdFire implementations and are intended to be used in conjunction with *The ColdFire Programmers Reference Manual.* These include the following:
  - *ColdFire MCF5102 User’s Manual* (MCF5102UM/AD)
  - *ColdFire MCF5202 User’s Manual* (MCF5202UM/AD)
  - *ColdFire MCF5204 User’s Manual* (MCF5204UM/AD)
  - *ColdFire MCF5206 User’s Manual* (MCF5206EUM/AD)

  - — *ColdFire MCF5206E User's Manual* (MCF5206EUM/AD)
  - — *ColdFire MCF5307 User's Manual* (MCF5307UM/AD)
  - — *ColdFire MCF5407 User's Manual* (MCF5407UM/AD)
- *ColdFire Programmers Reference Manual, R1.0* (MCF5200PRM/AD)
- *Using Microprocessors and Microcomputers: The Motorola Family,* William C. Wray, Ross Bannatyne, Joseph D. Greenfield

Additional literature on ColdFire implementations is being released as new processors become available. For a current list of ColdFire documentation, refer to the World Wide Web at http://www.motorola.com/ColdFire/.

Conventions

This document uses the following notational conventions:

MNEMONICS	In text, instruction mnemonics are shown in uppercase.
`mnemonics`	In code and tables, instruction mnemonics are shown in lowercase.
italics	Italics indicate variable command parameters. Book titles in text are set in italics.
0x0	Prefix to denote hexadecimal number
0b0	Prefix to denote binary number
REG[FIELD]	Abbreviations for registers are shown in uppercase. Specific bits, fields, or ranges appear in brackets. For example, RAMBAR[BA] identifies the base address field in the RAM base address register.
nibble	A 4-bit data unit
byte	An 8-bit data unit
word	A 16-bit data unit[1]
longword	A 32-bit data unit
x	In some contexts, such as signal encodings, x indicates a don't care.
n	Used to express an undefined numerical value
¬	NOT logical operator
&	AND logical operator
|	OR logical operator

[1]The only exceptions to this appear in the discussion of serial communication modules that support variable-length data transmission units. To simplify the discussion these units are referred to as words regardless of length.

Acronyms and Abbreviations

Table i lists acronyms and abbreviations used in this document.

Table i. Acronyms and Abbreviated Terms

Term	Meaning
ADC	Analog-to-digital conversion
ALU	Arithmetic logic unit
AVEC	Autovector
BDM	Background debug mode
BIST	Built-in self test
BSDL	Boundary-scan description language
CODEC	Code/decode
DAC	Digital-to-analog conversion
DMA	Direct memory access
DSP	Digital signal processing
EA	Effective address
EDO	Extended data output (DRAM)
FIFO	First-in, first-out
GPIO	General-purpose I/O
I^2C	Inter-integrated circuit
IEEE	Institute for Electrical and Electronics Engineers
IFP	Instruction fetch pipeline
IPL	Interrupt priority level
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LIFO	Last-in, first-out
LRU	Least recently used
LSB	Least-significant byte
lsb	Least-significant bit
MAC	Multiply accumulate unit, also Media access controller
MBAR	Memory base address register
MSB	Most-significant byte
msb	Most-significant bit
Mux	Multiplex

Table i. Acronyms and Abbreviated Terms (Continued)

Term	Meaning
NOP	No operation
OEP	Operand execution pipeline
PC	Program counter
PCLK	Processor clock
PLIC	Physical layer interface controller
PLL	Phase-locked loop
PLRU	Pseudo least recently used
POR	Power-on reset
PQFP	Plastic quad flat pack
PWM	Pulse width modulation
QSPI	Queued serial peripheral interface
RISC	Reduced instruction set computing
Rx	Receive
SIM	System integration module
SOF	Start of frame
TAP	Test access port
TTL	Transistor transistor logic
Tx	Transmit
UART	Universal asynchronous/synchronous receiver transmitter
USB	Universal serial bus

Terminology Conventions

Table ii shows terminology conventions used throughout this document.

Table ii Notational Conventions

Instruction	Operand Syntax
Opcode Wildcard	
cc	Logical condition (example: NE for not equal)
Register Specifications	
An	Any address register n (example: A3 is address register 3)
Ay,Ax	Source and destination address registers, respectively
Dn	Any data register n (example: D5 is data register 5)
Dy,Dx	Source and destination data registers, respectively
Rc	Any control register (example VBR is the vector base register)
Rm	MAC registers (ACC, MAC, MASK)
Rn	Any address or data register
Rw	Destination register w (used for MAC instructions only)
Ry,Rx	Any source and destination registers, respectively
Xi	index register i (can be an address or data register: Ai, Di)
Register Names	
ACC	MAC accumulator register
CCR	Condition code register (lower byte of SR)
MACSR	MAC status register
MASK	MAC mask register
PC	Program counter
SR	Status register
Port Name	
DDATA	Debug data port
PST	Processor status port
Miscellaneous Operands	
#<data>	Immediate data following the 16-bit operation word of the instruction
<ea>	Effective address
<ea>y,<ea>x	Source and destination effective addresses, respectively
<label>	Assembly language program label
<list>	List of registers for MOVEM instruction (example: D3–D0)
<shift>	Shift operation: shift left (<<), shift right (>>)
<size>	Operand data size: byte (B), word (W), longword (L)
bc	Both instruction and data caches

Table ii Notational Conventions (Continued)

Instruction	Operand Syntax
dc	Data cache
ic	Instruction cache
# <vector>	Identifies the 4-bit vector number for trap instructions
<>	identifies an indirect data address referencing memory
<xxx>	identifies an absolute address referencing memory
d*n*	Signal displacement value, *n* bits wide (example: d16 is a 16-bit displacement)
SF	Scale factor (x1, x2, x4 for indexed addressing mode, <<1n>> for MAC operations)
Operations	
+	Arithmetic addition or postincrement indicator
–	Arithmetic subtraction or predecrement indicator
x	Arithmetic multiplication
/	Arithmetic division
~	Invert; operand is logically complemented
&	Logical AND
|	Logical OR
^	Logical exclusive OR
<<	Shift left (example: D0 << 3 is shift D0 left 3 bits)
>>	Shift right (example: D0 >> 3 is shift D0 right 3 bits)
→	Source operand is moved to destination operand
←→	Two operands are exchanged
sign-extended	All bits of the upper portion are made equal to the high-order bit of the lower portion
If <condition> then <operations> else <operations>	Test the condition. If true, the operations after ‘then’ are performed. If the condition is false and the optional ‘else’ clause is present, the operations after ‘else’ are performed. If the condition is false and else is omitted, the instruction performs no operation. Refer to the Bcc instruction description as an example.

Table ii Notational Conventions (Continued)

Instruction	Operand Syntax
Subfields and Qualifiers	
{}	Optional operation
()	Identifies an indirect address
d_n	Displacement value, n-bits wide (example: d_{16} is a 16-bit displacement)
Address	Calculated effective address (pointer)
Bit	Bit selection (example: Bit 3 of D0)
lsb	Least significant bit (example: lsb of D0)
LSB	Least significant byte
LSW	Least significant word
msb	Most significant bit
MSB	Most significant byte
MSW	Most significant word
Condition Code Register Bit Names	
C	Carry
N	Negative
V	Overflow
X	Extend
Z	Zero