MOTOROLA
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68K ColdFire® MICROPROCESSORS

Errata to **MCF5272 ColdFire® Microprocessor User's Manual, rev. 0**

This addendum describes corrections to the *MCF5272 ColdFire Microprocessor User's Manual*, Motorola document order number MCF5272UM/D. In the General MCF5272 Changes section, information is given which needs to be changed throughout the book. In the Section and Page section, for convenience, the section number and page number of the addendum item in the user's manual are provided. The MCF5272 device referred to in this document is the MCF5272VF66. Please check the World Wide Web at http://www.motorola.com/ColdFire for the latest updates.

1. General MCF5272UM Changes

1.1 Incorrect Register Identifiers

Register identifiers were not completely updated throughout the user's manual from names used in early versions of the manual released under NDA. The principal chapters affected are UART, Ethernet, and PLIC. Motorola is publishing the old and new register names for the entire memory map since a significant amount of collateral documentation such as source code was developed using the old register names. For clarification of the register nomenclature, please refer to Table 1 through Table 14, which list the correct register names and mnemonics as they should all appear in the data book, along with the old ones. Identifiers that have changed are displayed in boldface type. Those that have not changed are marked "no change" in the New Mnemonic column.

Table 1. On-Chip Peripherals and Configuration Registers Memory Map

MBAR Offset	Register Name	Old Mnemonic	New Mnemonic
0x0000	Module Base Address Register, Read Only	MBAR	No change
0x0004	System Configuration Register	SCR	No change
0x0006	System Protection Register	SPR	No change

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Table 1. On-Chip Peripherals and Configuration Registers Memory Map (Continued)

MBAR Offset	Register Name	Old Mnemonic	New Mnemonic
0x0008	Power Management Register	PMR	No change
0x000E	Activate Low Power Register	ALPR	No change
0x0010	Device Identification Register	DIR	No change

Table 2. Interrupt Control Register Memory Map

MBAR Offset	Register Name	Old Mnemonic	New Mnemonic
0x0020	Interrupt Control Register 1	ICR1	No change
0x0024	Interrupt Control Register 2	ICR2	No change
0x0028	Interrupt Control Register 3	ICR3	No change
0x002C	Interrupt Control Register 4	ICR4	No change
0x0030	Interrupt Source Register	ISR	No change
0x0034	Programmable Interrupt Transition Register	PITR	No change
0x0038	Programmable Interrupt Wakeup Register	PIWR	No change
0x003F	Programmable Interrupt Vector Register	PIVR	No change

Table 3. Chip Select Register Memory Map

MBAR Offset	Register Name	Old Mnemonic	New Mnemonic
0x0040	CS Base Register 0	CSBR0	No change
0x0044	CS Option Register 0	CSOR0	No change
0x0048	CS Base Register 1	CSBR1	No change
0x004C	CS Option Register 1	CSOR1	No change
0x0050	CS Base Register 2	CSBR2	No change
0x0054	CS Option Register 2	CSOR2	No change
0x0058	CS Base Register 3	CSBR3	No change
0x005C	CS Option Register 3	CSOR3	No change
0x0060	CS Base Register 4	CSBR4	No change
0x0064	CS Option Register 4	CSOR4	No change
0x0068	CS Base Register 5	CSBR5	No change
0x006C	CS Option Register 5	CSOR5	No change
0x0070	CS Base Register 6	CSBR6	No change
0x0074	CS Option Register 6	CSOR6	No change
0x0078	CS Base Register 7	CSBR7	No change
0x007C	CS Option Register 7	CSOR7	No change

Table 4. GPIO Port Register Memory Map

MBAR Offset	Register Name	Old Mnemonic	New Mnemonic
0x0080	Port A Control Register	PACNT	No change
0x0084	Port A Data Direction Register	PADDR	No change
0x0086	Port A Data Register	PADAT	No change
0x0088	Port B Control Register	PBCNT	No change
0x008C	Port B Data Direction Register	PBDDR	No change
0x008E	Port B Data Register	PBDAT	No change
0x0094	Port C Data Direction Register	PCDDR	No change
0x0096	Port C Data Register	PCDAT	No change
0x0098	Port D Control Register	PDCNT	No change

Table 5. QSPI Module Memory Map

MBAR Offset	Register Name	Old Mnemonic	New Mnemonic
0x00A0	QSPI Mode Register	SPMODE	**QMR**
0x00A4	QSPI Delay Register	SPDELAY	**QDLYR**
0x00A8	QSPI Wrap Register	SPWRAP	**QWR**
0x00AC	QSPI Interrupt Register	SPINT	**QIR**
0x00B0	QSPI Address Register	SPADDR	**QAR**
0x00B4	QSPI Data Register	SPDATA	**QDR**

Table 6. PWM Module Memory Map

MBAR Offset	Register Name	Old Mnemonic	New Mnemonic
0x00C0	**PWM Control Register 0**	PWMCR1	**PWCR0**
0x00C4	**PWM Control Register 1**	PWMCR2	**PWCR1**
0x00C8	**PWM Control Register 2**	PWMCR3	**PWCR2**
0x00D0	**PWM Pulse Width Register 0**	PWMWD1	**PWWD0**
0x00D4	**PWM Pulse Width Register 1**	PWMWD2	**PWWD1**
0x00D8	**PWM Pulse Width Register 2**	PWMWD3	**PWWD2**

Table 7. DMA Module Memory Map

MBAR Offset	Register Name	Old Mnemonic	New Mnemonic
0x00E0	DMA Mode Register	DCMR	No change
0x00E6	DMA Interrupt Register	DCIR	No change
0x00E8	DMA Byte Count Register	DBCR	No change
0x00EC	DMA Source Address Register	DSAR	No change
0x00F0	DMA Destination Address Register	DDAR	No change

Table 8. UART0 Module Memory Map

MBAR Offset	Register Name	Old Mnemonic	New Mnemonic
0x0100	UART0 Mode Register 1/2	U1MR1/U1MR2	**U0MR1/U0MR2**
0x0104	UART0 Status	U1SR	**U0SR**
0x0104	UART0 Clock Select Register	U1CSR	**U0CSR**
0x0108	UART0 Command Register	U1CR	**U0CR**
0x010C	UART0 Receive Buffer	U1RxB	**U0RxB**
0x010C	UART0 Transmit Buffer	U1TxB	**U0TxB**
0x0110	UART0 CTS Change Register	U1CCR	**U0CCR**
0x0110	UART0 Auxiliary Control Register	U1ACR	**U0ACR**
0x0114	UART0 Interrupt Status Register	U1ISR	**U0ISR**
0x0114	UART0 Interrupt Mask Register	U1IMR	**U0IMR**
0x0118	UART0 Baud Prescaler MSB	U1BG1	**U0BG1**
0x011C	UART0 Baud Prescaler LSB	U1BG2	**U0BG2**
0x0120	UART0 AutoBaud MSB Register	U1ABR1	**U0ABR1**
0x0124	UART0 AutoBaud LSB Register	U1ABR2	**U0ABR2**
0x0128	UART0 TxFIFO Control/Status Register	U1TxFCSR	**U0TxFCSR**
0x012C	UART0 RxFIFO Control/Status Register	U1RxFCSR	**U0RxFCSR**
0x0134	UART0 CTS Unlatched Input	U1IP	**U0IP**
0x0138	UART0 RTS O/P Bit Set Command Register	U1OP1	**U0OP1**
0x013C	UART0 RTS O/P Bit Reset Command Register	U1OP0	**U0OP0**

Table 9. UART1 Module Memory Map

MBAR Offset	Register Name	Old Mnemonic	New Mnemonic
0x0140	UART1 Mode Register 1/2	U2MR1/U2MR2	**U1MR1/U1MR2**
0x0144	UART1 Status	U2SR	**U1SR**
0x0144	UART1 Clock Select Register	U2CSR	**U1CSR**
0x0148	UART1 Command Register	U2CR	**U1CR**
0x014C	UART1 Receive Buffer	U2RxB	**U1RxB**
0x014C	UART1 Transmit Buffer	U2TxB	**U1TxB**
0x0150	UART1 CTS Change Register	U2CCR	**U1CCR**
0x0150	UART1 Auxiliary Control Register	U2ACR	**U1ACR**
0x0154	UART1 Interrupt Status Register	U2ISR	**U1ISR**
0x0154	UART1 Interrupt Mask Register	U2IMR	**U1IMR**
0x0158	UART1 Baud Prescaler MSB	U2BG1	**U1BG1**
0x015C	UART1 Baud Prescaler LSB	U2BG2	**U1BG2**
0x0160	UART1 AutoBaud MSB Register	U2ABR1	**U1ABR1**
0x0164	UART1 AutoBaud LSB Register	U2ABR2	**U1ABR2**
0x0168	UART1 TxFIFO Control/Status Register	U2TxFCSR	**U1TxFCSR**
0x016C	UART1 RxFIFO Control/Status Register	U2RxFCSR	**U1RxFCSR**
0x0174	UART1 CTS Unlatched Input	U2IP	**U1IP**
0x0178	UART1 RTS O/P Bit Set Command Register	U2OP1	**U1OP1**
0x017C	UART1 RTS O/P Bit Reset Command Register	U2OP0	**U1OP0**

Table 10. SDRAM Controller Memory Map

MBAR Offset	Register Name	Old Mnemonic	New Mnemonic
0x0182	SDRAM Configuration Register	SDCCR	**SDCR**
0x0186	SDRAM Timing Register	SDCTR	**SDTR**

Table 11. Timer Module Memory Map

MBAR Offset	Register Name	Old Mnemonic	New Mnemonic
0x0200	Timer 0 Mode Register	TMR1	**TMR0**
0x0204	Timer 0 Reference Register	TRR1	**TRR0**
0x0208	Timer 0 Capture Register	TCR1	**TCAP0**
0x020C	Timer 0 Counter Register	TCN1	**TCN0**
0x0210	Timer 0 Event Register	TER1	**TER0**
0x0220	Timer 1 Mode Register	TMR2	**TMR1**
0x0224	Timer 1 Reference Register	TRR2	**TRR1**
0x0228	Timer 1 Capture Register	TCR2	**TCAP1**
0x022C	Timer 1 Counter Register	TCN2	**TCN1**
0x0230	Timer 1 Event Register	TER2	**TER1**
0x0240	Timer 2 Mode Register	TMR3	**TMR2**
0x0244	Timer 2 Reference Register	TRR3	**TRR2**
0x0248	Timer 2 Capture Register	TCR3	**TCAP2**
0x024C	Timer 2 Counter Register	TCN3	**TCN2**
0x0250	Timer 2 Event Register	TER3	**TER2**
0x0260	Timer 3 Mode Register	TMR4	**TMR3**
0x0264	Timer 3 Reference Register	TRR4	**TRR3**
0x0268	Timer 3 Capture Register	TCR4	**TCAP3**
0x026C	Timer 3 Counter Register	TCN4	**TCN3**
0x0270	Timer 3 Event Register	TER4	**TER3**
0x0280	Watchdog Reset Reference Register	WRRR	No change
0x0284	Watchdog Interrupt Reference Register	WIRR	No change
0x0288	Watchdog Counter Register	WCR	No change
0x028C	Watchdog Event Register	WER	No change

Table 12. PLIC Module Memory Map

MBAR Offset	Register Name	Old Mnemonic	New Mnemonic
0x0300	Port0 B1 Data Receive	PLRB10	**P0B1RR**
0x0304	Port1 B1 Data Receive	PLRB11	**P1B1RR**
0x0308	Port2 B1 Data Receive	PLRB12	**P2B1RR**
0x030C	Port3 B1 Data Receive	PLRB13	**P3B1RR**
0x0310	Port0 B2 Data Receive	PLRB20	**P0B2RR**
0x0314	Port1 B2 Data Receive	PLRB21	**P1B2RR**
0x0318	Port2 B2 Data Receive	PLRB22	**P2B2RR**
0x031C	Port3 B2 Data Receive	PLRB23	**P3B2RR**
0x0320	Port0-3 D Data Receive	PLRD0 PLRD1 PLRD2 PLRD3	**P0DRR** **P1DRR** **P2DRR** **P3DRR**
0x0328	Port0 B1 Data Transmit	PLTB10	**P0B1TR**
0x032C	Port1 B1 Data Transmit	PLTB11	**P1B1TR**
0x0330	Port2 B1 Data Transmit	PLTB12	**P2B1TR**
0x0334	Port3 B1 Data Transmit	PLTB13	**P3B1TR**
0x0338	Port0 B2 Data Transmit	PLTB20	**P0B2TR**
0x033C	Port1 B2 Data Transmit	PLTB21	**P1B2TR**
0x0340	Port2 B2 Data Transmit	PLTB22	**P2B2TR**
0x0344	Port3 B2 Data Transmit	PLTB23	**P3B2TR**
0x0348	Port0-3 D Data Transmit	PLTD0 PLTD1 PLTD2 PLTD3	**P0DTR** **P1DTR** **P2DTR** **P3DTR**
0x0350	Port0-1 GCI/IDL Configuration Register	PLCR0 PLCR1	**P0CR** **P1CR**
0x0354	Port2-3 GCI/IDL Configuration Register	PLCR2 PLCR3	**P2CR** **P3CR**
0x0358	Port0-1 Interrupt Configuration Register	PLICR0 PLICR1	**P0ICR** **P1ICR**
0x035C	Port2-3 Interrupt Configuration Register	PLICR2 PLICR3	**P2ICR** **P3ICR**
0x0360	Port0-1 GCI Monitor RX	PLGMR0 PLGMR1	**P0GMR** **P1GMR**
0x0364	Port2-3 GCI Monitor RX	PLGMR2 PLGMR3	**P2GMR** **P3GMR**
0x0368	Port0-1 GCI Monitor TX	PLGMT0 PLGMT1	**P0GMT** **P1GMT**
0x036C	Port2-3 GCI Monitor TX	PLGMT2 PLGMT3	**P2GMT** **P3GMT**

Table 12. PLIC Module Memory Map (Continued)

MBAR Offset	Register Name	Old Mnemonic	New Mnemonic
0x0370	GCI Monitor TX Status GCI Monitor TX abort	PLGMTS PLGMTA	**PGMTS** **PGMTA**
0x0374	Port0-3 GCI C/I RX	PLGCIR0 PLGCIR1 PLGCIR2 PLGCIR3	**P0GCIR** **P1GCIR** **P2GCIR** **P3GCIR**
0x0378	Port0-3 GCI C/I TX	PLGCIT0 PLGCIT1 PLGCIT2 PLGCIT3	**P0GCIT** **P1GCIT** **P2GCIT** **P3GCIT**
0x037C	GCI C/I TX Status	PGCITSR	No change
0x0384	Port0-1 Periodic Status	PLPSR0 PLPSR1	**P0PSR** **P1PSR**
0x0388	Port2-3 Periodic Status	PLPSR2 PLPSR3	**P2PSR** **P3PSR**
0x038C	Aperiodic Interrupt Status Register; Loop back Control	PLASR PLLCR	**PASR** **PLCR**
0x0392	D Channel Request	PLDRQ	**PDRQR**
0x0394	Port0-1 Sync Delay	PLSD0 PLSD1	**P0SDR** **P1SDR**
0x0398	Port2-3 Sync Delay	PLSD2 PLSD3	**P2SDR** **P3SDR**
0x039C	Clock Select	PLCKSEL	**PCSR**

Table 13. Ethernet Module Memory Map

MBAR Offset	Register Name	Old Mnemonic	New Mnemonic
0x0840	Ethernet Control Register	ECNTRL	**ECR**
0x0844	Ethernet Interrupt Event Register	IEVENT	**EIR**
0x0848	Ethernet Interrupt Mask Register	IMASK	**EIMR**
0x084C	Ethernet Interrupt Vector Status	IVEC	**IVSR**
0x0850	Ethernet Rx Ring Updated Flag	R_DES_ACTIVE	**RDAR**
0x0854	Ethernet Tx Ring Updated Flag	X_DES_ACTIVE	**TDAR**
0x0880	Ethernet MII Data Register	MII_DATA	**MMFR**
0x0884	Ethernet MII Speed Register	MII_SPEED	**MSCR**
0x08CC	Ethernet Receive Bound Register	R_BOUND	**FRBR**
0x08D0	Ethernet Rx FIFO Start Address	R_FSTART	**FRSR**
0x08E4	Transmit FIFO Watermark	X_WMRK	**TFWR**
0x08EC	Ethernet Tx FIFO Start Address	X_FSTART	**TFSR**
0x0944	Ethernet Rx Control Register	R_CNTRL	**RCR**
0x0948	Maximum Frame Length Register	MAX_FRM_LEN	**MFLR**
0x0984	Ethernet Tx Control Register	X_CNTRL	**TCR**
0x0C00	Ethernet Address (Lower)	ADDR_LOW	**MALR**
0x0C04	Ethernet Address (Upper)	ADDR_HIGH	**MAUR**
0x0C08	Ethernet Hash Table (Upper)	HASH_TABLE_HIGH	**HTUR**
0x0C0C	Ethernet Hash Table (Lower)	HASH_TABLE_LOW	**HTLR**
0x0C10	Ethernet Rx Descriptor Ring	R_DES_START	**ERDSR**
0x0C14	Ethernet Tx Descriptor Rin	X_DES_START	**ETDSR**
0x0C18	Ethernet Rx Buffer Size	R_BUFF_SIZE	**EMRBR**
0x0C40 – 0x0DFF	FIFO RAM	E_FIFO	**EFIFO**

Table 14. USB Module Memory Map

MBAR Offset	Register Name	Old Mnemonic	New Mnemonic
0x1002	USB Frame Number Register	USBFNR	**FNR**
0x1006	USB Frame Number Match Register	USBFNMR	**FNMR**
0x100A	USB Real-time Frame Monitor Register	USBRTFMR	**RFMR**
0x100E	USB Real-time Frame Monitor Match Register	USBRTFMMR	**RFMMR**
0x1013	USB Function Address Register	USBFAR	**FAR**
0x1014	USB Alternate Setting Register	USBASR	**ASR**
0x1018	USB Device Request Data1 Register	USBDRR1	**DRR1**
0x101C	USB Device Request Data2 Register	USBDRR2	**DRR2**
0x1022	USB Specification Number Register	USBSPECR	**SPECR**
0x1026	USB Endpoint 0 Status Register	USBEPSR0	**EP0SR**
0x1028	USB Endpoint 0 IN Config Register	USBEPICFG0	**IEP0CFG**
0x102C	USB Endpoint 0 OUT Config Register	USBEPOCFG0	**OEP0CFG**
0x1030	USB Endpoint 1 Configuration Register	USBEPCFG1	**EP1CFG**
0x1034	USB Endpoint 2 Configuration Register	USBEPCFG2	**EP2CFG**
0x1038	USB Endpoint 3 Configuration Register	USBEPCFG3	**EP3CFG**
0x103C	USB Endpoint 4 Configuration Register	USBEPCFG4	**EP4CFG**
0x1040	USB Endpoint 5 Configuration Register	USBEPCFG5	**EP5CFG**
0x1044	USB Endpoint 6 Configuration Register	USBEPCFG6	**EP6CFG**
0x1048	USB Endpoint 7 Configuration Register	USBEPCFG7	**EP7CFG**
0x104C	USB Endpoint 0 Control Register	USBEPCTL0	**EP0CTL**
0x1052	USB Endpoint 1 Control Register	USBEPCTL1	**EP1CTL**
0x1056	USB Endpoint 2 Control Register	USBEPCTL2	**EP2CTL**
0x105A	USB Endpoint 3 Control Register	USBEPCTL3	**EP3CTL**
0x105E	USB Endpoint 4 Control Register	USBEPCTL4	**EP4CTL**
0x1062	USB Endpoint 5 Control Register	USBEPCTL5	**EP5CTL**
0x1066	USB Endpoint 6 Control Register	USBEPCTL6	**EP6CTL**
0x106A	USB Endpoint 7 Control Register	USBEPCTL7	**EP7CTL**
0x106C	USB General/Endpoint 0 Interrupt Status Register	USBEPISR0	**EP0ISR**
0x1072	USB Endpoint 1 Interrupt Status Register	USBEPISR1	**EP1ISR**
0x1076	USB Endpoint 2 Interrupt Status Register	USBEPISR2	**EP2ISR**
0x107A	USB Endpoint 3 Interrupt Status Register	USBEPISR3	**EP3ISR**
0x107E	USB Endpoint 4 Interrupt Status Register	USBEPISR4	**EP4ISR**
0x1082	USB Endpoint 5 Interrupt Status Register	USBEPISR5	**EP5ISR**
0x1086	USB Endpoint 6 Interrupt Status Register	USBEPISR6	**EP6ISR**
0x108A	USB Endpoint 7 Interrupt Status Register	USBEPISR7	**EP7ISR**

Table 14. USB Module Memory Map (Continued)

MBAR Offset	Register Name	Old Mnemonic	New Mnemonic
0x108C	USB Endpoint 0 Interrupt Mask Register	USBEPIMR0	**EP0IMR**
0x1092	USB Endpoint 1 Interrupt Mask Register	USBEPIMR1	**EP1IMR**
0x1096	USB Endpoint 2 Interrupt Mask Register	USBEPIMR2	**EP2IMR**
0x109A	USB Endpoint 3 Interrupt Mask Register	USBEPIMR3	**EP3IMR**
0x109E	USB Endpoint 4 Interrupt Mask Register	USBEPIMR4	**EP4IMR**
0x10A2	USB Endpoint 5 Interrupt Mask Register	USBEPIMR5	**EP5IMR**
0x10A6	USB Endpoint 6 Interrupt Mask Register	USBEPIMR6	**EP6IMR**
0x10AA	USB Endpoint 7 Interrupt Mask Register	USBEPIMR7	**EP7IMR**
0x10AC	USB Endpoint 0 Data Register	USBEPDAT0	**EP0DR**
0x10B0	USB Endpoint 1 Data Register	USBEPDAT1	**EP1DR**
0x10B4	USB Endpoint 2 Data Register	USBEPDAT2	**EP2DR**
0x10B8	USB Endpoint 3 Data Register	USBEPDAT3	**EP3DR**
0x10BC	USB Endpoint 4 Data Register	USBEPDAT4	**EP4DR**
0x10C0	USB Endpoint 5 Data Register	USBEPDAT5	**EP5DR**
0x10C4	USB Endpoint 6 Data Register	USBEPDAT6	**EP6DR**
0x10C8	USB Endpoint 7 Data Register	USBEPDAT7	**EP7DR**
0x10CE	USB Endpoint 0 Data Present Register	USBEPDP0	**EP0DPR**
0x10D2	USB Endpoint 1 Data Present Register	USBEPDP1	**EP1DPR**
0x10D6	USB Endpoint 2 Data Present Register	USBEPDP2	**EP2DPR**
0x10DA	USB Endpoint 3 Data Present Register	USBEPDP3	**EP3DPR**
0x10DE	USB Endpoint 4 Data Present Register	USBEPDP4	**EP4DPR**
0x10E2	USB Endpoint 5 Data Present Register	USBEPDP5	**EP5DPR**
0x10E6	USB Endpoint 6 Data Present Register	USBEPDP6	**EP6DPR**
0x10EA	USB Endpoint 7 Data Present Register	USBEPDP7	**EP7DPR**
0x1400 – 0x17FF	USB Configuration RAM, 1 K Bytes	USB_CFG_RAM	No change

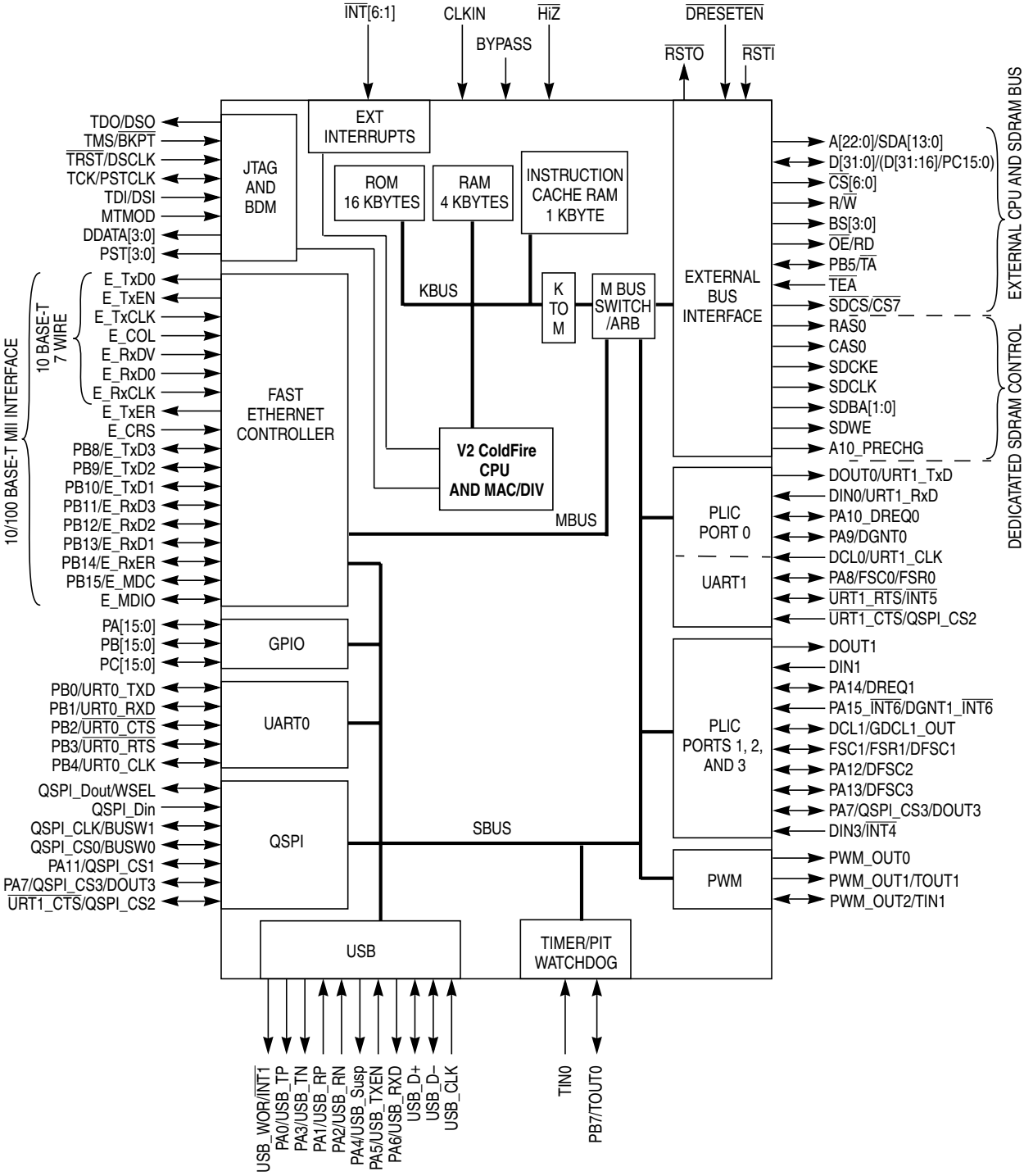
NOTE:

The MBAR Offset column corresponds to Tables A-1 through A-16 of the *MCF5272 User's Manual* (Motorola document order number MCF5272UM/D). 16- and/or 8-bit wide registers may be offset by 0, 1, 2, or 3 bytes from the offset address shown above. Refer to the *MCF5272 User's Manual* for actual positioning of 16- or 8-bit registers in a 32-bit long word.

1.2 Chapter 20 Figures

The signal CLKIN should be replaced by SDCLK in Figures 20-3, 20-4 through 20-17, and 20-20.

1.3 MCF5272 Block Diagram with Signal Interfaces



NOTE: GPIO pins shown above are multiplexed with most other signals.

2. Section and Page

7.2.1/7-3	Table 7-2. Interrupt and Power Management Register Mnemonics. Replace text: TMR1, TMR2, TMR3, TMR4 with TMR0, TMR1, TMR2, TMR3. Replace text: Timers 1-4 …. with Timers 3-0 …
7.2.2.1/7-4	Figure 7-2. Interrupt Control Register 1 (ICR1) Replace text: TMR1, TMR2, TMR3, TMR4 with TMR0, TMR1, TMR2, TMR3.
7.2.3/7-7	Figure 7-6. Interrupt Source Register (ISR) Replace text: TMR1, TMR2, TMR3, TMR4 with TMR0, TMR1, TMR2, TMR3.
7.2.5./7-9	Figure 7-8. Programmable Interrupt Wakeup Register (PIWR) Replace text: TMR1, TMR2, TMR3, TMR4 with TMR0, TMR1, TMR2, TMR3. Correct bits 31-4 description in Table 7-6 to: 0 Interrupt cannot wake up the CPU when interrupt source is active. 1 Interrupt wakes up the CPU from low-power modes.
7.2.6/7-10	Table 7-8. MCF5272 Interrupt Vector Table Replace text: TMR1, TMR2, TMR3, TMR4 with TMR0, TMR1, TMR2, TMR3. Replace text: Timer 1, Timer 2, Timer 3, Timer 4 with Timer 0, Timer 1, Timer 2, Timer 3.
9.3/9-5—9-6	Tables 9-3, 9-4, 9-5, and 9-6 Change Mbytes in the column headings to Mbits.
9.5.1/9-7	Figure 9-3. SDRAM Configuration Register (SDCR) The correct address of this 16-bit register is: MBAR + 0x0182
9.5.2/9-9	Figure 9-4. SDRAM Timing Register (SDTR) The correct address of this 16-bit register is: MBAR + 0x0186
12.3.2.13/12-17	Figure 12-16. USB Endpoint 0 Control Register Change reset value for bits 31:23 to 0x00. Change reset value for bits 22:16 to 0x00. Change reset value for bits 15:8 to 0x00. Change reset value for bits 7:0 to 0x04.

12.3.2.14/12-20	Figure 12-17. USB Endpoint 1-7 Control Register Change reset value for bits 15:8 to 0x00. Change reset value for bits 7:0 to 0x04.
13.3.2/13-14	Figure 3-11. PLIC Internal Timing Signal Routing At the top left of the figure, change P1CR[SFSM] to P1CR[FSM].
13.5.7/13-20	Figure 13-19. Port Configuration Registers (P0CR–-P3CR) In the address row, the address for P1CR should be 0x352 and the address for P2CR should be 0x354.
14.4.2/14-6	Baud Rate Selection Add the following sentence: The maximum QSPI clock frequency is one-fourth the clock frequency applied at the CLKIN pin. Change the first sentence to: Baud rate is selected by writing a value from 2–255 into QMR[BAUD].
14.4.2/14-7	Table 14-2. QSPI_CLK Frequency as Function of CPU Clock and Baud Rate Remove row corresponding to QMR[BAUD] = 1.
14.5.7/14-15	Table 14-7. QCR0–QCR15 Field Descriptions Add these sentences to the description for bits 11–8 QSPI_CS: Bits 11–8 map directly to QSPI_CS[3:0], respectively. If it is desired to use those bits as a chip select value, then an external demultiplexor must be connected to the QSPI_CS[3:0] pins.
14.5.8/14-15	Programming Example Item 1, second sentence should be changed to: Write PACNT with 0x0080_4000 to enable QSPI_CS1 and QSPI_CS3.
17.1/17-1	General Purpose I/O Module Overview Change second sentence of first paragraph to: The GPIO signal multiplexing is shown in Table 17-1.
17.2.2/17-6	Table 17-5. PBCNT Field Descriptions Change description for bits 23–22 PBCNT11 to: 1x Reserved.
17.2.2/17-7	Table 17-5. PBCNT Field Descriptions Replace bits 3-2 description text: TIN3 with TIN2. (2 places).
17.2.2/17-7	Table 17-6. Port B Control Register Function Bits Replace text: TIN3 with TIN2.

17.2.4/17-8 Table 17-7. PDCNT Field Descriptions
Replace bits 15-14 description text: PWM_OUT3 with PWM_OUT2.
Replace bits 13-12 description text: PWM_OUT2 with PWM_OUT1.
Replace bits 3-2 description text: TIN4 with TIN3. (2 places).

17.2.4/17-9 Table 17-8. Port D Control Register Function Bits
Replace text: TIN4 with TIN3.
Replace text: TIN1 with TIN0.
Replace text: PWM_OUT3 with PWM_OUT2.
Replace test: PWM_OUT2 with PWM_OUT1.
Replace footnote text: timer 4 with timer 3.

19.2/19-16 Address Bus……..
Change section title to:
Address Bus (A[22:0], SDA[13:0])
Change signal name of first paragraph to:
SDA[13:0]

19.4/19-17 Chip Selects…….
Change section title to:
Chip Selects ($\overline{CS7}$/$\overline{SDCS}$, $\overline{CS}$[6:0])

19.5.5/19-19 Hi-Z
Correct signal name to
$\overline{HiZ}$
Add the following text:
Hi-Z configuration input is sampled on the rising edge of Reset Output ($\overline{RSTO}$).

19.14.1/19-28 QSPI Synchronous Serial Data Output (QSPI_Dout)
The section title should be:
QSPI Synchronous Serial Data Output (QSPI_Dout/WSEL)
Add the following text:
WSEL configuration input is sampled on the rising edge of Reset Output ($\overline{RSTO}$).

19.14.3/19-28 QSPI Serial Clock (QSPI_CLK/BUSW1)
Add the following text:
BUSW1 configuration input is sampled on the rising edge of Reset Output ($\overline{RSTO}$).

19.14.4/19-28 Synchronous Peripheral Chip Select 0 (QSPI_CS0/BUSW0)
Add the following text:
BUSW0 configuration input is sampled on the rising edge of Reset Output ($\overline{RSTO}$).

19.14.7/19-29 Synchronous Peripheral chip select 3
Remove sentence:
QSPI_CS3 can be programmed to be active high or low.

19.15/19-29 Physical Layer Interface Controller PLIC Ports
Change section title to:
Physical Layer Interface Controller PLIC Ports and UART 1.

19.15.3.3/19-33 QSPI_CS3, Port 3 GCI/IDL ……
Add the following sentence to QSPI mode description:
QSPI_CS3 can be programmed to be active high or low.

19.17/19-36 Operating Mode Configuration Pins
Add the following text:
These signals are sampled on the rising edge of Reset Output ($\overline{\text{RSTO}}$).

19.18/19-37 Power Supply Pins
Change text to:
The VDD/GND pins are connected to 3.3 V supply and associated ground. When the on-chip USB transceiver is used, the USB_VDD and USB_GND pins are connected to the 3.3 V device supply and associated ground. When the on-chip USB transceiver is not used, USB_GND should be connected to the device GND and USB_VDD left unconnected. Refer to Section 12.2.1.1 USB Transceiver Interface.

20.5.1/20-7 Table 20-3. Data Bus Byte Strobes
Replace Table 20-3 with the following three tables:

Table 15. Byte Strobe Operation for 32-Bit Data Bus

$\overline{\text{BS3}}$	$\overline{\text{BS2}}$	$\overline{\text{BS1}}$	$\overline{\text{BS0}}$	Access Type	Access Size	Data Located On
1	1	1	1	None	None	—
1	1	1	0	FLASH/SRAM	Byte	D[31:24]
1	1	0	1	FLASH/SRAM		D[23:16]
1	0	1	1	FLASH/SRAM		D[15:8]
0	1	1	1	FLASH/SRAM		D[7:0]
1	1	0	0	FLASH/SRAM	Word	D[31:16]
0	0	1	1	FLASH/SRAM		D[15:0]
0	0	0	0	FLASH/SRAM	Longword	D[31:0]
1	1	1	0	SDRAM	Byte	D[7:0]
1	1	0	1	SDRAM		D[15:8]
1	0	1	1	SDRAM		D[23:16]
0	1	1	1	SDRAM		D[31:24]
1	1	0	0	SDRAM	Word	D[15:0]
0	0	1	1	SDRAM		D[31:16]
0	0	0	0	SDRAM	Longword	D[31:0]

Table 16. Byte Strobe Operation for 16-Bit Data Bus-SRAM Cycles

$\overline{BS1}$	$\overline{BS0}$	Access Size	Data Located On
1	1	None	—
1	0	Byte	D[31:24]
0	1	Byte	D[23:16]
0	0	Word	D[31:16]

Table 17. Byte Strobe Operation for 16-Bit Data Bus-SDRAM Cycles

$\overline{BS3}$	$\overline{BS2}$	Access Type	Data Located On
1	1	None	—
1	0	Byte	D[23:16]
0	1	Byte	D[31:24]
0	0	Word	D[31:16]

20.12.2/20-26 Normal Reset

Add the following sentence at end of first paragraph:

At power on reset both $\overline{RSTI}$ and $\overline{DRESETEN}$ must be asserted simultaneously. If $\overline{DRESETEN}$ is not asserted at the same time as $\overline{RSTI}$ at power up the SDRAMC cannot be initialized by software.

Change first sentence of third paragraph to:

The levels of the mode select inputs, QSPI_Dout/WSEL, QSPI_CLK/BUSW1, QSPI_CS0/BUSW0, and $\overline{HiZ}$ are sampled when $\overline{RSTO}$ negates and select the port size of $\overline{CS0}$ and the physical data bus width after a master reset occurs.

22.1/22-1 Figure 22-1. MCF5272 Pinout (196 MAPBGA)

The pin names should be corrected as follows:

Pin Number	Correct Name
F4	$\overline{RSTO}$
K6	PWM_OUT2/TIN1
K2	$\overline{URT1_CTS}$/QSPI_CS2
K10	$\overline{CS1}$
L11	$\overline{CS5}$
M2	PA14/DREQ1
M12	$\overline{RSTI}$
N5	PWM_OUT0
N11	$\overline{CS3}$
N12	$\overline{DRESETEN}$
N14	$\overline{HiZ}$
P5	PWM_OUT1/TOUT1
P11	$\overline{CS2}$
P12	$\overline{CS6}$

23.2/23-3 Table 23-4. DC Electrical Specifications
For input leakage specifications list, change DRQ to $\overline{\text{IRQ}}$[6:1]

23.2.1/23-3 Output Driver Capability and Loading
Change all 11 mA drive capable pins to 10 mA.
Change all 7 mA drive capable pins to 6 mA.
Change 5 mA drive capable pin to 4 mA.

23.3.2/23-6 Processor Bus Input Timing Specifications
Change characteristic text for bus spec item B1f to:
Mode selects (BUSW[1:0], WSEL, $\overline{\text{HiZ}}$) valid to SDCLK (setup) (when $\overline{\text{RSTI}}$ asserted)
Change characteristic text for bus spec item B2d to:
SDCLK to asynchronous control inputs ($\overline{\text{RSTI}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{INT}}$x) invalid (hold)

23.4.9/23-28 QSPI Electrical Specifications
Change QSPI spec item QS3 to a maximum of 12 ns instead of 12.5 ns.

A.2/A-7 Table A-12. SDRAM Controller Memory Map
The correct registor locations are shown below.

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x0180	Reserved		SDRAM Configuration Register (SDCR)	
0x0184	Reserved		SDRAM Timing Register (SDTR)	

A.2/A-8 Table A-14. PLIC Module Memory Map
The user's manual implies port 0, 1, 2, and 3 D data transmit registers are 32 bits wide. These registers are eight bits wide. The correct register mapping is shown below.

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x0348	Port 0 D Data Transmit (P0DTR)	Port 1 D Data Transmit (P1DTR)	Port 2 D Data Transmit (P2DTR)	Port 3 D Data Transmit (P3DTR)

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