XCF5272

Errata to XCF5272

Preface

This document identifies implementation differences between the XCF5272 processor and the description contained in the XCF5272 User's Manual. Please check the Web at http://www.motorola.com/ColdFire for the latest updates.

This errata applies to the 1K75N mask version of the part. The 1K75N version can be identified as follows:

- SIMBC Device ID Register (DIR) having 32-bit value of 0x2440 301D
- JTAG ID Register having 32-bit value of 0x2440 301D
- USB Specification Number Register (SPECR) having 16-bit value of 0x1101

This errata lists differences from the XCF5272 User's Manual.

Table 1 summarizes the XCF5272 errata.

Table 1. Summary of XCF5272 Errata

Errata ID	Module Affected	Date Errata Added	Errata Title
1.	USB	21 May 2001	USB module sends zero length packet instead of NAK in response to request from host
2.	USB	21 May 2001	USB signal eye meets V1.1 spec with waiver
3.	USB	4 June 2001	USB D+/D– pins ESD are 700 V HBM and 75 V MM

1. USB module sends zero length packet instead of NAK in response to request from host

This errata applies to all USB Endpoint Control Registers (EPnCTL).

1.1 Description of problem

The USB module issues a zero-length data packet instead of a NAK when an endpoint receives an IN request (device to host transfer) and the endpoint has no data to send. Refer to Table 8-2 of USB v1. 1 specification (section 8.4.5.1). This problem manifests itself when communicating with PCs running the Microsoft Windows Communications Device Class USB driver. This driver is normally included with Windows Millennium Edition operating system and upgrades for the Windows 98 operating system. The Windows USB Communications Device Class driver responds with an ACK to the zero-length packet returned by the XCF5272 and then no longer generates any further tokens.

On the XCF5272, the response to an IN request is controlled by the IN_DONE bit. There is an IN_DONE bit associated with each of the 8 endpoints. See descriptions for Endpoint Control Registers, EPnCTL. When the IN_DONE bit is set, the USB module only sends maximum size packets or NAK responses if the FIFO (first-in, first out) contains less than a maximum packet size. If the bit is cleared, the USB module sends any amount of data in the FIFO or zero-length packets when the FIFO is empty. By default, this bit is cleared.

The IN_DONE bit operates as follows:

This bit controls the USB module's response to IN packets from the host. This bit must be set at the beginning of a transfer and cleared after all data for the transfer has been written to the FIFO. This bit allows transfers to be handled correctly.

1 = CPU Busy writing transfer into the IN FIFO. The USB module will only send maximum size packets or NAK responses if the FIFO contains less than a maximum size packet.

0 = CPU Done writing transfer into the IN FIFO. The USB module will send any amount of data in the FIFO or zero-length packets when the FIFO is empty.

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1.2 Workarounds

1.2.1 Software Workaround 1

A software workaround has been identified that requires the IN_DONE bit to be set by software at all times. This bit should only be cleared when all of the data for a transfer has been placed into the FIFO. At this point, the USB module will send a partial or zero-length packet indicating the end of a transfer. The software should then reset the IN_DONE bit so that no more zero-length packets are sent. The End-of-Transfer (EOT) status bit should be used (interrupt or polling) to know when to reset the IN_DONE bit. However, it may not be guaranteed that the application software will be able to reset the IN_DONE bit before the host sends another IN request. This timing could vary greatly with processor speed, operating system (device and host), host USB controller, etc.

1.2.2 Software Workaround 2

Provide a product specific USB host driver that substitutes for the standard Microsoft Communications device class driver. This driver should take into account the XCF5272 USB interface software solution described above.

2. USB signal eye meets V1.1 spec with waiver

2.1 Description of problems

2.1.1 Signal eye crossover voltage

Measurements of the USB signal eye crossover voltage for full speed operation have values as high as 2.02 V. The USB specification states that crossover voltage must be in the range of 1.3 V to 2.0 V.

2.1.2 Paired pulse jitter

Full speed jitter is measured for the JK and KJ signal transitions of the USB sync pulse.

For paired pulse JK jitter, the full speed spec is ±1 ns. The XCF5272 passes the source driver jitter spec with waiver due to reported measurement of –617 ps to +2188 ps of jitter.

2.2 Hardware Workaround

There is no existing hardware workaround. Equipment using the on-chip XCF5272 USB I/O transceiver should pass existing USB 1.1 compliance tests with a waiver.

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3. USB D+/D– pins ESD are 700 V HBM and 75 V MM

3.1 Description of problem

ESD HBM testing passed 1 kV except for the USB_D+ and USB_D– pins which pass 700 V. ESD MM testing passed 100 V except for the USB_D+ and USB_D– pins which pass 75 V.

3.2 Workaround

None

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