

## Low-Voltage 1:10 Differential ECL/PECL/HSTL Clock Driver

The MC100EP111 is a low skew 1-to-10 differential driver, designed with clock distribution in mind. It accepts two clock sources into an input multiplexer. The ECL/PECL input signals can be either differential or single-ended if the  $V_{BB}$  output is used. HSTL inputs can be used when the EP111 is operating under PECL conditions. The selected signal is fanned out to 10 identical differential outputs.

- 100ps Part-to-Part Skew typical
- 35ps Output-to-Output Skew typical
- Differential Design
- $V_{BB}$  Output
- Low Voltage  $V_{EE}$  Range of  $-2.25$  to  $-3.8V$  for ECL
- Low Voltage  $V_{CC}$  Range of  $+2.25$  to  $+3.8V$  for PECL and HSTL
- 75k $\Omega$  Input Pulldown Resistors
- ECL/PECL Outputs

The EP111 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate-to-gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent  $t_{pd}$  distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

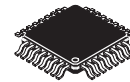
To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50 $\Omega$ , even if only one side is being used. In most applications, all ten differential pairs will be used and therefore terminated. In the case where fewer than ten pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The MC100EP111, as with most other ECL devices, can be operated from a positive  $V_{CC}$  supply in PECL mode. This allows the EP111 to be used for high performance clock distribution in +3.3V or +2.5V systems. Designers can take advantage of the EP111's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using PECL, designers should refer to Motorola Application Note AN1406/D.

The MC100EP111 may be driven single-endedly utilizing the  $V_{BB}$  bias output with the  $\overline{CLK0}$  input. If a single-ended signal is to be used, the  $V_{BB}$  pin should be connected to the  $\overline{CLK0}$  input and bypassed to ground via a 0.01  $\mu F$  capacitor. The  $V_{BB}$  output can only source/sink 0.2mA; therefore, it should be used as a switching reference for the MC100EP111 only. Part-to-Part Skew specifications are not guaranteed when driving the MC100EP111 single-endedly.

**MC100EP111**

**LOW-VOLTAGE  
1:10 DIFFERENTIAL  
ECL/PECL/HSTL  
CLOCK DRIVER**



**FA SUFFIX**  
32-LEAD LQFP PACKAGE  
CASE 873A-02



# MC100EP111

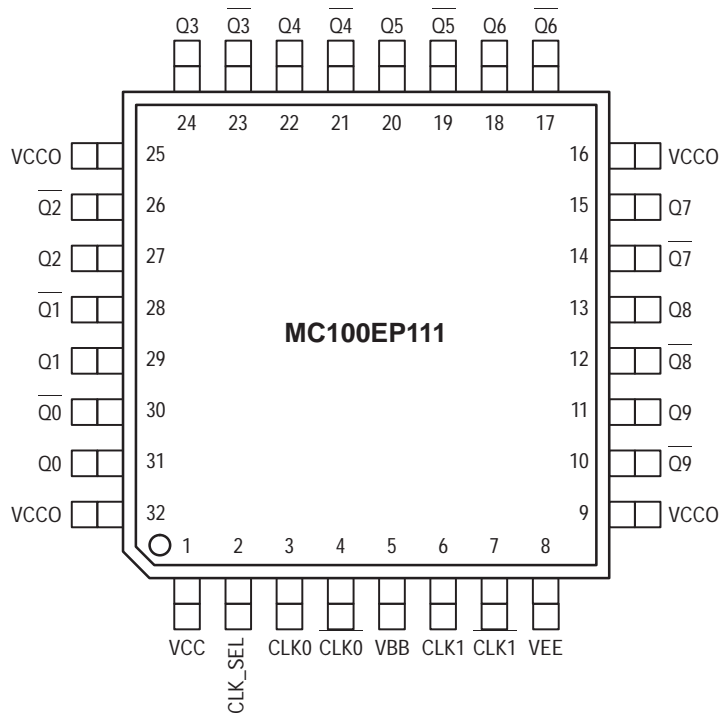


Figure 1. 32-Lead TQFP Pinout (Top View)

## PIN NAMES

Pins	Function
CLK0, $\overline{\text{CLK0}}$	Differential ECL/PECL Input Pair
CLK1, $\overline{\text{CLK1}}$	Differential HSTL Input Pair
Q0:9, $\overline{\text{Q0:9}}$	Differential PECL Outputs
CLK_SEL	Active Clock Select Input
VBB	VBB Output

## FUNCTION

CLK_SEL	Active Input
0	CLK0, $\overline{\text{CLK0}}$
1	CLK1, $\overline{\text{CLK1}}$

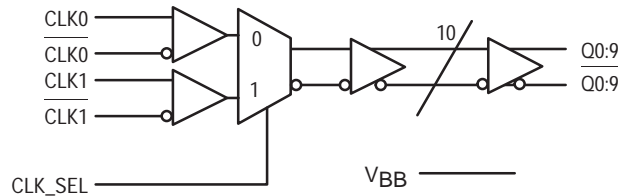


Figure 2. Logic Symbol

## ABSOLUTE MAXIMUM RATINGS\*

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	Supply Voltage	-0.3	4.6	V
$V_I$	Input Voltage	-0.3	$V_{CC} + 0.3$	V
$I_{IN}$	Input Current		$\pm 20$	mA
$T_{Stor}$	Storage Temperature Range	-40	125	$^{\circ}\text{C}$

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

## THERMAL CHARACTERISTICS

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

## DC CHARACTERISTICS

Vsupply : VCC=VCC0 = 0.0 volts, VEE = -2.25 to -3.80 volts

Symbol	Characteristic	-40°C			25°C			70°C			Unit	Condition
		Min	typ	Max	Min	typ	Max	Min	typ	Max		
IEE	Internal supply current	45		85	60		95	65		105	mA	Absolute value of current All outputs terminated 50Ω to VCC=-2.0V Includes pullup/pull-down resistors
ICC	Output and Internal supply current	270		360	290		380	300		380		
IIN	Input current			150			150			150		
VBB	Internally generated bias voltage	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V	for VEE = -3.0 to -3.8 volts for VEE = -2.25 to -2.75 volts
VBB	Internally generated bias voltage	-1.38		-1.16	-1.38		-1.16	-1.38		-1.16		
VIH	Input HIGH voltage (CLK_SEL)	-1.165		-0.880	-1.165		-0.880	-1.165		-0.880	V	Difference of input = $V_{IH} - V_{IL}^1$ Cross point of input = average ( $V_{IH}, V_{IL}$ )
VIL	Input LOW voltage (CLK_SEL)	-1.810		-1.475	-1.810		-1.475	-1.810		-1.475		
VPP	Input amplitude (CLK0,CLK0)	0.5		1.3	0.5		1.3	0.5		1.3		
VCMR	Common mode voltage (CLK0,CLK0)	VEE+1.0		-0.3	VEE+1.0		-0.3	VEE+1.0		-0.3		
VOH	Output HIGH voltage	-1.30		-0.95				-1.20		-0.90	mV	IOH = -30 mA IOL = -5 mA
VOL	Output LOW voltage	-1.85		-1.40				-1.90		-1.50		
VOUtp	Differential output swing	350						500				

## DC CHARACTERISTICS

Vsupply : VCC=VCC0 = 2.25 to 3.80 volts, VEE = 0.0 volts

Symbol	Characteristic	-40°C			25°C			70°C			Unit	Condition
		Min	typ	Max	Min	typ	Max	Min	typ	Max		
IEE	Internal supply current	45		85	60		95	65		105	mA	Absolute value of current All outputs terminated 50Ω to VCC=-2.0V Includes pullup/pull-down resistors
ICC	Output and Internal supply current	270		360	290		380	300		380		
IIN	Input current			150			150			150		
VBB	Internally generated bias voltage	VCC-1.38		VCC-1.26	VCC-1.38		VCC-1.26	VCC-1.38		VCC-1.26	V	for VCC = 3.0 to 3.8 volts for VCC = 2.25 to 2.75 volts
VBB	Internally generated bias voltage	VCC-1.38		VCC-1.16	VCC-1.38		VCC-1.16	VCC-1.38		VCC-1.16		
VIH	Input HIGH voltage (CLK_SEL)	VCC-1.165		VCC-0.880	VCC-1.165		VCC-0.880	VCC-1.165		VCC-0.880	V	Difference of input = $V_{IH} - V_{IL}^1$ Cross point of input = average ( $V_{IH}, V_{IL}$ )
VIL	Input LOW voltage (CLK_SEL)	VCC-1.810		VCC-1.475	VCC-1.810		VCC-1.475	VCC-1.810		VCC-1.475		
VPP	Input amplitude (CLK0,CLK0)	0.5		1.3	0.5		1.3	0.5		1.3		
VCMR	Common mode voltage (CLK0,CLK0)	1		VCC-0.3	1		VCC-0.3	1		VCC-0.3		
Vdif	Differential input voltage (CLK1,CLK1)	0.4		1.9	0.4		1.9	0.4		1.9	V	Difference of input = $V_{IH} - V_{IL}$
Vx	Input crossover voltage (CLK1,CLK1)	0.68		0.9	0.68		0.9	0.68		0.9	V	Cross point of input = average ( $V_{IH}, V_{IL}$ )
VOH	Output HIGH voltage	VCC-1.30		VCC-0.95				VCC-1.20		VCC-0.90	mV	IOH = -30 mA IOL = -5 mA
VOL	Output LOW voltage	VCC-1.85		VCC-1.40				VCC-1.90		VCC-1.50		
VOUtp	Differential output swing	350						500				

Note 1. VPP minimum and maximum required to maintain AC specifications. Actual device function will tolerate minimum VPP of 100 mV.

# MC100EP111

## AC CHARACTERISTICS – PECL Input

Vsupply : VCC=VCC0 = 2.25 to 3.80 volts, VEE = 0.0 volts –OR–  
VCC=VCC0 = 0.0 volts, VEE = –2.25 to –3.80 volts

Symbol	Characteristic	–40°C			25°C			70°C			Unit	Condition
		Min	typ	Max	Min	typ	Max	Min	typ	Max		
Tpd	Differential propagation delay										ps	Nominal (single input condition) VPP = 0.650V, VCMR = VCC–0.800V Note 2
	CLK0, $\overline{\text{CLK0}}$ to all Q0, $\overline{\text{Q0}}$ thru Q9, $\overline{\text{Q9}}$	350		500	380		530	450		600		
	Tsk(part)	Part to part skew			150					150		
Tsk(out-put)	Output to output skew for given part		35	70		30	65		30	60	ps	Note 2
Tpd	Differential propagation delay										ps	Note 2
	CLK0, $\overline{\text{CLK0}}$ to all Q0, $\overline{\text{Q0}}$ thru Q9, $\overline{\text{Q9}}$	280		600	300		620	370		700		
	Tsk(part)	Part to part skew			320					330		
Tsk(out-put)	Output to output skew for given part		35	70		30	65		30	60	ps	Note 2
Fmax	Maximum frequency			1500			1500			1500	MHz	Functional to 1.5 GHz Timing specifications apply up to 1.0 GHz
Tr / Tf	Output rise and fall times (20%, 80%)	100		300	100		300	100		300	ps	All outputs terminated 500Ω to VCC–2.0V

## AC CHARACTERISTICS – HSTL Input

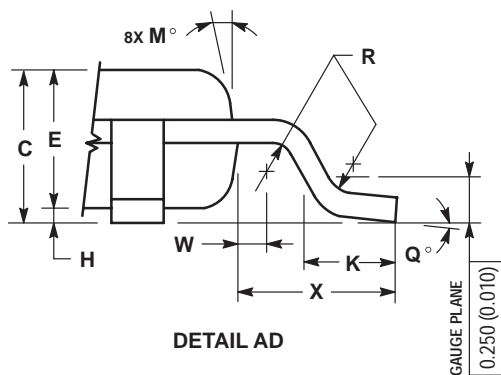
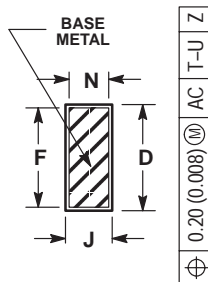
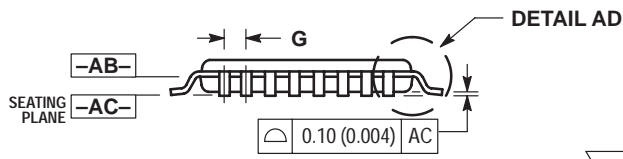
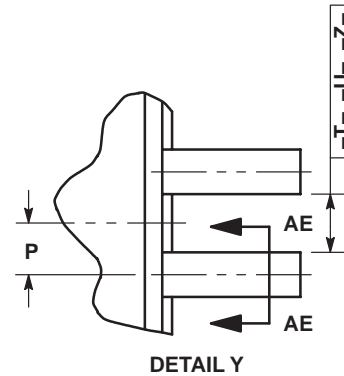
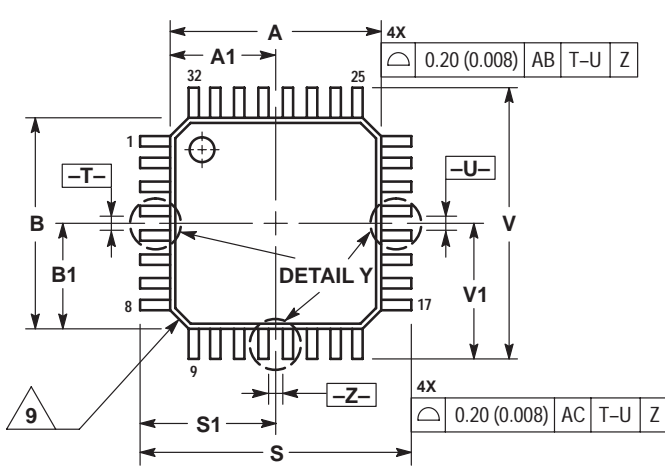
Vsupply : VCC=VCC0 = 2.25 to 3.8 volts, VEE = 0.0 volts

Symbol	Characteristic	–40°C			25°C			70°C			Unit	Condition
		Min	typ	Max	Min	typ	Max	Min	typ	Max		
Tpd	Differential propagation delay										ps	Nominal (single input condition) Vdif = 1.000V, Vx = VEE+0.750V Note 2
	CLK1, $\overline{\text{CLK1}}$ to all Q0, $\overline{\text{Q0}}$ thru Q9, $\overline{\text{Q9}}$	380		530	420		570	500		650		
	Tsk(part)	Part to part skew			150					150		
Tsk(out-put)	Output to output skew for given part		35	70		30	65		30	60	ps	Note 2
Tpd	Differential propagation delay										ps	All input conditions (full input range) Note 2
	CLK1, $\overline{\text{CLK1}}$ to all Q0, $\overline{\text{Q0}}$ thru Q9, $\overline{\text{Q9}}$	300		600	350		650	430		750		
	Tsk(part)	Part to part skew			300					320		
Tsk(out-put)	Output to output skew for given part		35	70		30	65		30	60	ps	Note 2
Fmax	Maximum frequency			250			250			250	MHz	Functional to 250 MHz Timing specifications apply up to 250 MHz
Tr / Tf	Output rise and fall times (20%, 80%)	100		300	100		300	100		300	ps	All outputs terminated 500Ω to VCC–2.0V

Note 2. For operation with 2.5 volt supply, the output termination is 50Ω to VEE. For operation at 3.3 volt supply, the output termination is 50Ω to VCC–2v.

OUTLINE DIMENSIONS

FA SUFFIX  
 PLASTIC LQFP PACKAGE  
 CASE 873A-02  
 ISSUE A




- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: MILLIMETER.
  - DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
  - DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
  - DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
  - DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
  - DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
  - MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
  - EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.000	BSC	0.276	BSC
A1	3.500	BSC	0.138	BSC
B	7.000	BSC	0.276	BSC
B1	3.500	BSC	0.138	BSC
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800	BSC	0.031	BSC
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12°	REF	12°	REF
N	0.090	0.160	0.004	0.006
P	0.400	BSC	0.016	BSC
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000	BSC	0.354	BSC
S1	4.500	BSC	0.177	BSC
V	9.000	BSC	0.354	BSC
V1	4.500	BSC	0.177	BSC
W	0.200	REF	0.008	REF
X	1.000	REF	0.039	REF

## NOTES

## NOTES

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