Low-Cost, Low-Power Level Shifting in Mixed-Voltage Systems

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Introduction

The increasing demand for lower system power consumption has brought many new design challenges. Among them is the problem of safely and efficiently interfacing the various switching levels in today's mixed 3.3-V and 5-V systems while maintaining the lowest possible total system power consumption. Two competing methods of accomplishing this mixed-mode signal translation have emerged:

- Split-rail or dual 3.3-V and 5-V V_{CC} devices
- Completely 5-V tolerant, pure 3.3-V V_{CC} components

This application report deals with the pros and cons of using both device types and offers additional suggestions for even greater system power savings.

Split-Rail Level Shifters

Split-rail level shifters are a class of transceiver devices that have both a 5-V and 3.3-V V_{CC} rail. Products in this class can be used effectively as level shifters and datapath voltage translators, but the following precautions are usually recommended:

- Dual-V_{CC} rail devices typically have strict power sequencing requirements to prevent leakage or even damage to the devices in the event that one V_{CC} rail ramps faster than the other. These stringent requirements are often difficult to meet from a system-timing standpoint and offer little flexibility for partial system power down or other advanced power-saving design techniques.
- Simply because the device has a 5-V V_{CC} pin does not necessarily ensure that the part will actually switch all the way to the 5-V rail. Switching to 5 V is one way to reduce the power consumption in 5-V memories or other pure 5-V CMOS circuits that are driven by a level-shifter device (this application report will demonstrate others as well).

The data sheet for the product in question reveals whether the part drives all the way to the 5-V rail. If the output high-voltage (V_{OH}) minimum is around 4.44 V, it does drive to the rail. Five-volt level shifters with TTL-compatible outputs typically drive only to around 3.6 V.

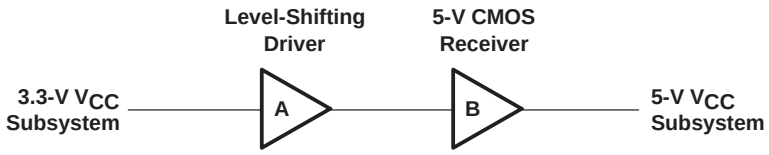
5-V Tolerant, Pure 3.3-V V_{CC} Level Shifters

A second class of products created to meet these design challenges offers the same voltage translation and level-shifting capabilities as the split-rail devices previously mentioned. From a single V_{CC} source, they avoid the power-sequencing problems of the split rails and also are offered in a number of functions, bit widths, and storage options. The one potential drawback of the single-V_{CC} products is that the outputs do not pull all the way to the 5-V V_{CC} rail. But, is this really a drawback?

The Misconception About ΔI_{CC}

The component selection of a level shifter impacts two major aspects of total system-power dissipation:

- The impact that the V_{OH} level of the driving part (A, in Figure 1) has on the power dissipation of the receiving device (B, in Figure 1), commonly known as ΔI_{CC}
- The power of the device itself



Note: Unidirectional mode illustrated for simplicity.

Figure 1. Basic Logic Data Transceiver

ΔI_{CC} is the added power dissipation induced into a TTL-compatible 5-V CMOS device (B, in Figure 1) due to the V_{OH} level of the driving device (A, in Figure 1). It would be correct to expect that a TTL-compatible 5-V CMOS product have higher power dissipation if it was driven by a device with a V_{OH} of 3.6 V than if that same device was driven by a 5-V V_{OH} driver.

Figure 2 shows a typical CMOS input stage and the ΔI_{CC} current associated with switching the device through the input voltage range from 0 to V_{CC}.

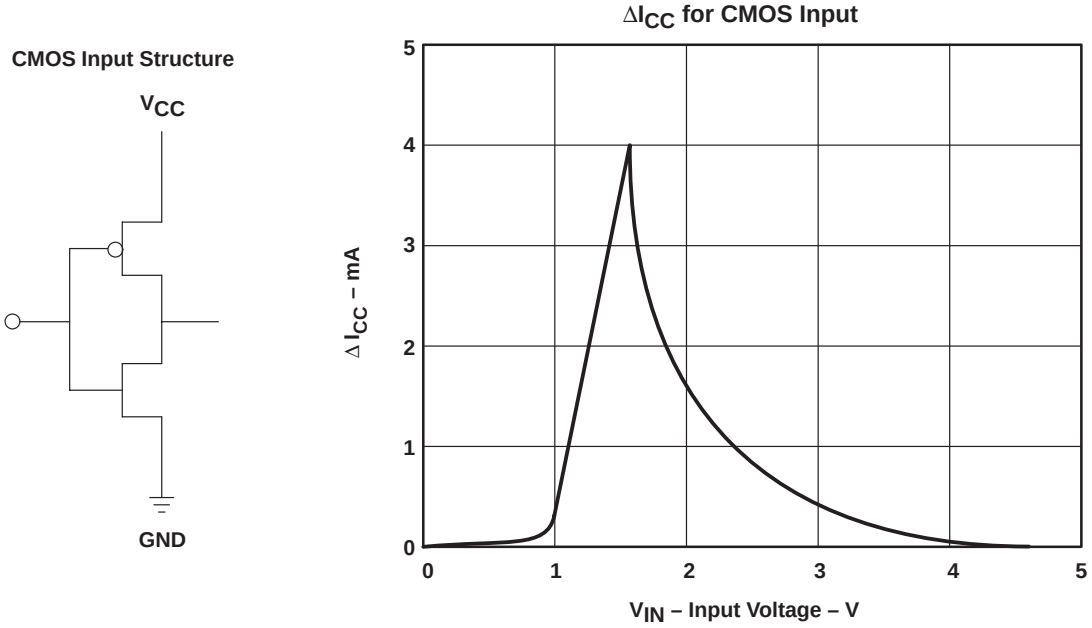


Figure 2. Basic CMOS Input Structure and Typical ΔI_{CC} Current

As expected, the ΔI_{CC} current approaches zero at the V_{CC} and ground rails, and peaks in the TTL-threshold region of 1.5 V.

Figure 3 is a graph of the ΔI_{CC} (i.e., additional I_{CC}) that is induced into a 16-bit device (all outputs switching) as a function of V_{OH} and frequency.

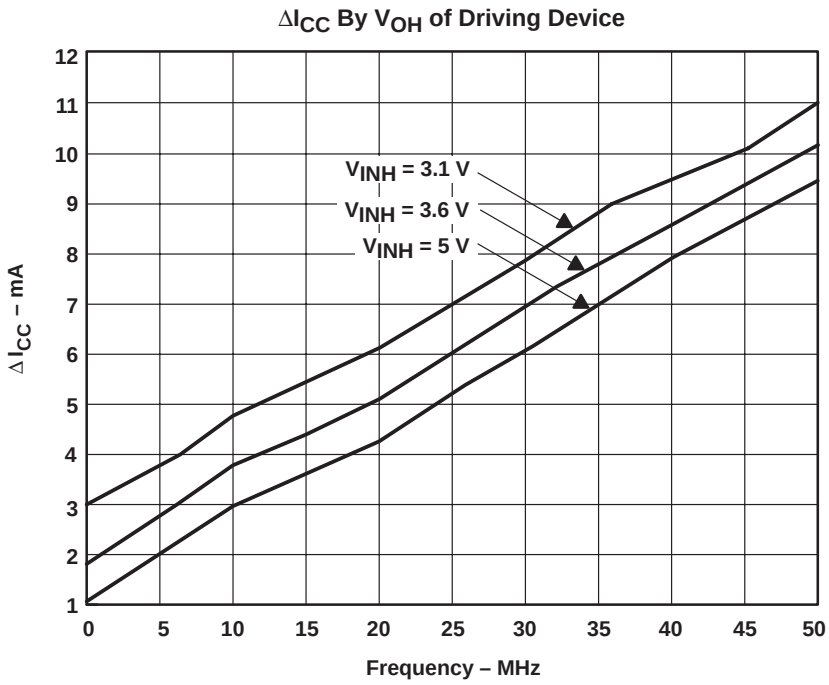


Figure 3. ΔI_{CC} – 16-Bit Device

As shown in Figure 3, ΔI_{CC} is, in fact, 2 to 3 mA higher for the case where V_{OH} is only 3.1 V, than for the same device driven to the 5-V rail by a pure 5-V CMOS device. From this, one might conclude that the best possible solution would be to always select a part that switches all the way to the 5-V rail, but this conclusion fails to consider the impact of system power on the driving device.

Figure 4 shows the V_{OH} of two devices: the FCT164245 split-rail device from Integrated Device Technologies (IDT) and the 'LVT16245A from Texas Instruments.

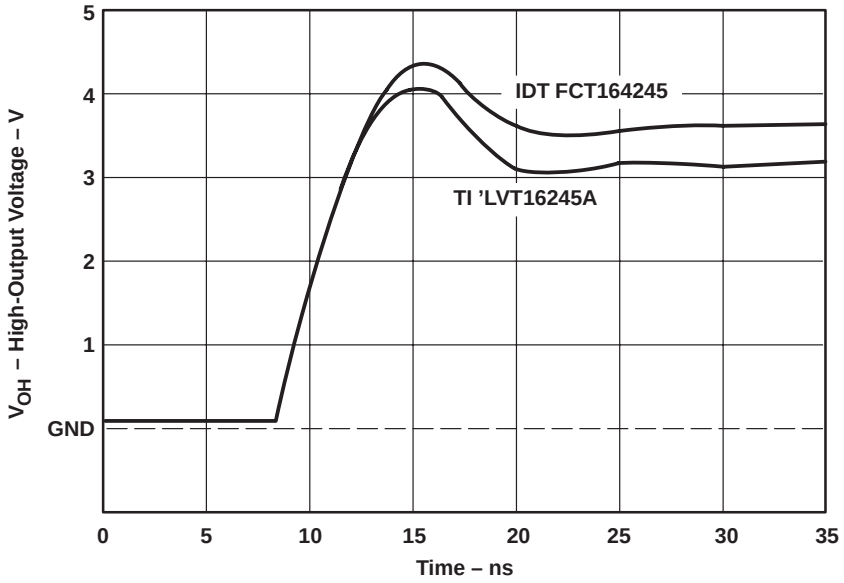


Figure 4. V_{OH} of FCT164245 and 'LVT16245A

From Figure 4, it can be correctly concluded that the induced ΔI_{CC} current in a part driven by the LVT part would be higher than the FCT device. The problem with this conclusion is that ΔI_{CC} is only one of the two components of total system power dissipation that selection of a level-shifter device has from a system standpoint.

Figure 5 shows the total power dissipation of the same IDT split-rail device, the TI 'LVT16245A, and the worst-case ΔI_{CC} (V_{OH} = 3.1 V) plotted on the same vertical scale.

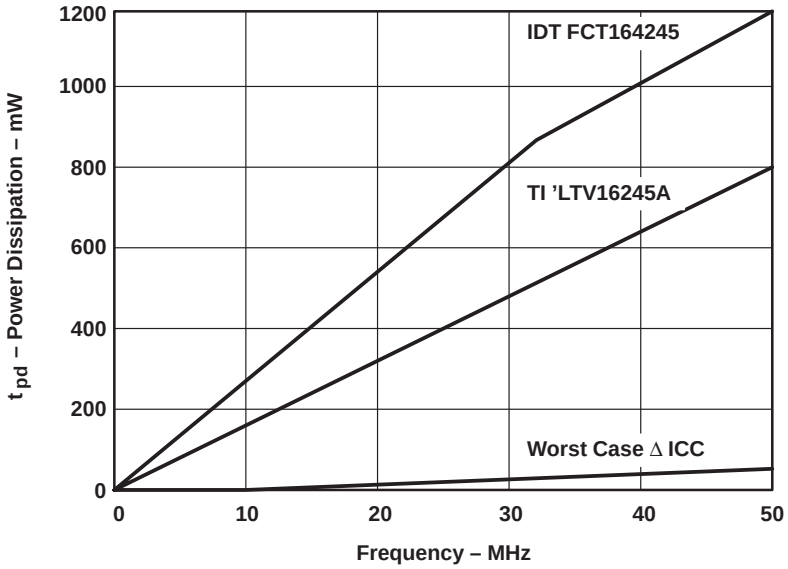


Figure 5. Total-System Power-Dissipation Impact

From Figure 5, it can be seen that, even if a split-rail device pulls all the way to the 5-V rail (which the IDT part does not), the power savings in ΔI_{CC} is more than offset by the huge switching currents that the split rail draws from the 5-V rail. The negative implications on heating, reliability, and battery life are obvious.

More Savings Are Possible

Some systems use a means of power savings known as partial power down. In partial power-down mode, a system basically shuts off the V_{CC} to some unused circuits during times of inactivity, thus eliminating even low standby currents. All of the members of TI's low-voltage technology (LVT) product line previously mentioned offer a parametric specification I_{off}, which ensures that the output pins of the parts remain in a high-impedance state when the supply voltage is at 0 V. This prevents an inactive LVT device from dragging down the bus of an active part in the system and allows the LVT part to become a partition for the partially powered-down unused subsystem. The LVT device still functions as a level shifter and voltage translator when power is restored to the inactive subsystem.

Another aspect of system power dissipation is the use of passive resistor pullups to keep a local bus from floating and causing damage to the devices on the bus. Pullups were sufficient for the older desktop systems where power consumption was not as much of a concern, but pullup resistors in portable equipment can have a serious impact on battery life, and as such must be addressed.

Products like the 'LVT16245A (and others) from TI have a circuit feature called a bus-hold cell (shown in Figure 6). This cell eliminates these passive components and all of the procurement costs, board space, bus parasitics, and power dissipation associated with them. The bus-hold cell does not load down the bus or add any significant power dissipation to the LVT device.

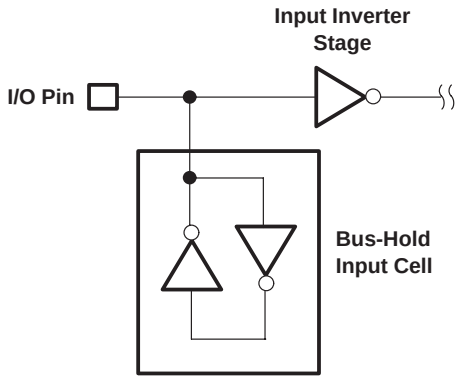


Figure 6. LVT Bus-Hold Cell

Conclusion

Mixed 3.3-V and 5-V systems can be optimized for low power and low cost by the judicious selection of the appropriate voltage-level shifter component. Split-rail level shifters can affect this voltage translation, but selection of this device is burdened with serious design tradeoffs in power sequencing, partial system power down, and system power dissipation. Further savings in both power and component cost can be realized if the component selected has a bus-hold cell or other means of eliminating passive system components.

Acknowledgment

The author of this document is Mark McClear.