ABT
Advanced BiCMOS Technology Characterization Information

SCBA008B
June 1997

TEXAS INSTRUMENTS

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Introduction

The purpose of this document is to assist the designers of high-performance digital logic systems in using the advanced BiCMOS technology (ABT) logic family.

Detailed electrical characteristics of these bus-interface devices are provided and tables and graphs have been included to compare specific parameters of the ABT family with those of other logic families.

In addition, typical data is provided to give the hardware designer a better understanding of how the ABT devices operate under various conditions.

The major subject areas covered in the report are as follows:

- AC Performance
- Power Considerations
- Input Characteristics
- Output Characteristics
- Signal Integrity
- Advanced Packaging
- Characterization Information

The characterization information provided is typical data and is not intended to be used as minimum or maximum specifications, unless noted as such.

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AC Performance

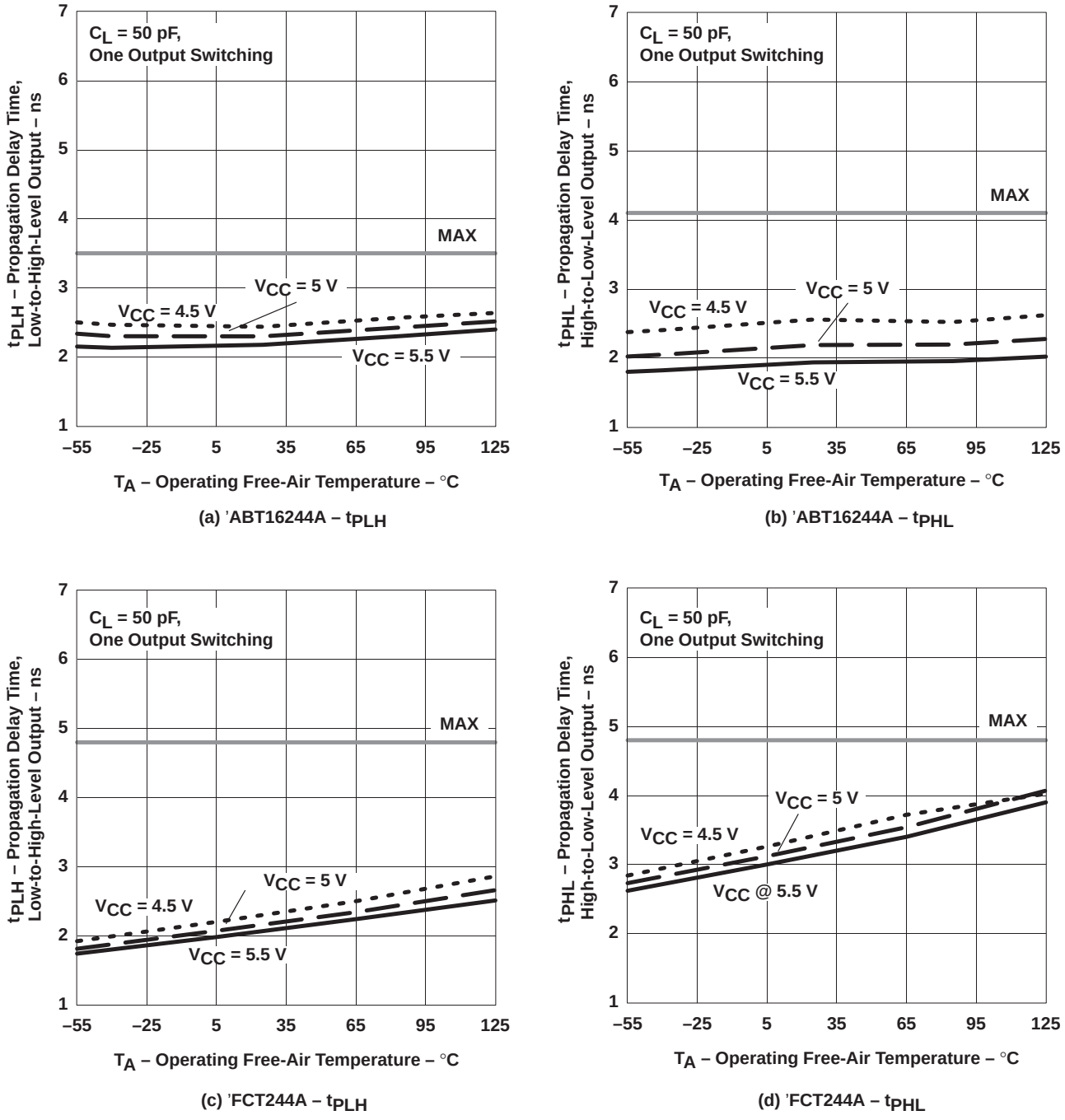
As microprocessor operating frequencies increase, the period of time allotted for operations, such as memory access or arithmetic functions, decreases. With this in mind, TI developed a family of bus-interface devices – ABT – utilizing advanced BiCMOS technology. The goal of the ABT family of devices is to give system designers one bus-interface solution that provides high drive capability, good signal integrity, and propagation delays short enough to appear transparent with respect to overall system performance.

Advances in IC process technology, including smaller minimum feature size, tighter metal pitch, and shallower junctions, combine to provide stronger drive strengths and smaller parasitic capacitances. As a result, internal propagation delays have become extremely short. With the advent of the 0.8-μm, EPIC-IIB™ BiCMOS process and new circuit innovations, the ABT family offers typical propagation delays as low as 2-3 ns as shown in Figure 1. Maximum specifications are as low as 3–5 ns, depending on the device type.

Figure 2 shows the propagation delay versus change in both temperature and supply voltage for an ’ABT16244A, ’FCT244A, and a ’F244 device. The graphs highlight two important aspects of the ABT logic family. First, ABT interface devices have extremely short propagation delay times. The figures clearly show the improvement in speed of an ABT device over that of a 74F and 74FCTA device. Second, the variance in speed with respect to both temperature and supply voltage is minimal for ABT. At low temperatures, the increase in CMOS performance compensates for the decrease in bipolar device strength. At high temperatures, the reverse occurs. This complementary performance of both CMOS and bipolar devices on a single chip results in a slope that is virtually flat across the entire temperature range of –55°C to 125°C.

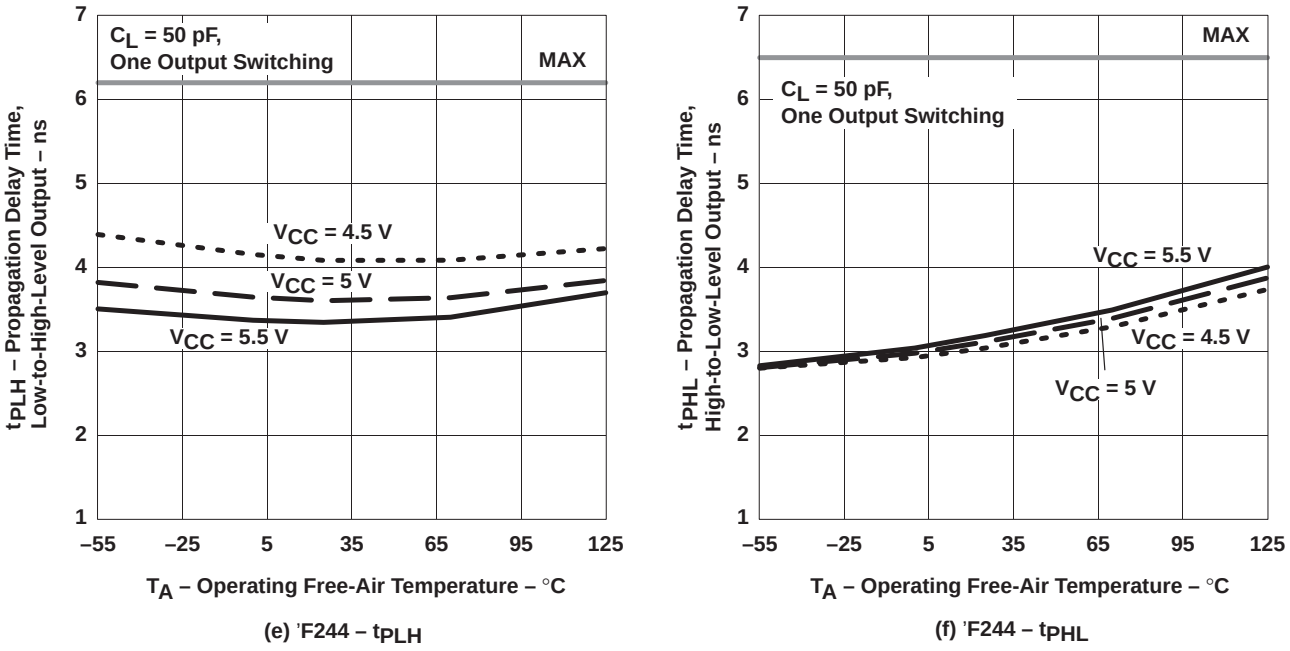
For most applications, the data sheet specifications may not provide all of the information a designer would like to see for a particular device. For instance, a designer might benefit from data such as propagation delay with multiple outputs switching or with various loads. This type of data is extremely difficult to test using automatic test equipment; therefore, it is provided in this document as family characteristics shown in Figure 2 and Figure 3.

To get a clear picture of where ABT stands in reference to other logic families, data is shown for a comparable (same function) 74F and 74FCTA device. It is clear that ABT is the designer's best choice for bus-interface applications that require consistent speed performance over various conditions.



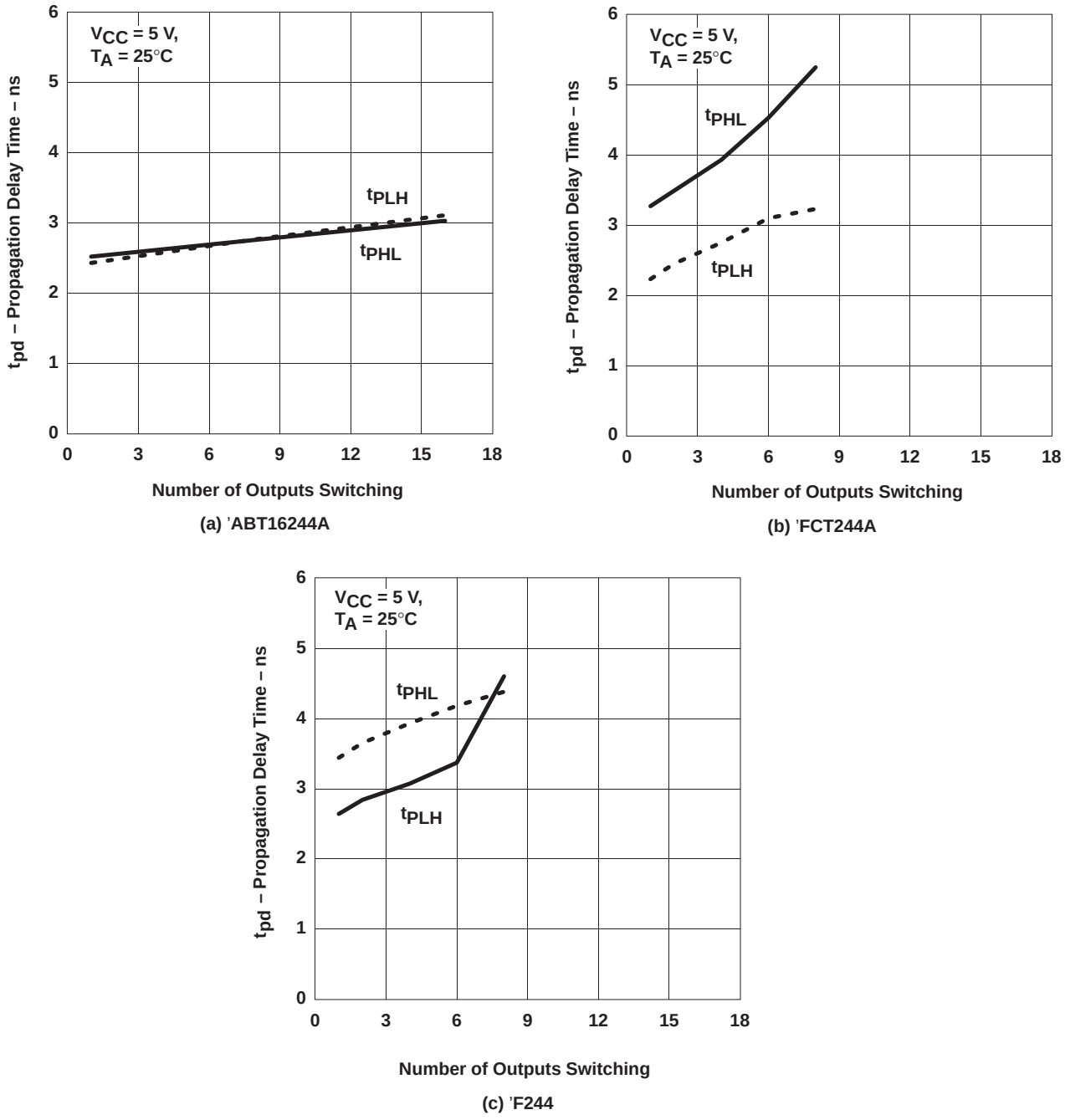
NOTE: MAX is data sheet specification

Figure 1. Propagation Delay vs Operating Free-Air Temperature A to Y



NOTE: MAX is data sheet specification.

Figure 1. Propagation Delay vs Operating Free-Air Temperature A to Y (Continued)

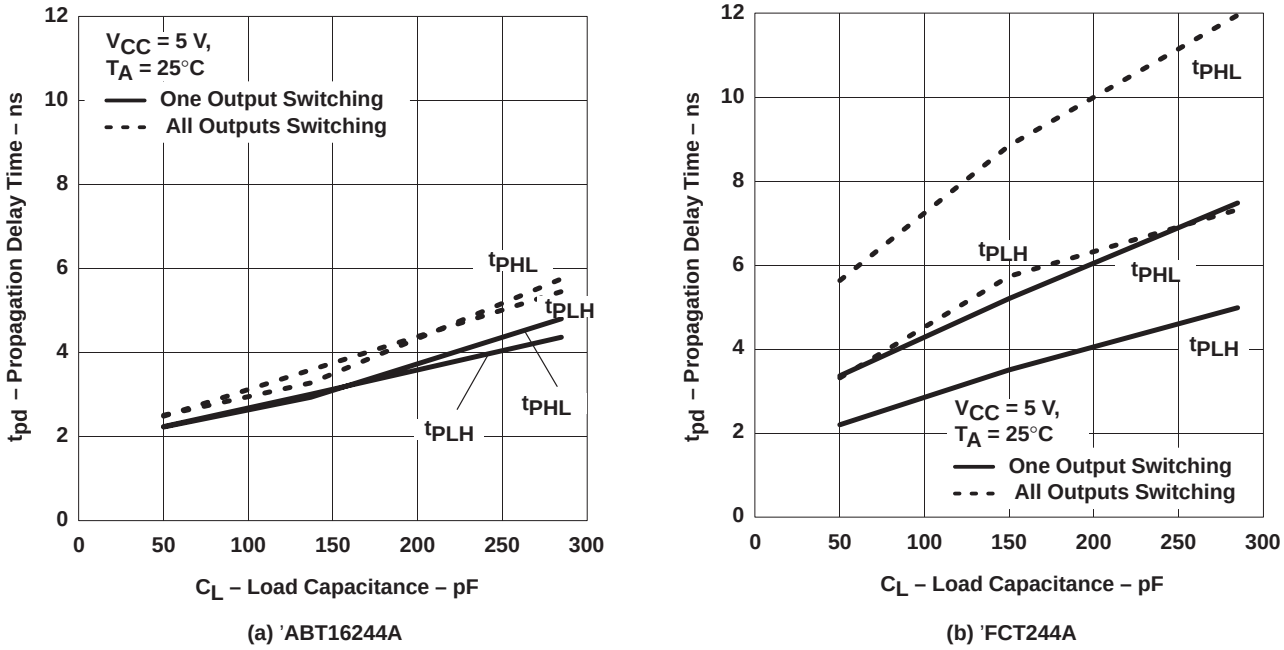


(a) 'ABT16244A

(b) 'FCT244A

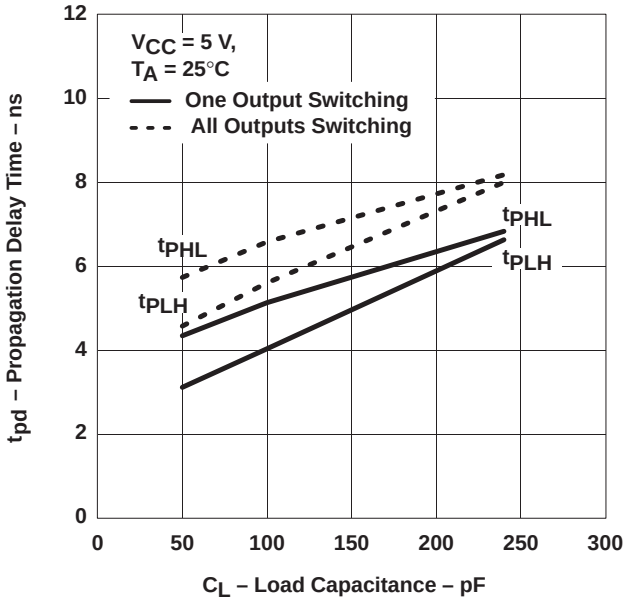
(c) 'F244

Figure 2. Propagation Delay Time vs Number of Outputs Switching



(a) 'ABT16244A

(b) 'FCT244A



(c) 'F244

Figure 3. Propagation Delay vs Capacitive Load

Power Considerations

With the challenge to make systems more dense while improving performance comes the need to replace power-hungry devices without compromising speed. The ABT family of drivers provides a solution with low CMOS power consumption and high-speed bipolar technology on a single device.

There are two basic things to consider when calculating power consumption, static (dc) power, and dynamic power. Static power is calculated using the value of I_{CC} as shown in the data sheet. This is a dc value with no load on the outputs. To understand the relationship between pure CMOS, pure bipolar, and advanced BiCMOS for dc power rating, see Table 1, which shows the various data sheet values. The bipolar device shows the highest I_{CC} values, with little relief, regardless of the state of the outputs. This is not the case with ABT octals, which offer the low static power consumption of CMOS while in the high-impedance state, or when the outputs are high (I_{CCZ}, I_{CCH}).

Table 1. Supply Current

PARAMETER	TEST CONDITIONS		'F244		'FCT244		SN74ABT244	
			MIN	MAX	MIN	MAX	MIN	MAX
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		60 mA				250 µA
		Outputs low		90 mA				30 mA
		Outputs disabled		90 mA				250 µA
	V_{CC} = maximum, V ≥ V_{CC} – 0.2 V, V ≤ V_{CC} – 0.2 V					1.5 mA		

Dynamic power involves the charging and discharging of internal capacitances, as well as the external load capacitance. It is this dynamic component that makes up the majority of the total power dissipation. Figure 4 shows power as a function of frequency for ABT, FCT, and F devices. Although bipolar devices tend to have extremely high static power, there is a point on the frequency curve, commonly referred to as the crossover point, where the CMOS device no longer consumes less power. With ABT devices, the power increase at higher frequencies is less than that of the pure CMOS FCT.

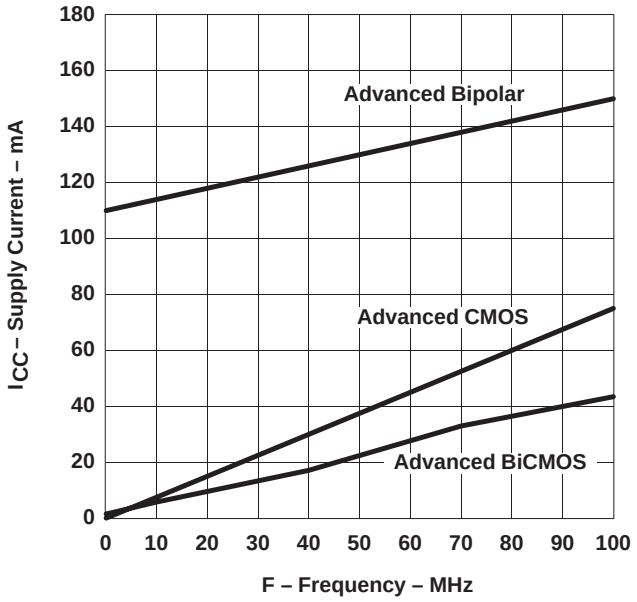


Figure 4. Supply Current vs Frequency

The use of bipolar transistors in the output stage is advantageous in two ways. First, the voltage swing is less than with a CMOS output, reducing the power consumed when charging or discharging the external load. Second, bipolar transistors are capable of turning off more efficiently than CMOS transistors, thus reducing the flow of current from V_{CC} to GND. Combined, these features allow for better power performance at high frequencies.

Input Characteristics

ABT bus-interface devices are designed to ensure TTL-compatible input levels switching between 0.8 V and 2 V (typically 1.5 V). Additionally, these inputs are implemented with CMOS circuitry, resulting in high impedance (low leakage) and low capacitance, which reduces overall bus loading. This section is an overview of the circuitry utilized for a typical ABT input, the corresponding electrical characteristics, and guidelines for proper termination of unused inputs.

ABT Input Circuitry

Figure 5 shows a typical ABT input schematic. A pure CMOS-input threshold is normally set at one-half of V_{CC}. To shift the threshold voltage to be centered around 1.5 V (see Figure 6), the supply voltage of the input stage is dropped by the diode, D1, and the transistor, Q1. Reducing the voltage at the source of Q_p enables it to turn off more efficiently when flow is from V_{CC} to GND (ΔI_{CC}). When the input is in the low state, Q_r raises the voltage of the source of Q_p to V_{CC} to ensure proper operation of the following stage. This feedback circuit provides approximately 100 mV of input hysteresis, which increases the noise margin and helps ensure the device is free from oscillations when operated within specified input ramp rates.

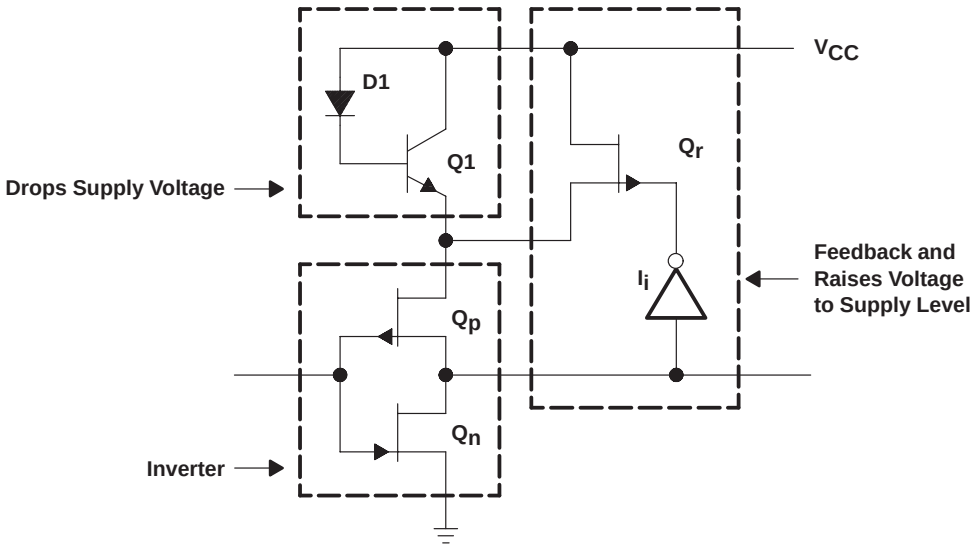


Figure 5. Simplified Input Stage of an ABT Circuit

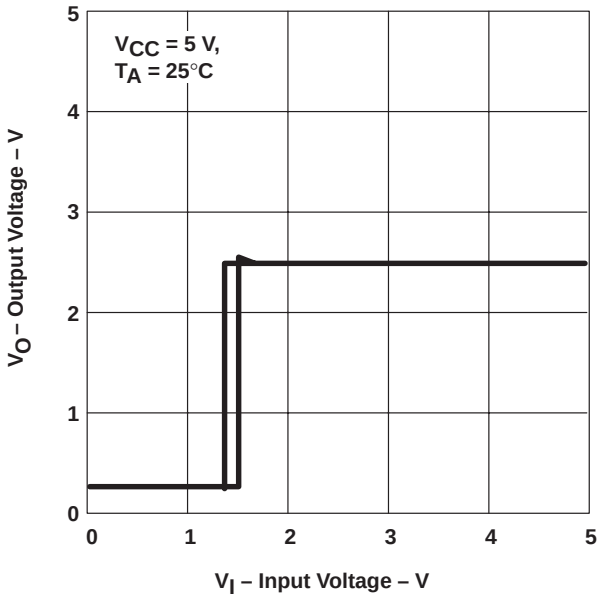


Figure 6. Output Voltage vs Input Voltage

Input Current Loading

The utilization of submicron (0.8-µm) CMOS technology for the input stage of ABT devices causes minimal loading of the system bus due to low leakage currents and low capacitance. The small geometries of the EPIC-IIB process have resulted in capacitances as low as 3 pF for inputs and 8 pF for C_{io} of a transceiver. Figure 7 and Table 2 indicate the low input current performance and specifications. Considering this low capacitance along with the negligible input current, systems designers can decrease their overall bus loading.

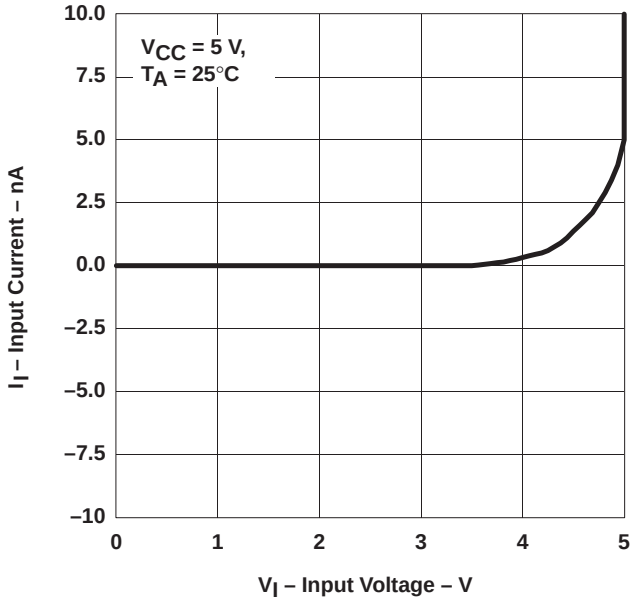


Figure 7. Input Current vs Input Voltage

Table 2. Input Current Specifications

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT245		SN74ABT245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±1		±1		±1	µA
I_{OZH}†	V_{CC} = 5.5 V,	V_O = 2.7 V			50		50		50	µA
I_{OZL}†	V_{CC} = 5.5 V,	V_O = 0.5 V			–50		–50		–50	µA

† The parameters I_{OZH} and I_{OZL} include the input leakage current.

Supply Current Change (ΔI_{CC})

Because ABT devices utilize a CMOS-input stage but operate in a TTL-level signal environment, there is a current specification unique to this set of conditions known as ΔI_{CC}. Given a CMOS inverter with the input voltage set so that both the p and n channel devices are on, current flows from V_{CC} to GND. This can occur when the input to an ABT device is at a valid high level (>2 V), which turns on the n-channel, but not high enough to completely turn off the p-channel device. The current that flows under these conditions is specified in the data sheet (ΔI_{CC}) and is measured one input at a time with the input voltage set at 3.4 V. Figure 8 shows the change in I_{CC} as the input is ramped from 0 V to 5 V. For ABT non-storage devices, a feature is added that turns off the input when the outputs are disabled to reduce power consumption (see Table 3 for an example. Refer to individual data sheets for this specification).

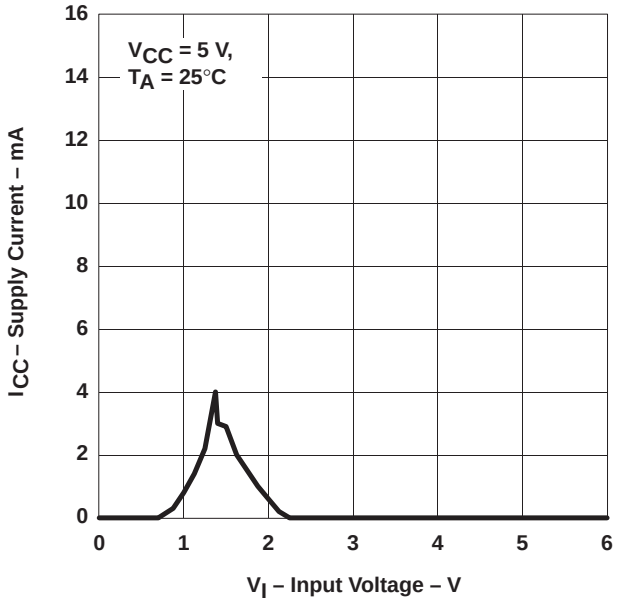


Figure 8. Supply Current vs Input Voltage

Table 3. Supply Current Change (ΔI_{CC})

PARAMETER	TEST CONDITIONS		T_A = 25°C		SN54ABT244		SN74ABT244		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
ΔI_{CC}†	V_I = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled		1.5		1.5		1.5	mA
		Outputs disabled		50		50		50	µA

† This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Proper Termination of Unused Inputs

With advancements in speed, logic devices have become more sensitive to slow input edge rates. A slow input edge rate, coupled with the noise generated on the power rails when the output switches, can cause excessive output glitching or, in some cases, oscillations. Similar situations can occur if an unused input is left floating or not being actively held at a valid logic level.

These problems are due to voltage transients induced on the device's power system as the output load current (I_O) flows through the parasitic lead inductances during switching (see Figure 9). Since the device's internal power-supply nodes are used as voltage references throughout the integrated circuit, the inductive voltage spikes (V_{gnd}) affect the way signals appear to the internal gate structures. For instance, as the voltage at the device's ground node rises, the input signal (V_i') appears to decrease in magnitude. This undesirable phenomena can erroneously change the output's transition if a threshold violation takes place.

In the case of a slowly rising input edge, if the ground movement is large enough, the apparent signal, V_i', at the device appears to be driven back through the threshold and the output starts to switch in the opposite direction. If worst-case conditions prevail (simultaneously switching all of the outputs with large transient load currents) the slow input edge is repeatedly driven back through the threshold, resulting in output oscillation.

ABT devices are recommended to have input edge rates faster than 5 ns/V for standard parts, and 10 ns/V for the Widebus™ series of products when the outputs are enabled. A critical area for this edge rate is in the transition region between 1 V and 2 V. It is also recommended to hold inputs or I/O pins at a valid logic high or low when they are not being used or when the part driving them is in the high-impedance state.

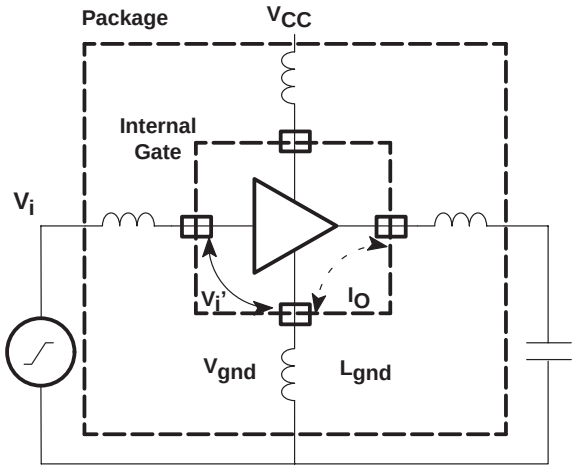


Figure 9. Sample Input/Output Model

Output Characteristics

The current trend is consolidation of the functionality of multiple logic devices into complex, high pin-count ASICs and programmables. There are a number of important advantages for utilizing bus-interface devices in standard high-volume packages. These include the need for high drive capability and good signal integrity. The use of bipolar circuitry in the output stage makes it possible to provide these requirements, along with increased speed, using the ABT family.

Figure 10 shows a simplified schematic of an ABT output stage. Data is transmitted to the gate of M1, which acts as a simple current switch. When M1 is turned on, current flows through R1 and M1 to the base of Q4, turning it on and driving the output low. At the same time, the base of Q2 is pulled low, thus turning off the upper output. For a low-to-high transition, the gate of M1 must be driven low, turning M1 off. Current through R1 charges the base of Q2, pulling it high and turning on the Darlington pair, consisting of Q2 and Q3. Meanwhile, with its supply of base drive cut off, Q4 turns off, and the output switches from low to high. R2 is used to limit output current in the high state, and D1 is a blocking diode used to prevent reverse current flow in specific power-down applications.

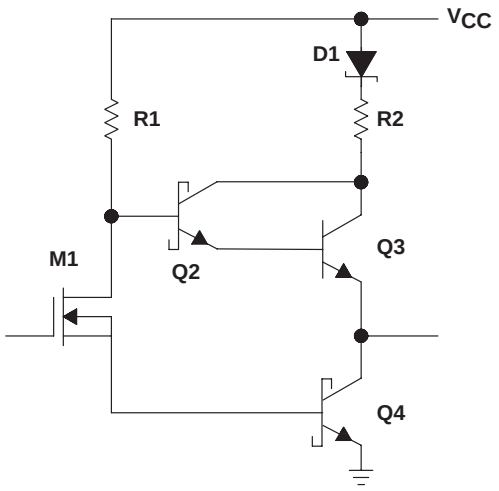


Figure 10. Simplified ABT Output Stage

A clear advantage of using bipolar circuitry in the output stage (as opposed to CMOS) is the reduced voltage swing. This helps to lower ground noise and reduce power consumption. Refer to *Signal Integrity* and *Power Considerations* in this document for further information.

Output Drive

The I_{OH} and I_{OL} curves for a typical ABT output are shown in Figure 11. With a specified I_{OL} of 64 mA and I_{OH} of –32 mA, ABT accommodates many standard backplane specifications. However, these devices are capable of driving well beyond these limits. This is important when considering switching a low-impedance backplane on the incident wave.

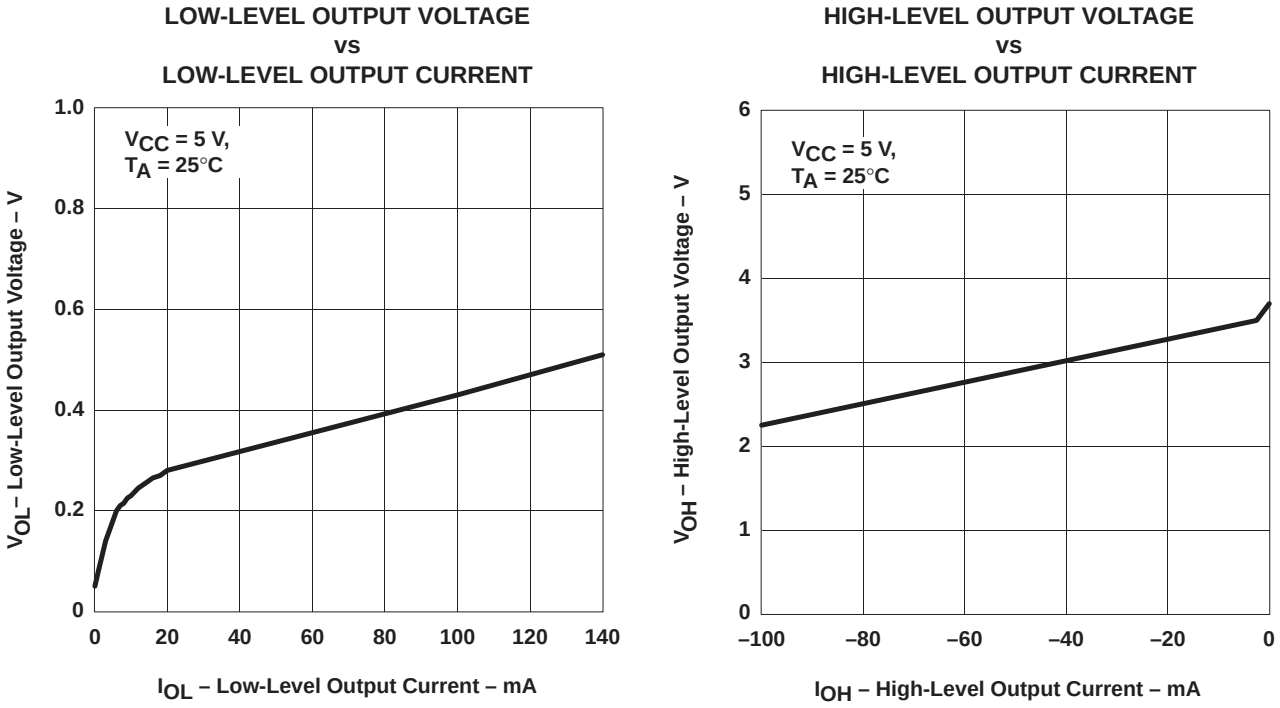


Figure 11. Typical ABT Output Characteristics

Incident-wave switching ensures that for a given transition (either high-to-low or low-to-high) the output reaches a valid V_{IH} or V_{IL} level on the initial wave front (i.e., does not require reflections). Figure 12 shows the problems a designer might encounter when a device does not switch on the incident wave. A shelf below $V_{IL(max)}$, signal A, causes the propagation delay to slow by the amount of time it takes for the signal to reach the receiver and reflect back. Signal B shows the case in which there is a shelf in the threshold region. When this happens, the input to the receiver is uncertain and could cause several problems associated with slow input edges, depending on the length of time the shelf remains in this region. A signal as shown in example C does not cause a problem because the shelf does not occur until the necessary V_{IH} level has been attained.

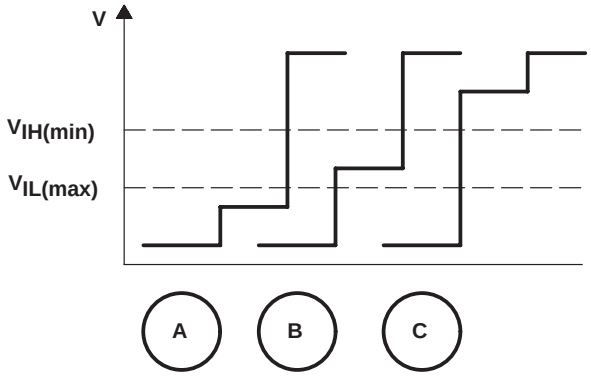


Figure 12. Reflected Wave Switching

Using typical V_{OH} and V_{OL} values along with data points from the curves, ABT devices can typically drive lines in the 25-Ω range on the incident wave.

For a low-to-high transition, (I_{OH} = 85 mA @ V_{OH} = 2.4 V)

$$Z_{LH} = \frac{V_{OH}(min) - V_{OL}(typ)}{I_{OH}} = \frac{2.4\ V - 0.3\ V}{85\ mA} - 25\ \Omega \quad (1)$$

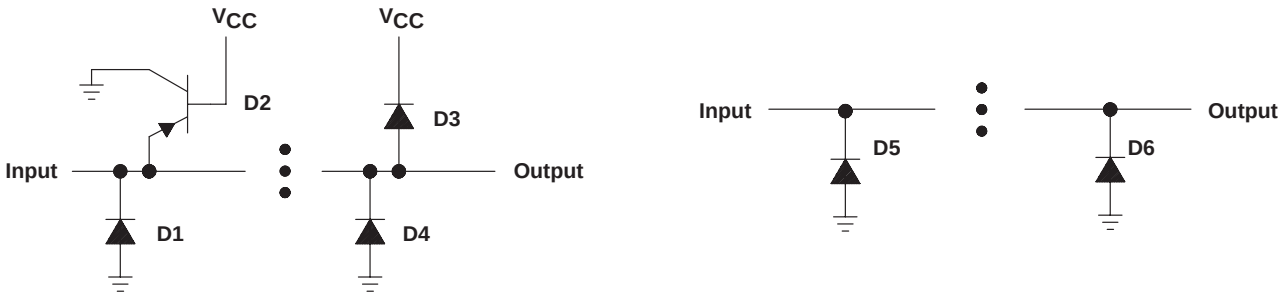
For a high-to-low transition, (I_{OL}= 135 mA @ V_{OL}= 0.5 V)

$$Z_{HL} = \frac{V_{OH}(typ) - V_{OL}(max)}{I_{OL}} = \frac{3.5\ V - 0.5\ V}{135\ mA} - 22\ \Omega \quad (2)$$

Partial Power Down

One application, addressed when designing the ABT family, is partial system power down. When using a standard CMOS device, there is a path from either the input or the output (or both) to V_{CC}. This prevents partial power down for such applications as hot-card insertion without adding current limiting components. This is not the case with ABT as these paths have been eliminated with the use of blocking diodes. Figure 13 shows functionally equivalent schematics of the input structures for CMOS and ABT devices.

Consider the situation shown in Figure 14. The driving device is powered with V_{CC} = 5 V, while the receiving device is powered down (V_{CC} = 0). If these devices are CMOS, the receiver can be powered up through diode D2 when the driver is in a high state. ABT devices do not have a comparable path and are thus immune to this problem, making them more desirable for this application.



(a) CMOS EQUIVALENT INPUT STRUCTURE

(b) ABT EQUIVALENT INPUT STRUCTURE

Figure 13. Simplified Input Structures for CMOS and ABT Devices

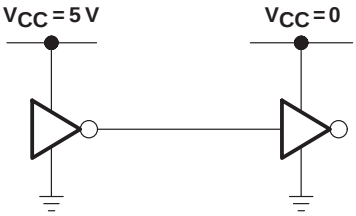


Figure 14. Example of Partial System Power Down

Signal Integrity

A frequent concern of system designers is the performance degradation of ICs when outputs are switched. TI's priority when designing the ABT bus-interface family was to insure signal integrity and eliminate the need for excess settling time of an output waveform. This section addresses the simultaneous switching performance of both the ABT octals and the Widebus functions.

Simultaneous-Switching Phenomenon

Figure 15 shows a simple model of an output pin, including the associated capacitance of the output load and the inherent inductance of the ground lead. The voltage drop across the GND inductor, V_L, is determined by the value of the inductance and the rate of change in current across the inductor. When multiple outputs are switched from high to low, the transient current (di/dt) through the GND inductor generates a difference in potential on the chip ground with respect to the system ground. This induced GND variation can be observed indirectly as shown in Figure 16. The voltage output low peak (V_{OLP}) is measured on one quiet output when all others are switched from high to low.

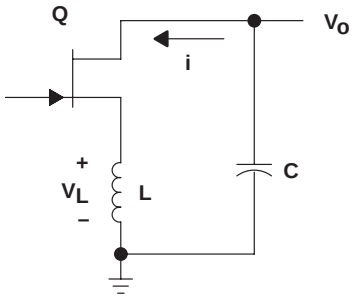
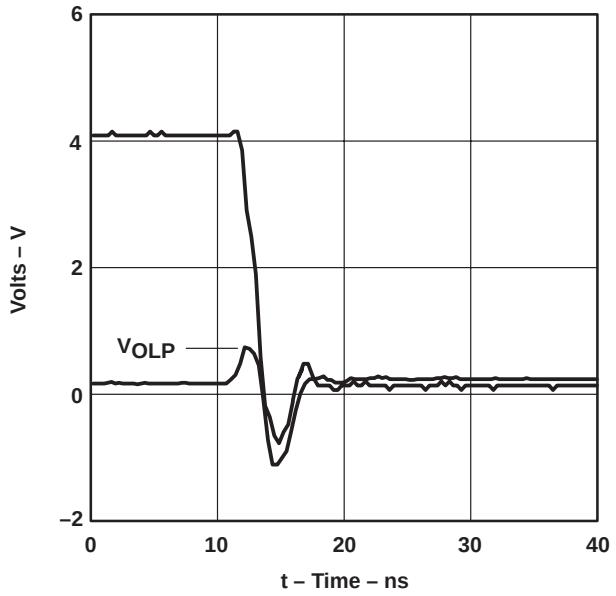


Figure 15. Simultaneous-Switching Output Model



NOTE: V_{OLP} = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs

Figure 16. Simultaneous-Switching-Noise Waveform

A similar phenomena occurs with respect to the V_{CC} plane on a low-to-high transition, known as voltage output high valley (V_{OHV}). Most problems are associated with a large V_{OLP} because the range for a logic 0 is much less than the range for a logic 1, as shown in Figure 17. For a comprehensive discussion of simultaneous switching, see *Simultaneous Switching Evaluation and Testing*, Section 4.1, in the *Advanced CMOS Logic (ACL) Designer's Handbook*, literature number SCAA001B.

The impact of these voltage noise spikes on a system can be extreme. The noise can cause loss of stored data, severe speed degradation, false clocking, and/or reduction in system noise immunity. For an overview of how propagation delay is affected by the switching of multiple outputs, please refer to *ac Performance* in this document.

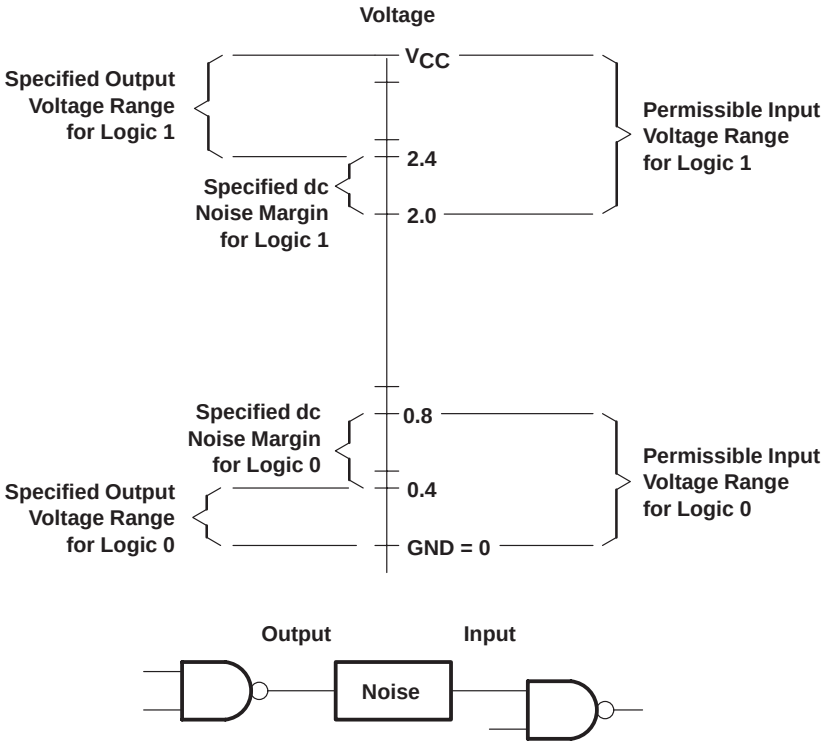


Figure 17. TTL DC Noise Margin

Simultaneous Switching Solutions

Some methods an IC manufacturer can use to reduce the effects of simultaneous switching include: reducing the inductance of the power pins, adding multiple power pins, and controlling the turn on of the output. These techniques are described in the *Advanced CMOS Logic (ACL) Designer's Handbook*, literature number SCAA001B.

Octal ABT devices employ the standard end-pin GND and V_{CC} configuration, while maintaining acceptable simultaneous switching performance, as shown in Figure 18. This is due to the TTL-level output swing (0.3–3 V) and a controlled feedback, which limits the base drive to the lower output.

The ABT Widebus series (16-, 18-, and 20-bit functions) are offered in an SSOP package (see *Packaging* in this document), which TI developed to save valuable board space and reduce simultaneous switching effects. One might expect an increase in noise with 16 outputs switching in a single package; however, the simultaneous switching performance is actually improved. There is a GND pin for every two outputs and a V_{CC} pin for every four. This allows the transient current to be distributed across multiple power pins and decreases the overall d_i/d_t effect. This results in a typical V_{OLP} value on the order of 500 mV for the ABT16500, as shown in Figure 19.

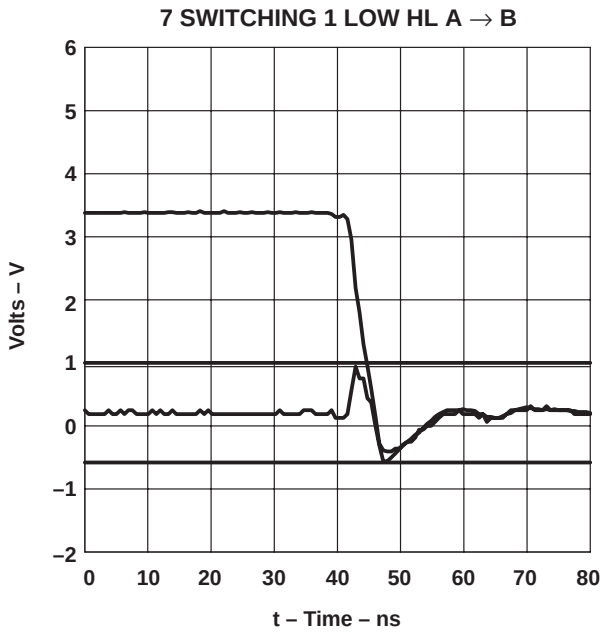


Figure 18. ABT646A Simultaneous-Switching Waveform

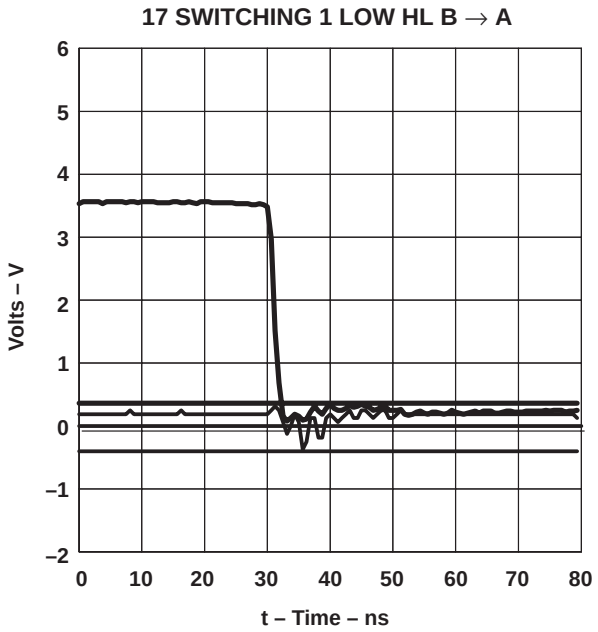


Figure 19. ABT16500B Simultaneous-Switching Waveform

Advanced Packaging

Along with a strong commitment to provide fast, low- power, high-drive ICs, TI is the leader in logic packaging advancements. The development of the shrink small-outline package (SSOP) in 1989 provided system designers the opportunity to reduce the amount of board space required for bus-interface devices by 50%. Several 24-pin solutions including the familiar SOIC, the SSOP, and the TSOP (thin small-outline package) are shown in Figure 20.

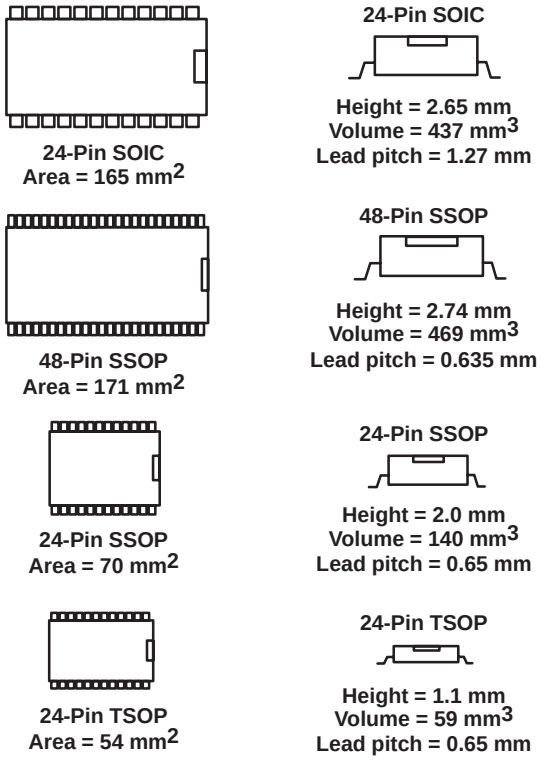


Figure 20. 24-Pin Surface-Mount Comparison

The 48/56-pin SSOP packages allow for twice the functionality (16-, 18-, and 20-bit functions) in approximately the same board area as a standard SOIC. This is accomplished by using a 25-mil (0.635 mm) lead pitch, as opposed to 50-mil (1.27 mm) in SOIC. Figure 21 shows a typical pinout structure for the 48-pin SSOP. The flow-through architecture is standard for all Widebus devices, making signal routing easier during board layout. Also note the distributed GND and V_{CC} pins, which improve simultaneous switching effects as discussed in *Signal Integrity* in this document.

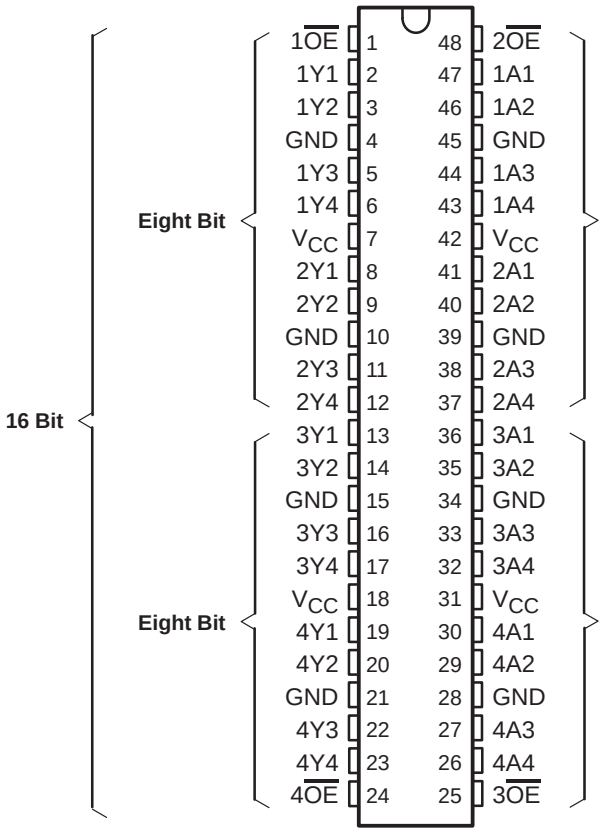


Figure 21. Distributed Pinout of ’ABT16244A

When using the small pin count SSOPs (8-, 9-, and 10-bit functions) the same functionality occupies less than half the board area of a SOIC (70 mm^2 vs 165 mm^2). There also is a height improvement over the SOIC, which is beneficial when the spacing between boards is a consideration. For very dense memory arrays the packaging evolution has been taken one step further with the TSOP. The TSOP thickness of 1.1 mm gives a 58% height improvement over the SOIC.

Table 4 provides a quick reference of the mechanical specifications of the various SSOP packages. For more information, see *Recent Advancements in Bus-Interface Packaging and Processing*, literature number SCZA001A, and *Thin Very Small-Outline Package (TVSOP)*, literature number SCBA009C.

Table 4. SSOP Metric Specifications†

PACKAGE SPECIFICATIONS						PIN SPECIFICATIONS	
PACKAGE TYPE	PINS	INDUSTRY STANDARD	THICKNESS (mm)	BODY WIDTH (mm)	STANDOFF HEIGHT (mm)‡	PIN PITCH (mm)	PIN WIDTH (mm)
SSOP	20	EIAJ	2.00	5.3	0.05	0.650	0.30
SSOP	24	EIAJ	2.00	5.3	0.05	0.650	0.30
SSOP	28	JEDEC	2.59	7.5	0.20	0.635	0.25
SSOP	48	JEDEC	2.59	7.5	0.20	0.635	0.25
SSOP	56	JEDEC	2.59	7.5	0.20	0.635	0.25

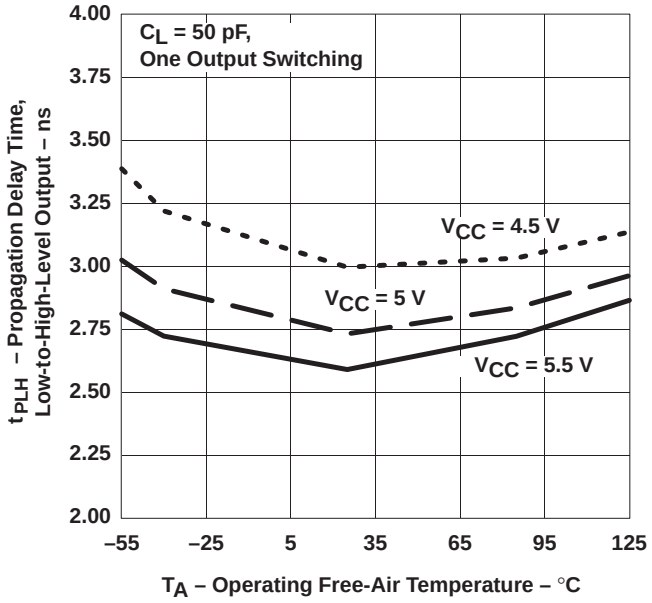
† All values are maximum typical values unless otherwise indicated.
‡ Minimum values

APPENDIX A
’ABT646A Characterization Data

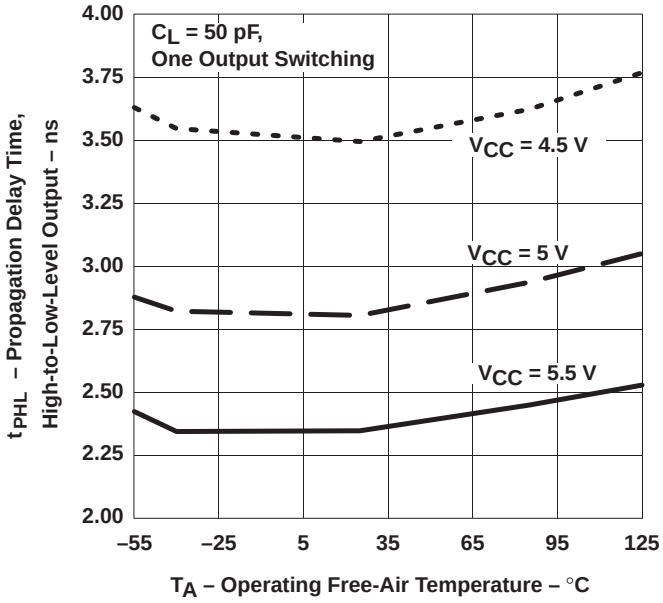
A

Propagation Delay Time vs Temperature

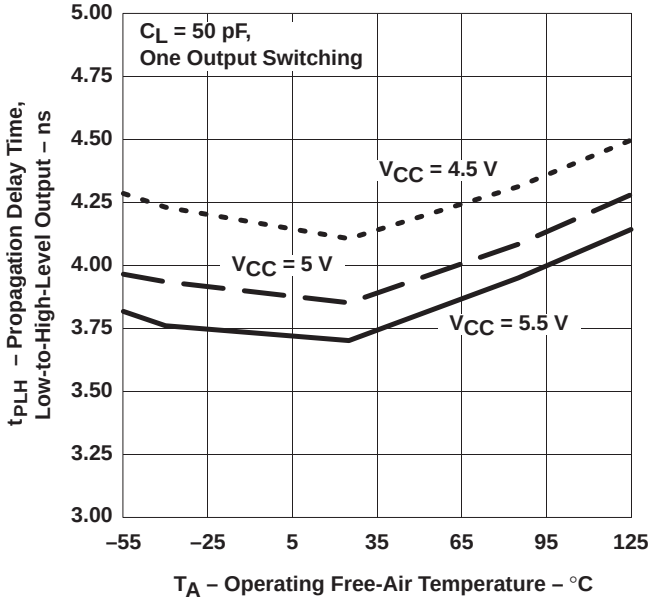
**PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A TO B**



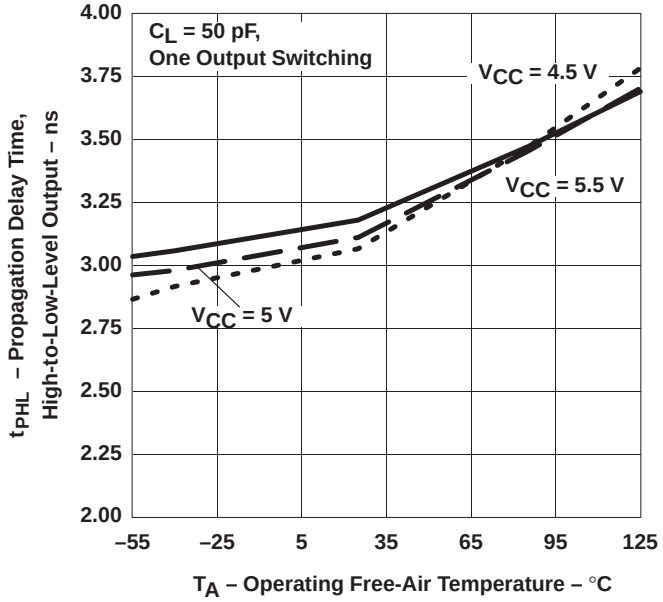
**PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A TO B**



**PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
CLKAB to B**

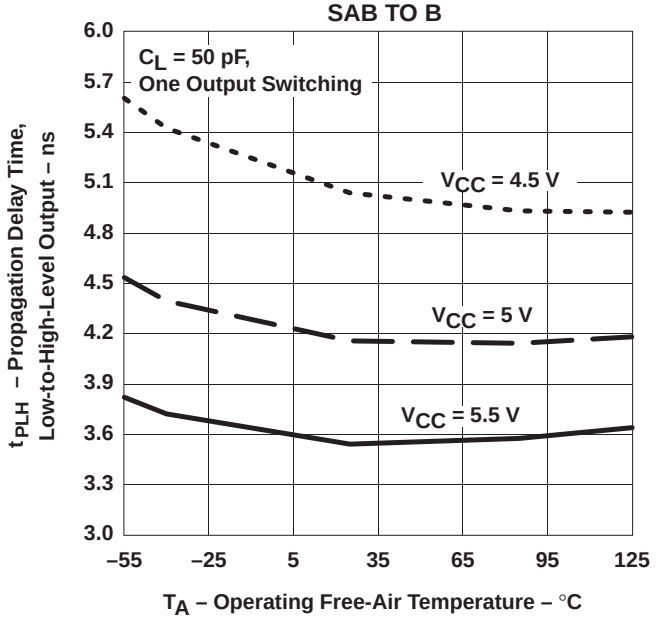


**PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
CLKAB TO B**

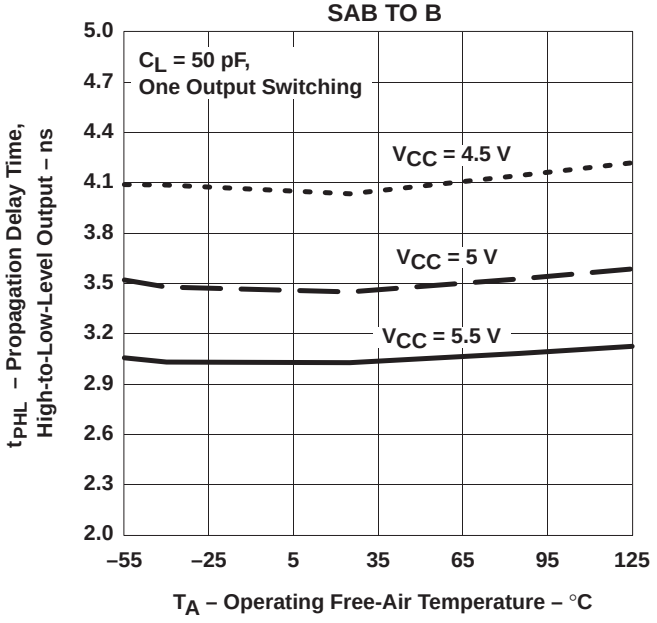


Propagation Delay Time vs Temperature

PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
SAB TO B

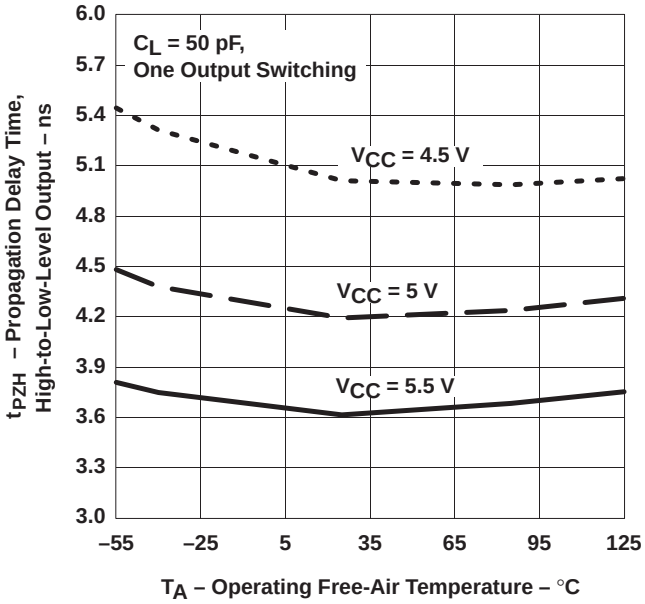


PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
SAB TO B

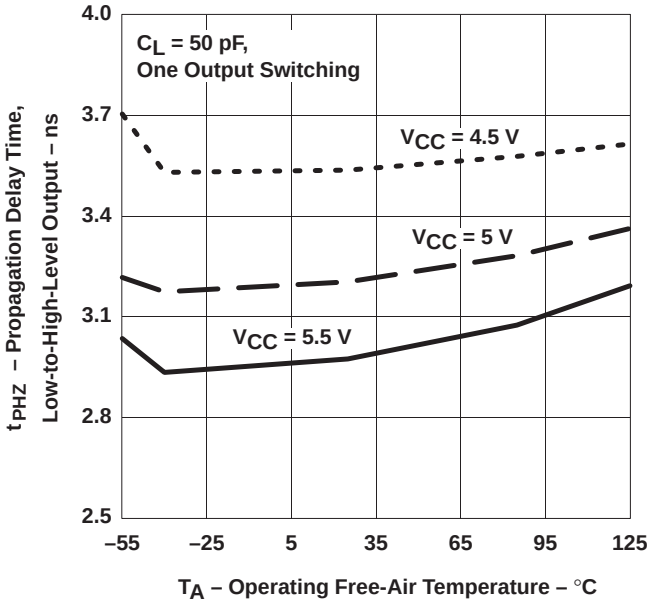


Propagation Delay Time vs Temperature

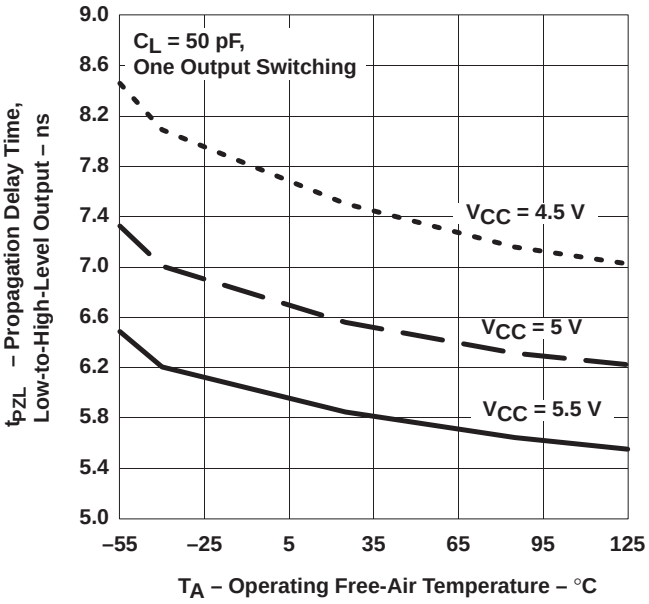
PROPAGATION DELAY TIME
ENABLE-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO B



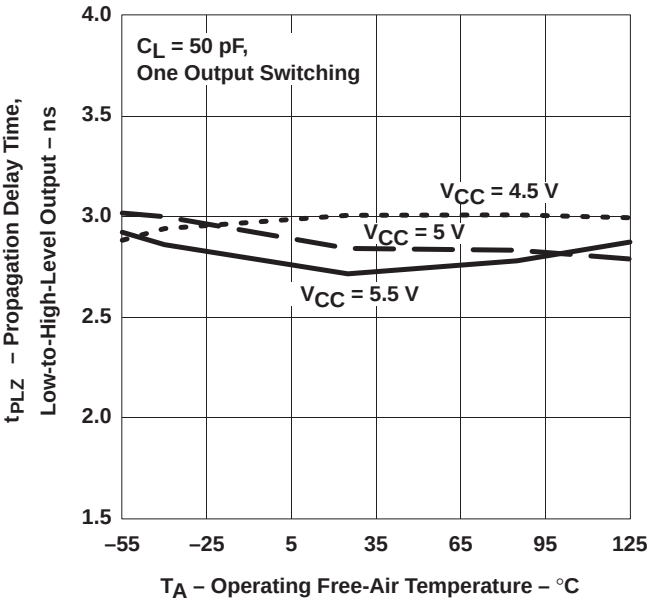
PROPAGATION DELAY TIME
DISABLE-FROM-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO B



PROPAGATION DELAY TIME
ENABLE-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO B

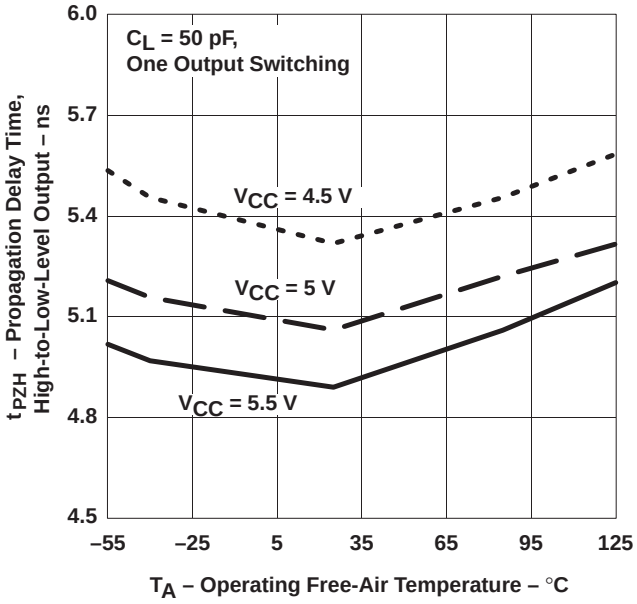


PROPAGATION DELAY TIME
DISABLE-FROM-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO B

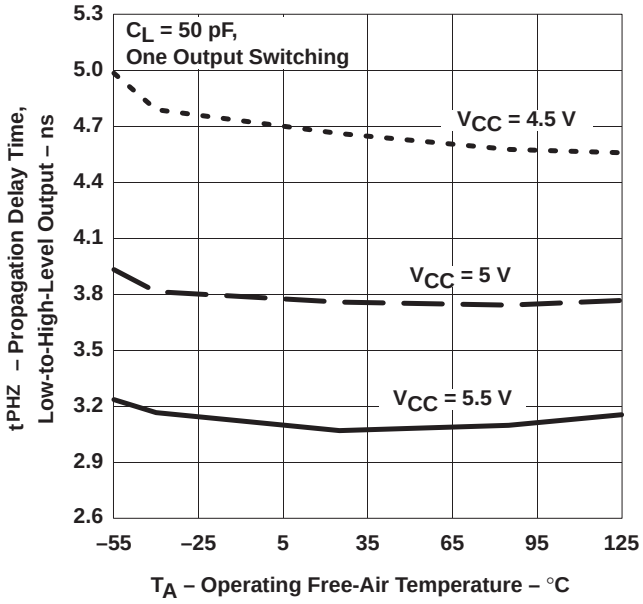


Propagation Delay Time vs Temperature

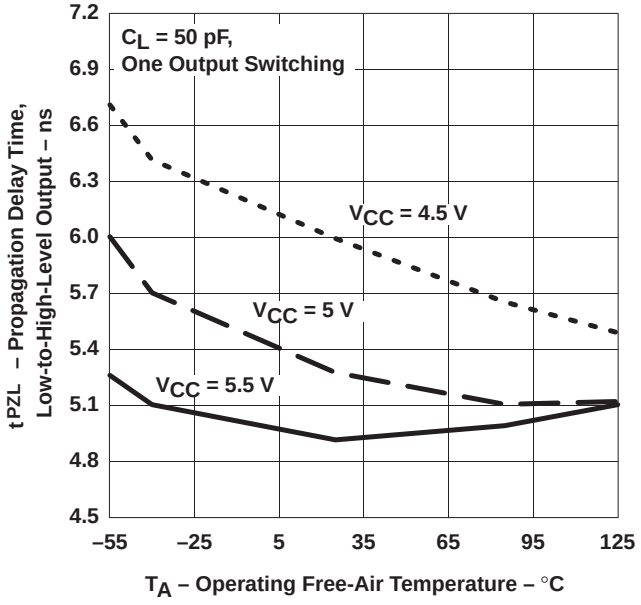
**PROPAGATION DELAY TIME
ENABLE-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
DIR TO B**



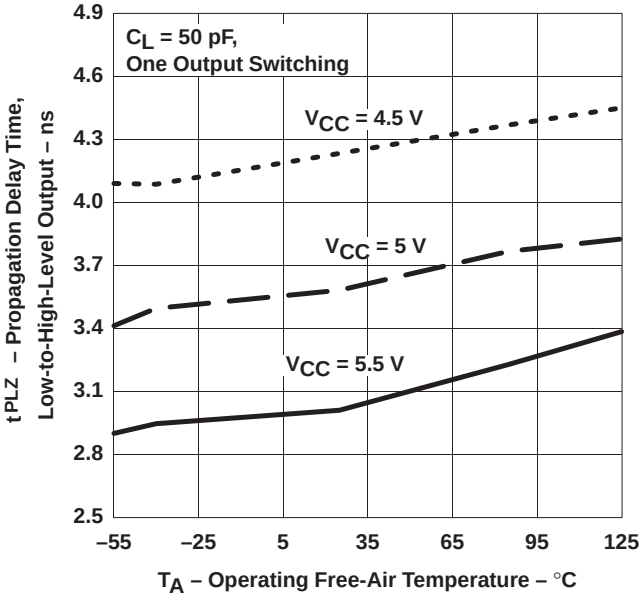
**PROPAGATION DELAY TIME
DISABLE-FROM-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
DIR TO B**



**PROPAGATION DELAY TIME
ENABLE-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
DIR TO B**

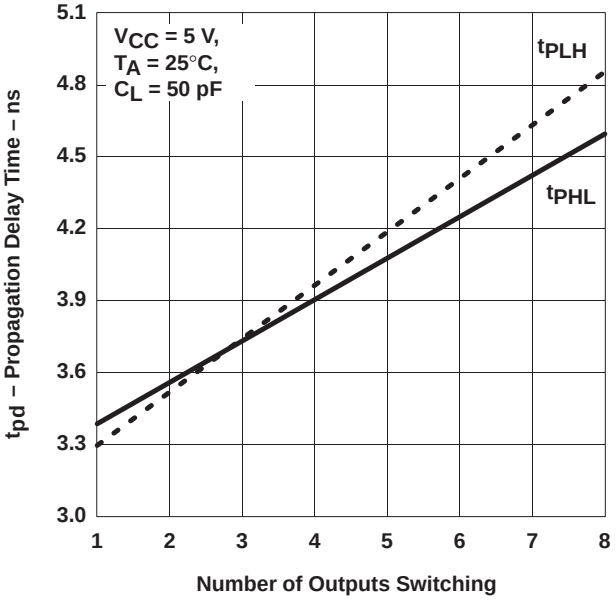


**PROPAGATION DELAY TIME
DISABLE-FROM-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
DIR TO B**

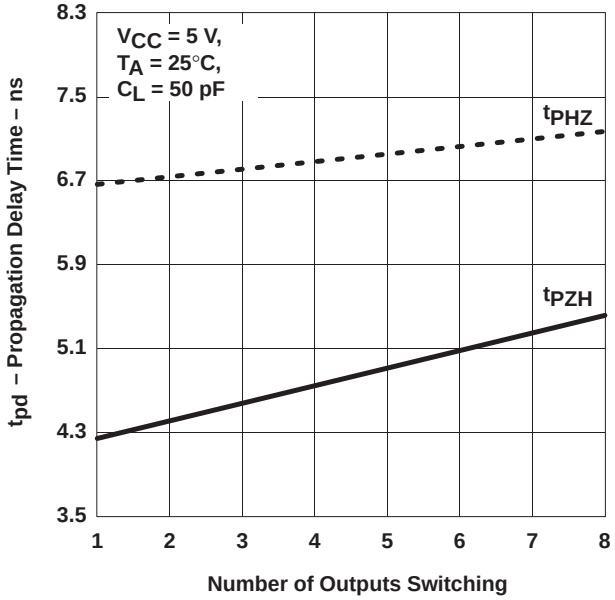


Propagation Delay Time vs Number of Outputs Switching

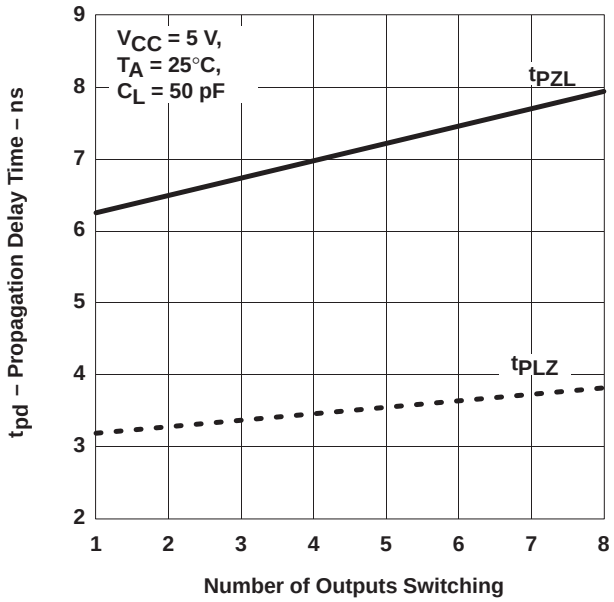
PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING A TO B



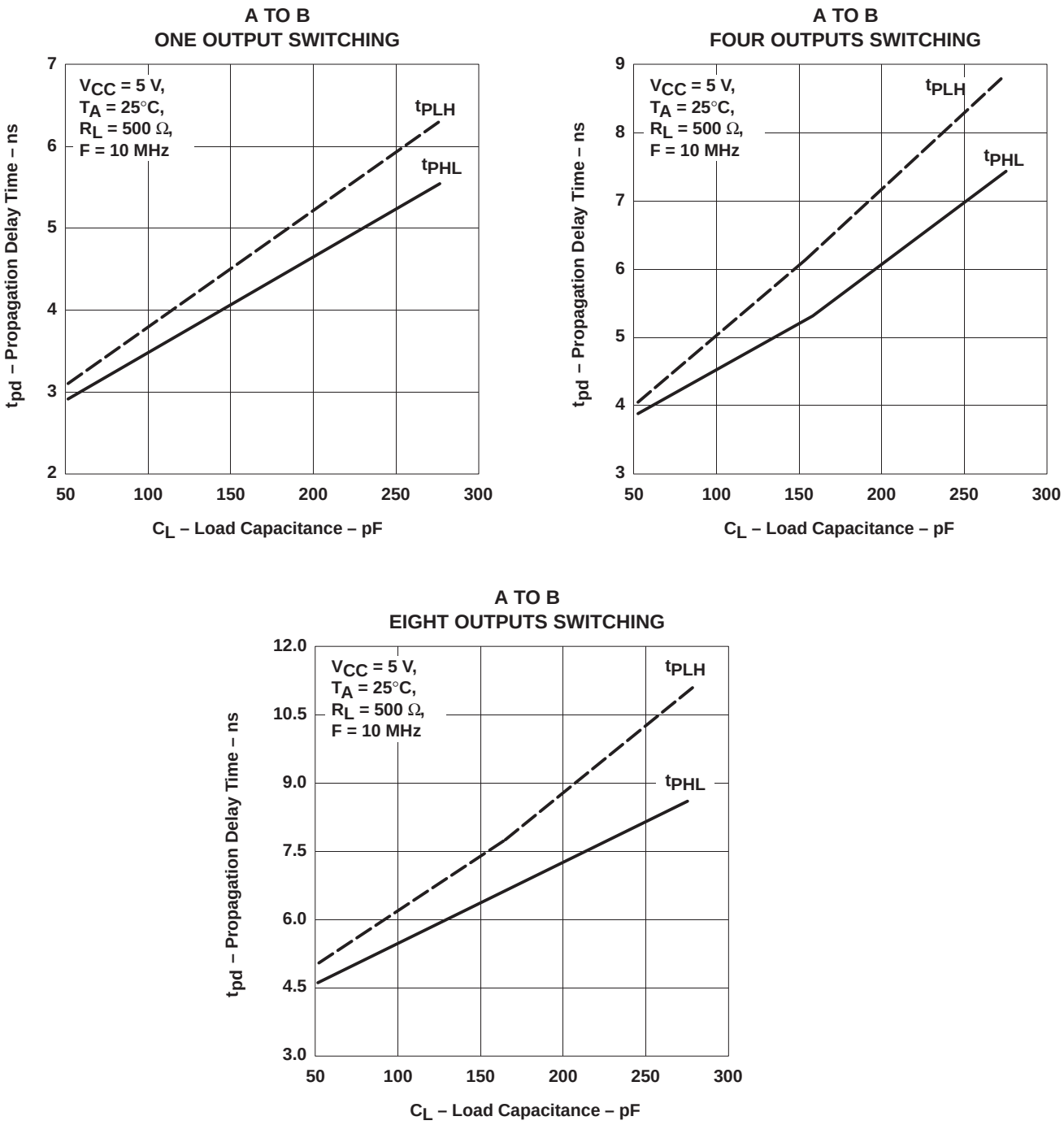
PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING A TO B



PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING A TO B

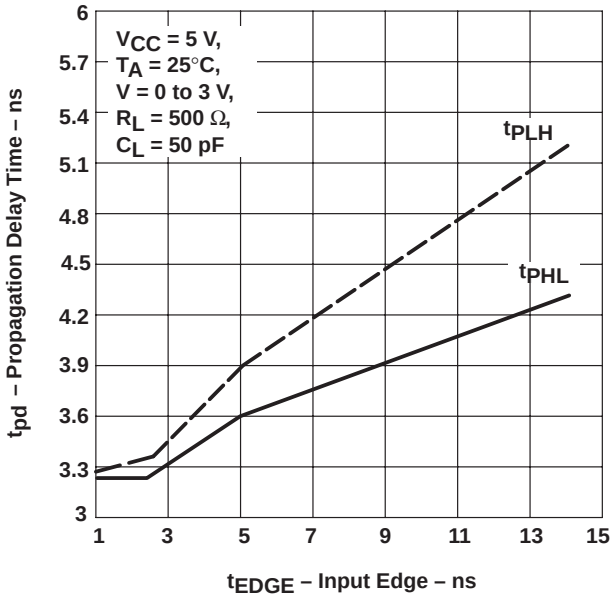


Propagation Delay Time vs Load Capacitance

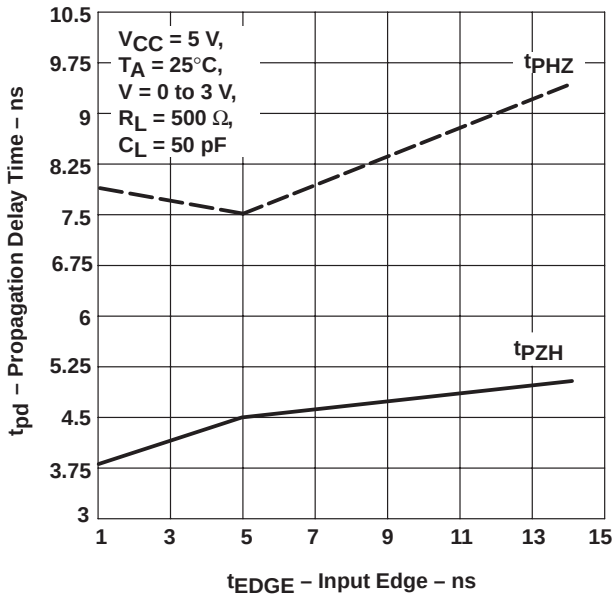


Propagation Delay Time vs Input Edge

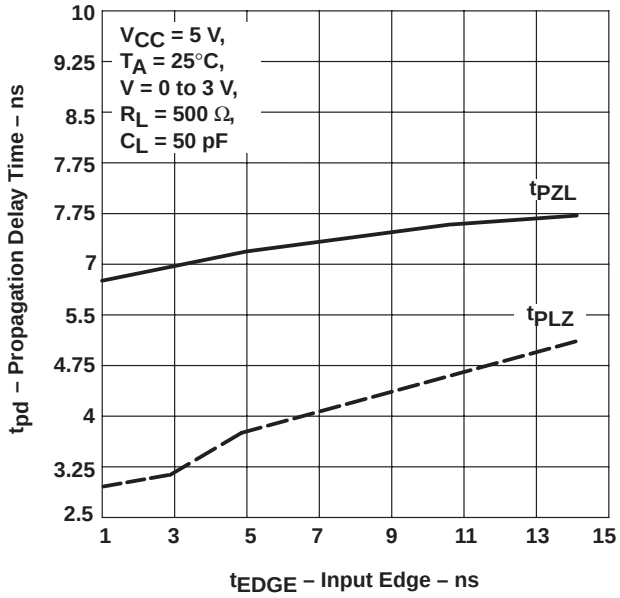
PROPAGATION DELAY TIME vs INPUT EDGE A TO B



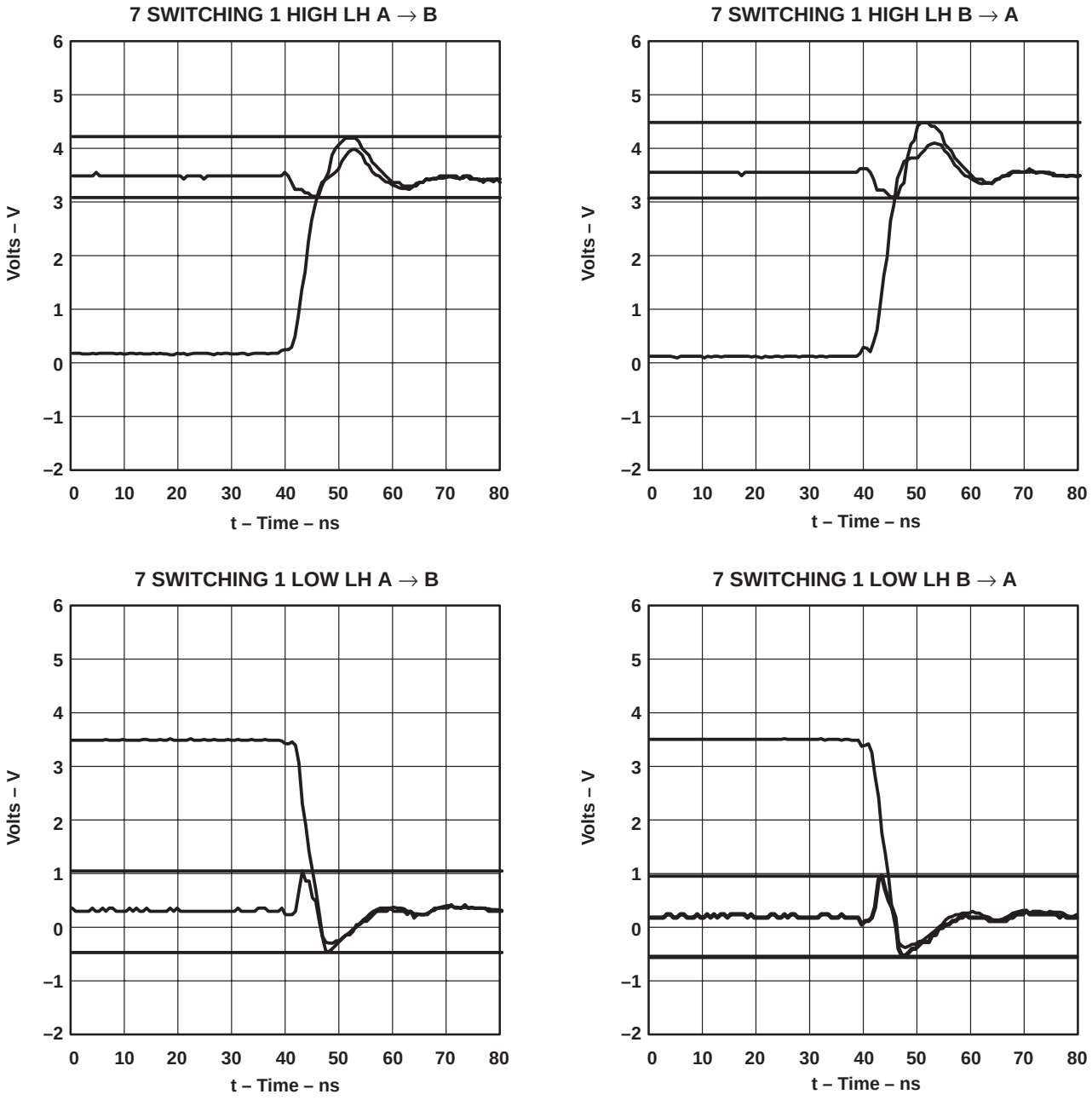
PROPAGATION DELAY TIME vs INPUT EDGE A TO B



PROPAGATION DELAY TIME vs INPUT EDGE A TO B



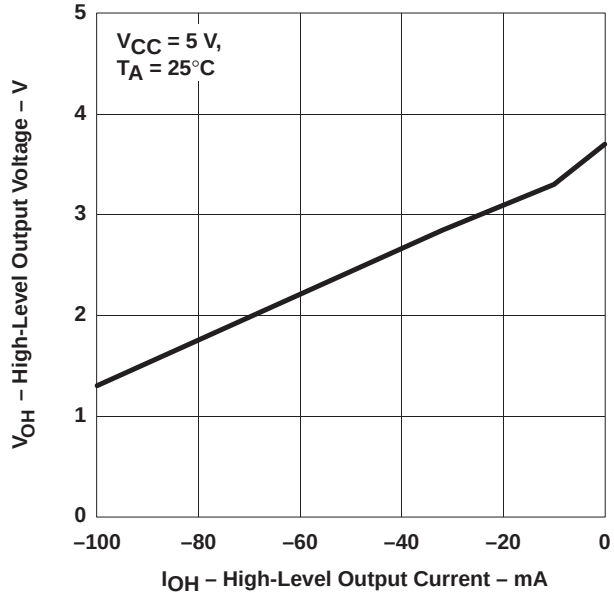
V_{OHV} and V_{OLP}



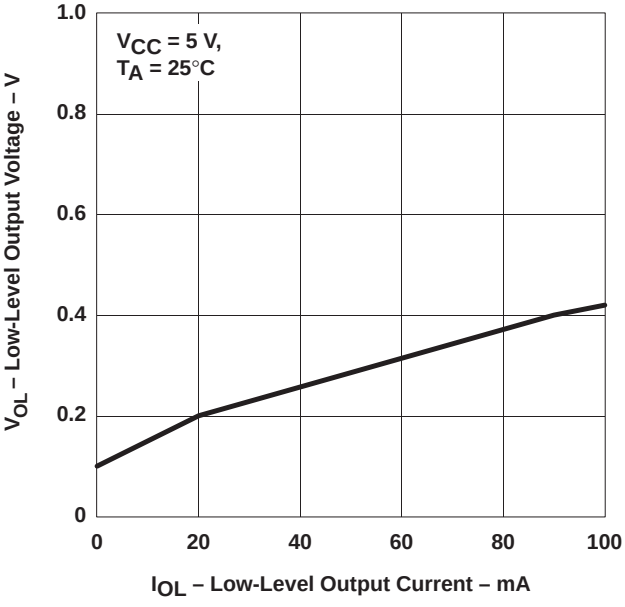
V_{OHV} = Minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs.
V_{OLP} = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.

Typical Characteristics

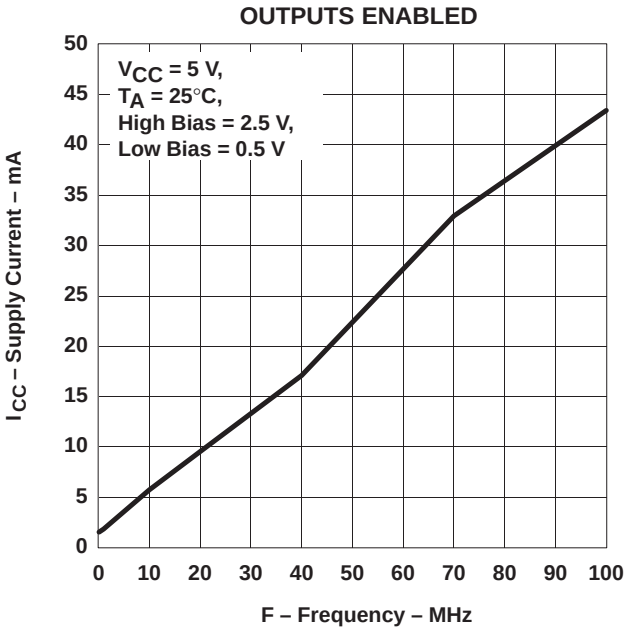
HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

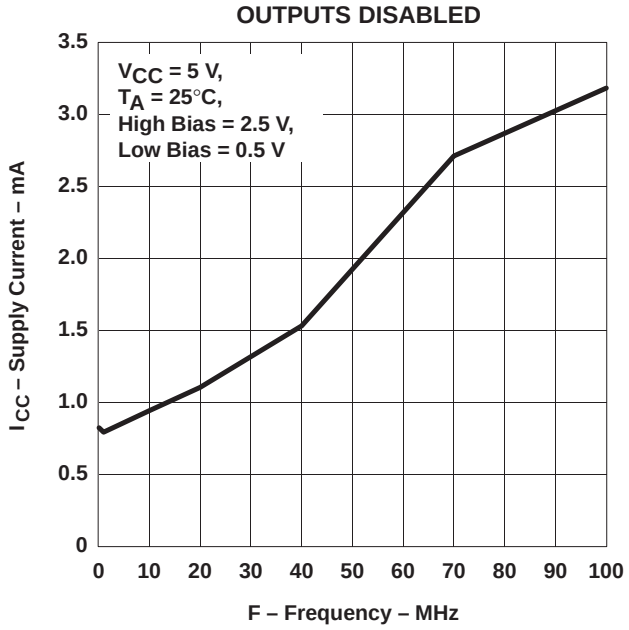


LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT



Supply Current vs Frequency





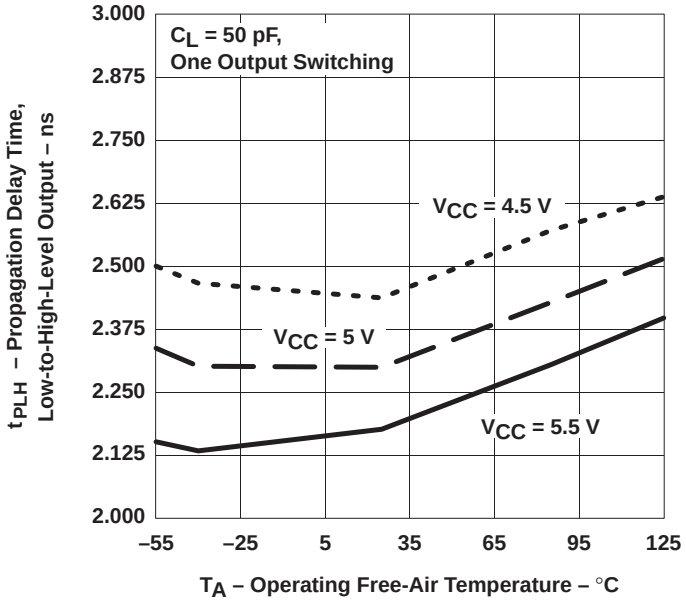
APPENDIX B

SN54ABT16244, SN74ABT16244A Characterization Data

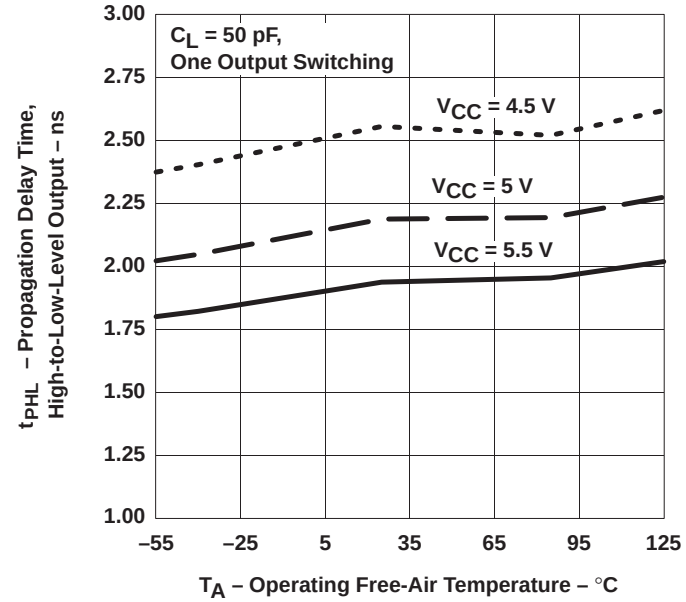
B

Propagation Delay Time vs Temperature

PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A TO Y

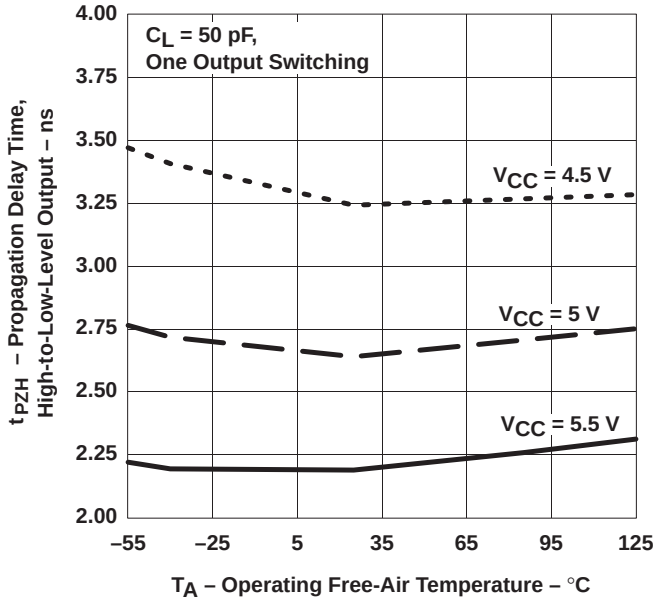


PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A TO Y

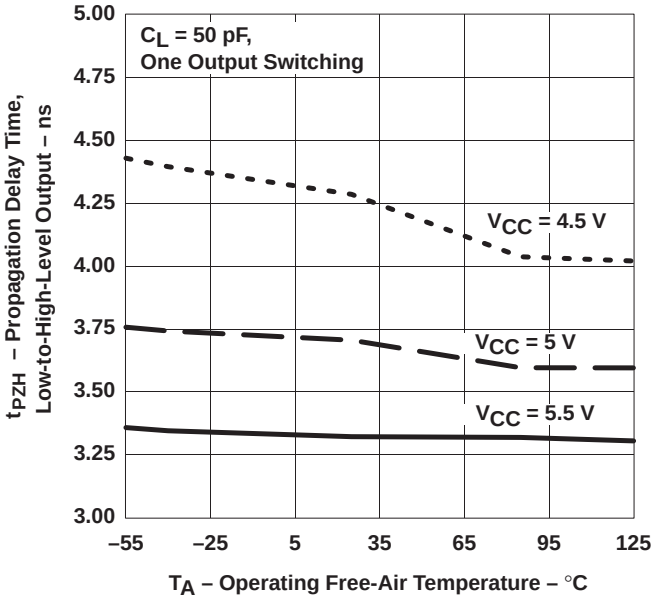


Propagation Delay Time vs Temperature

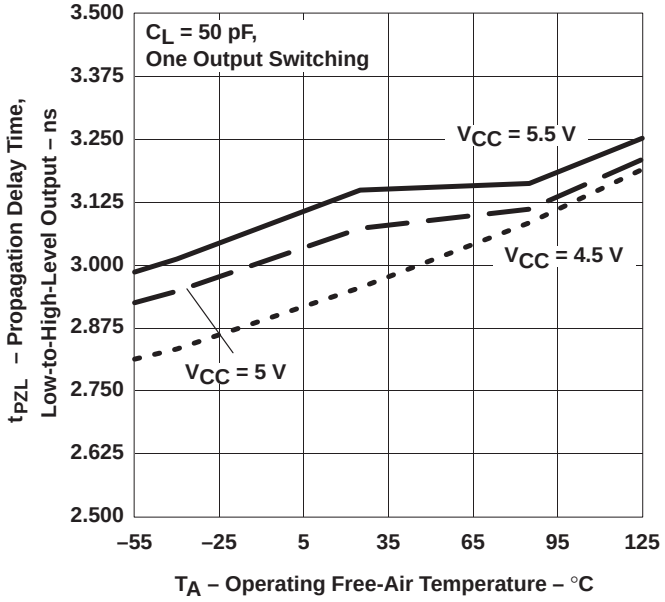
PROPAGATION DELAY TIME
ENABLE-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO Y



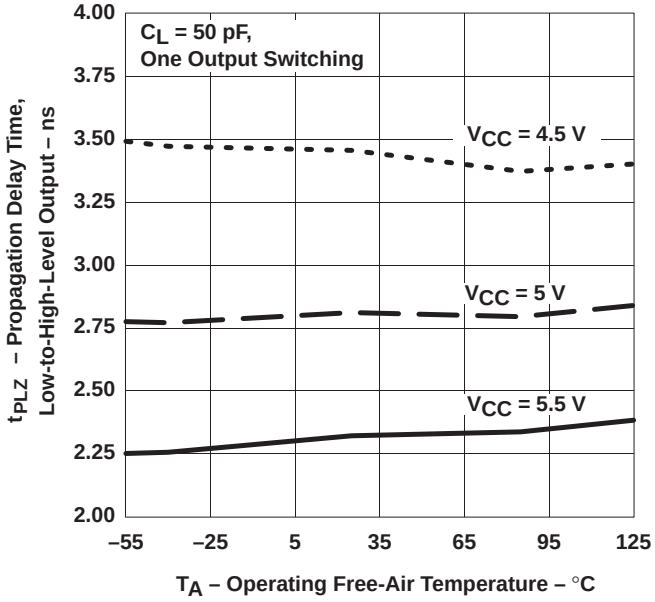
PROPAGATION DELAY TIME
DISABLE-FROM-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TOY



PROPAGATION DELAY TIME
ENABLE-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO Y

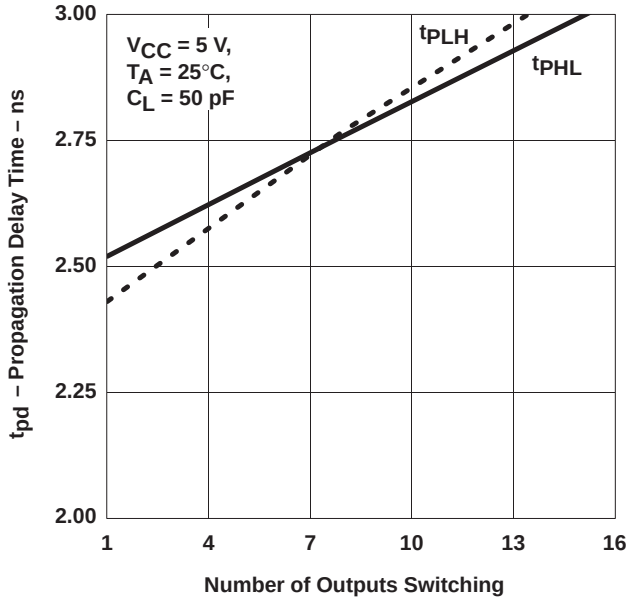


PROPAGATION DELAY TIME
DISABLE-FROM-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO Y

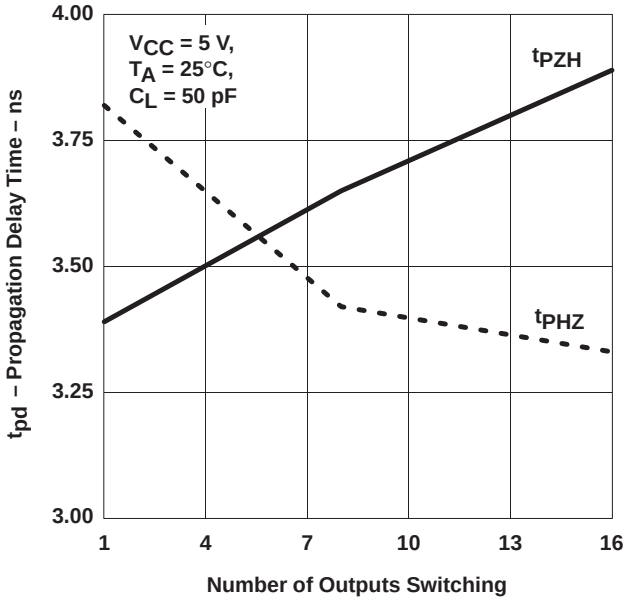


Propagation Delay Time vs Number of Outputs Switching

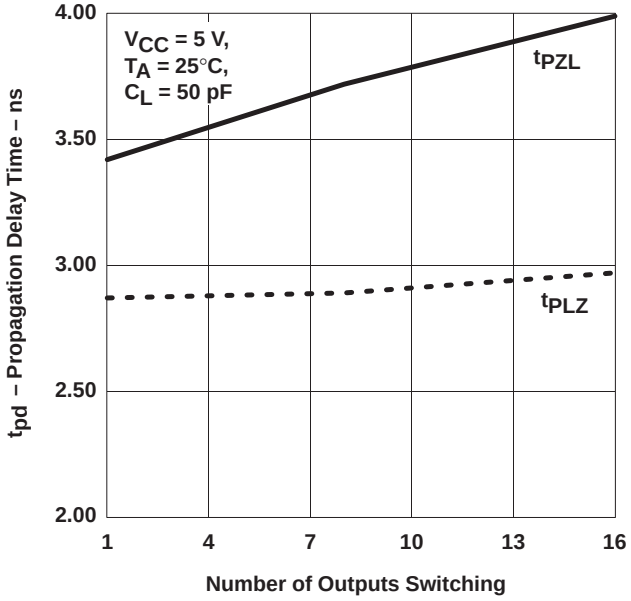
PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING A TO Y



PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING $\overline{OE}$ TO Y

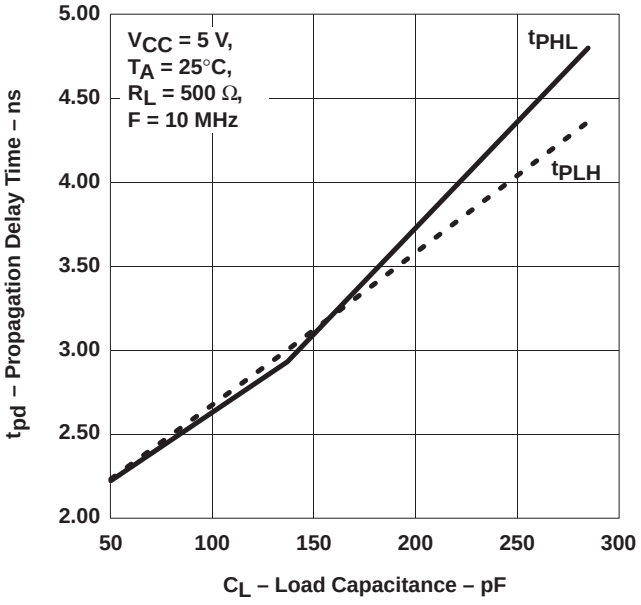


PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING $\overline{OE}$ TO Y

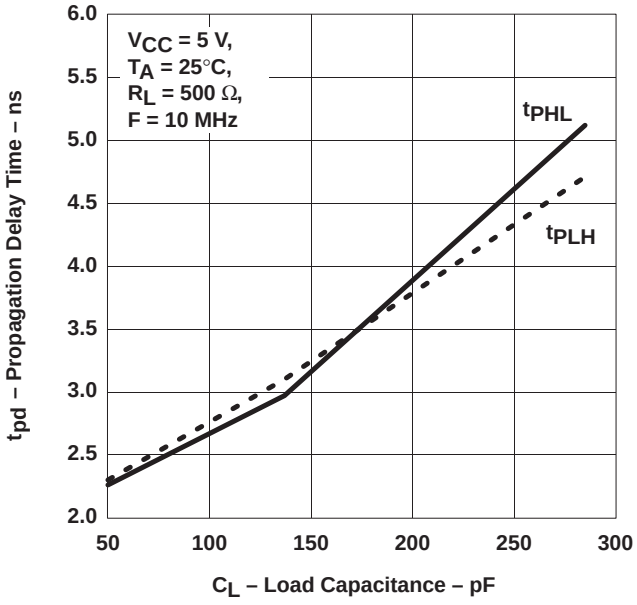


Propagation Delay Time vs Load Capacitance

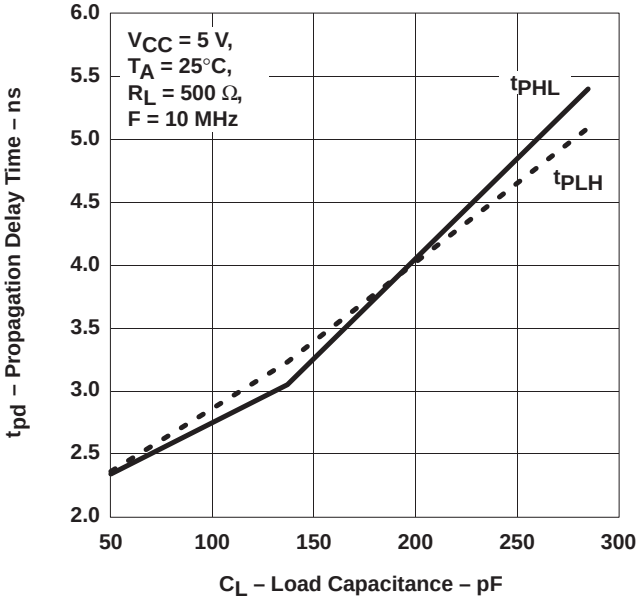
A TO Y
ONE OUTPUT SWITCHING



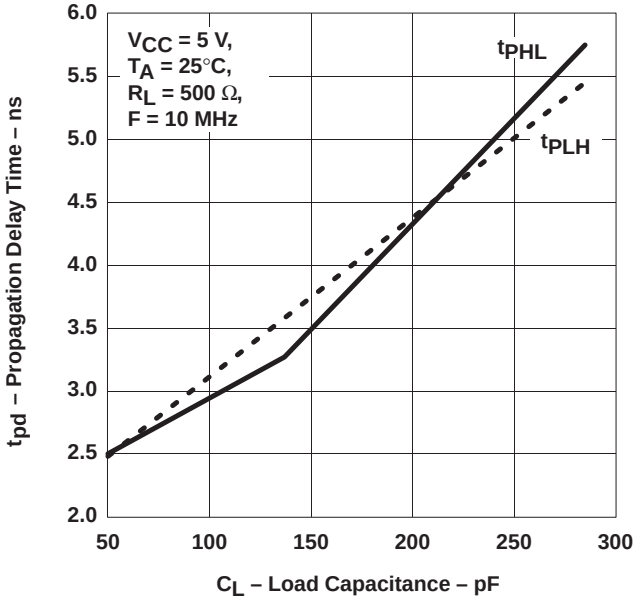
A TO Y
FOUR OUTPUTS SWITCHING



A TO Y
EIGHT OUTPUTS SWITCHING

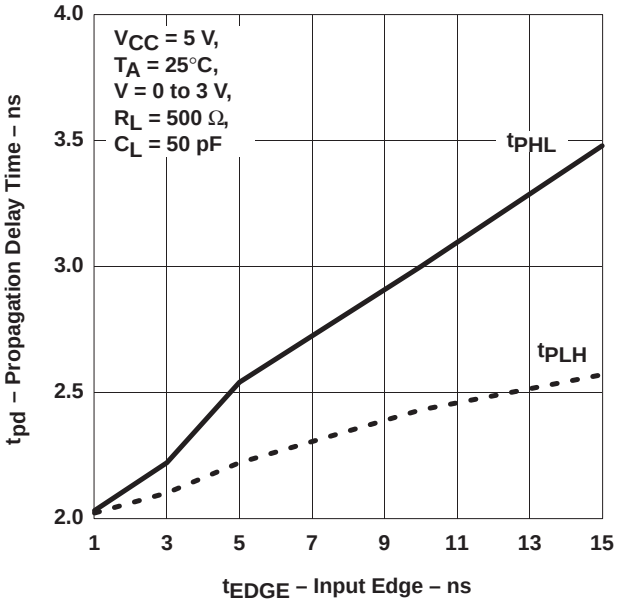


A TO Y
16 OUTPUTS SWITCHING

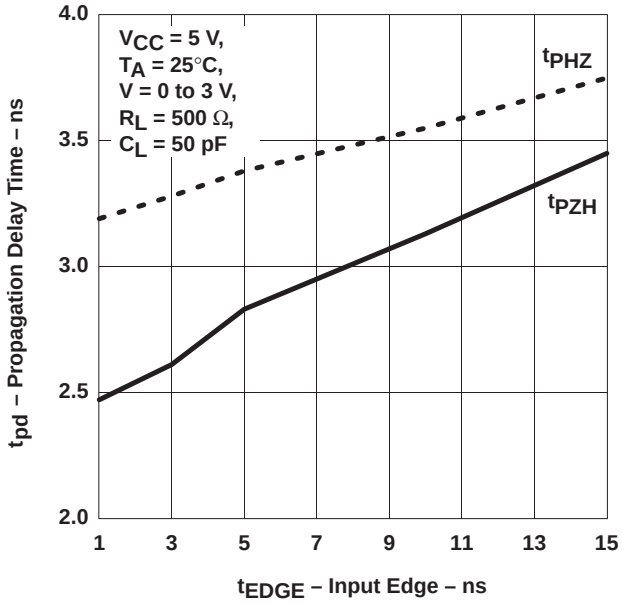


Propagation Delay Time vs Input Edge

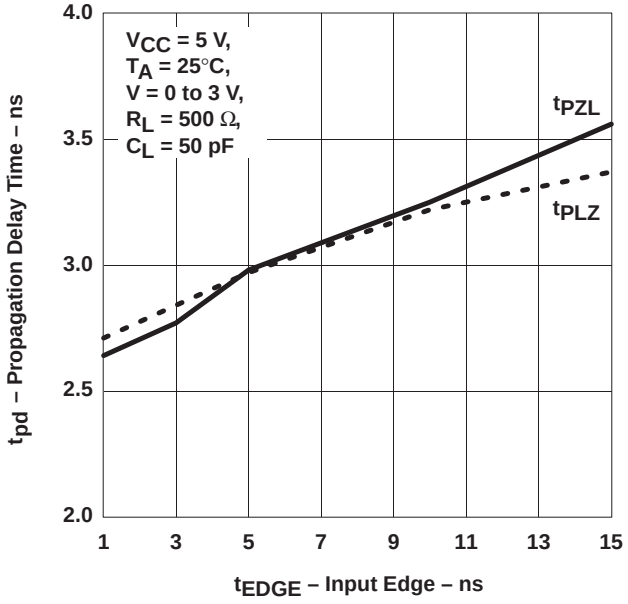
PROPAGATION DELAY TIME vs INPUT EDGE A TO Y



PROPAGATION DELAY TIME vs INPUT EDGE $\overline{OE}$ TO Y

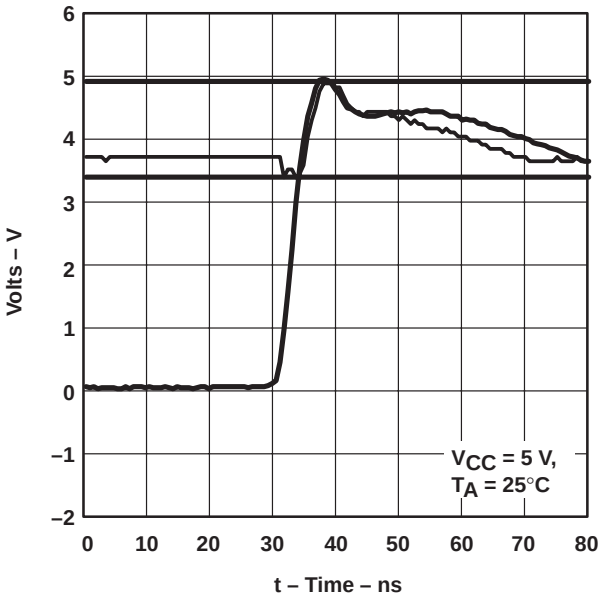


PROPAGATION DELAY TIME vs INPUT EDGE $\overline{OE}$ TO Y

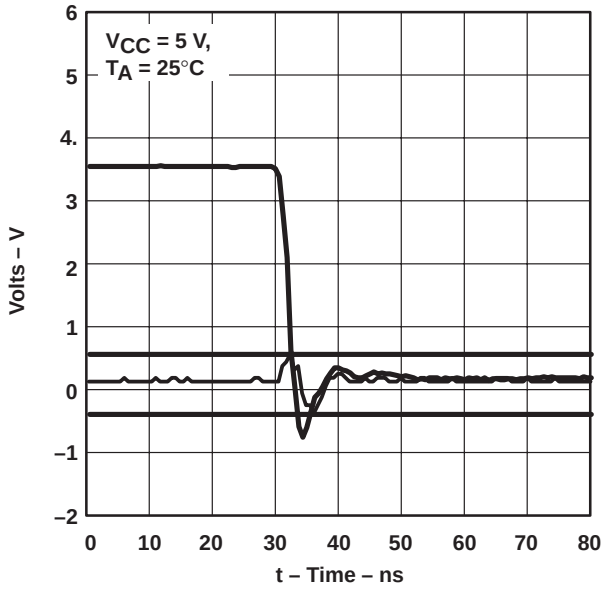


V_{OHV} and V_{OLP}

15 SWITCHING 1 HIGH LH A → Y



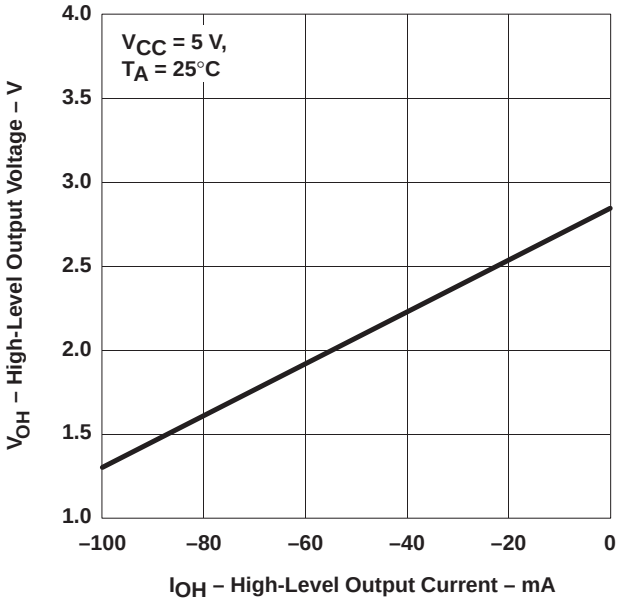
15 SWITCHING 1 LOW HL A → Y



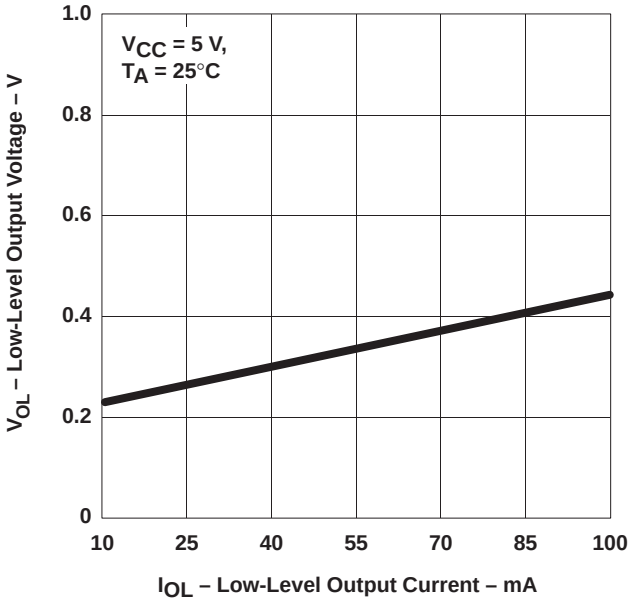
V_{OHV} = Minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs.
V_{OLP} = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.

Typical Characteristics

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

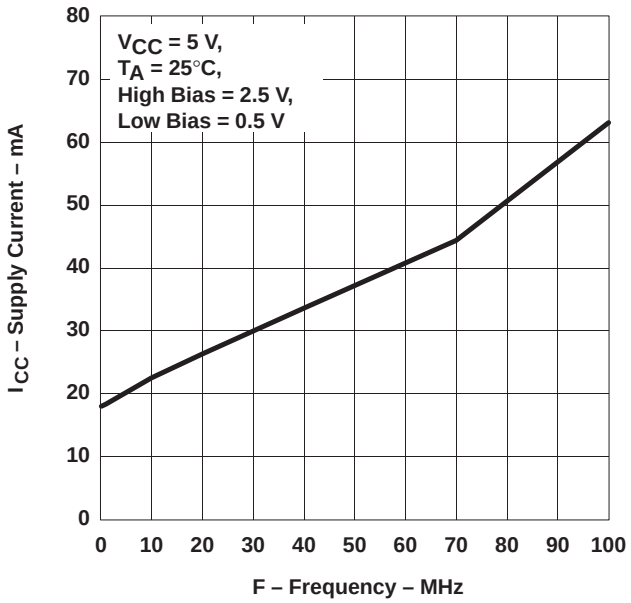


LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

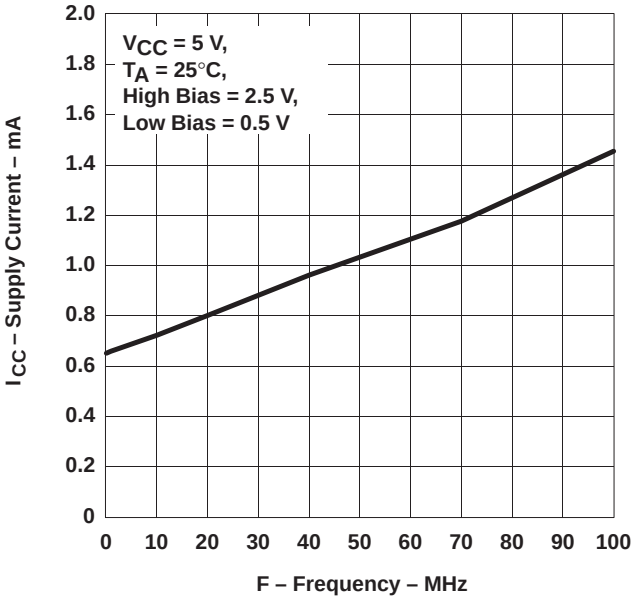


Supply Current vs Frequency

OUTPUTS ENABLED



OUTPUTS DISABLED

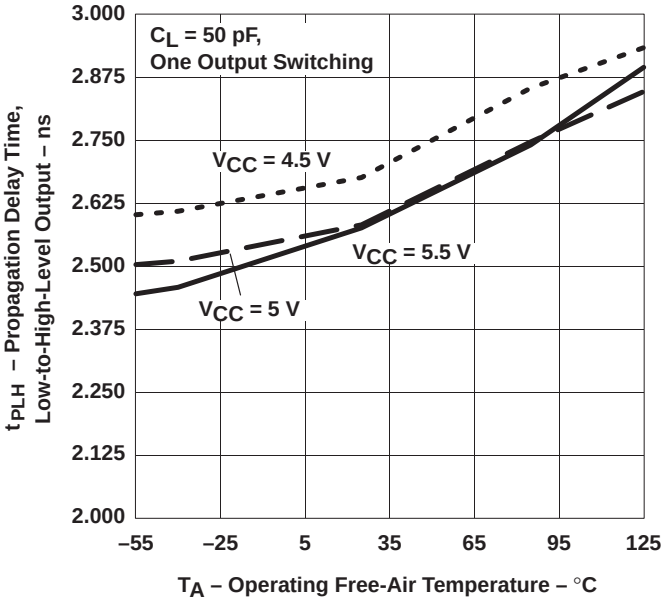


APPENDIX C
’ABT16500B Characterization Data

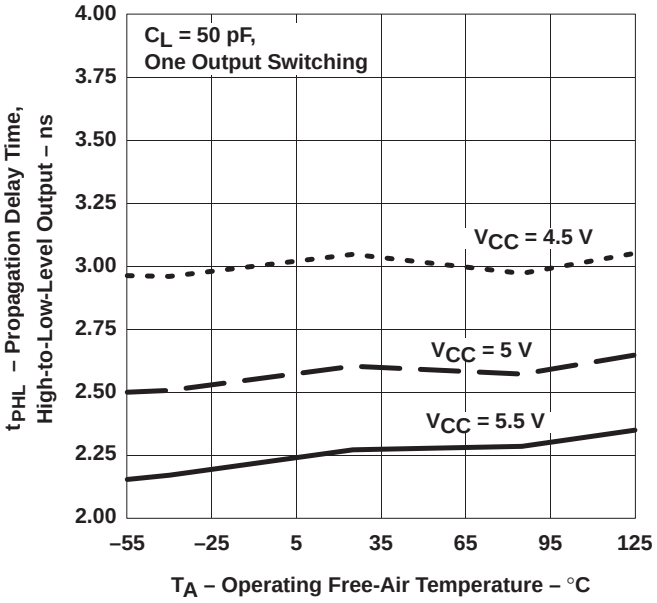
C

Propagation Delay Time vs Temperature

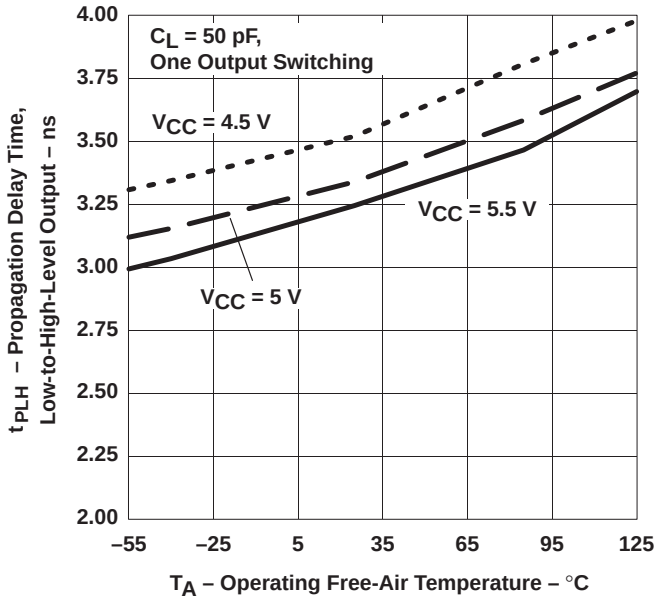
**PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A TO B**



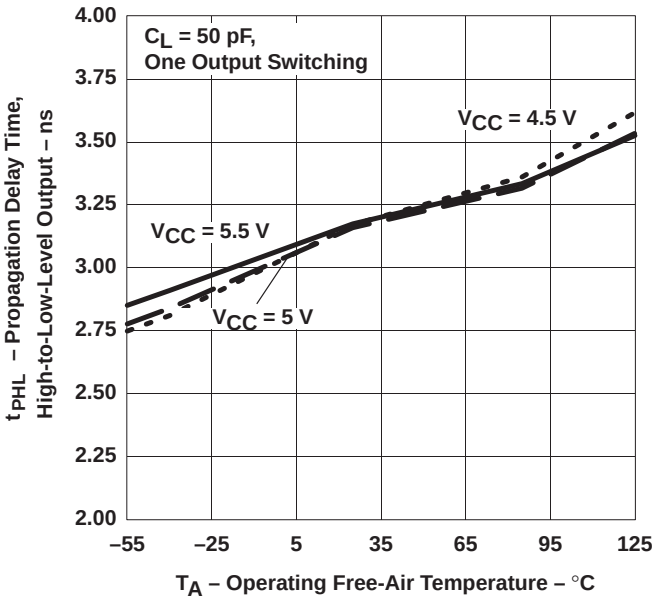
**PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A TO B**



**PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
LEAB TO B**

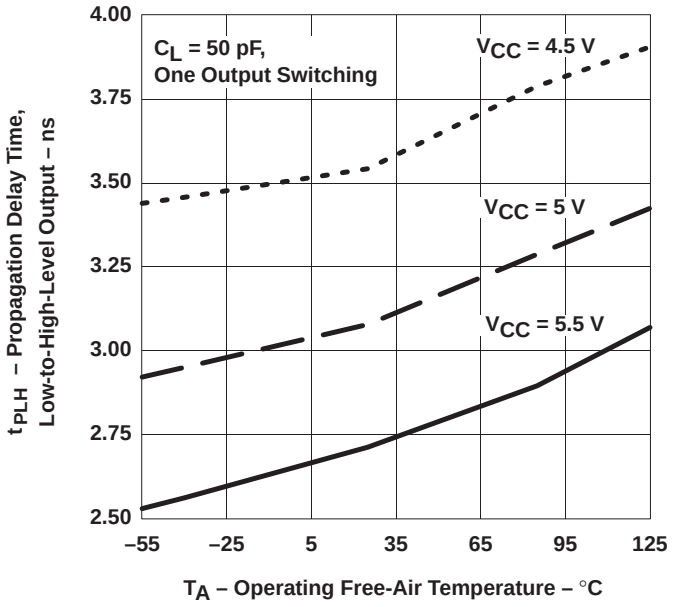


**PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
LEAB TO B**

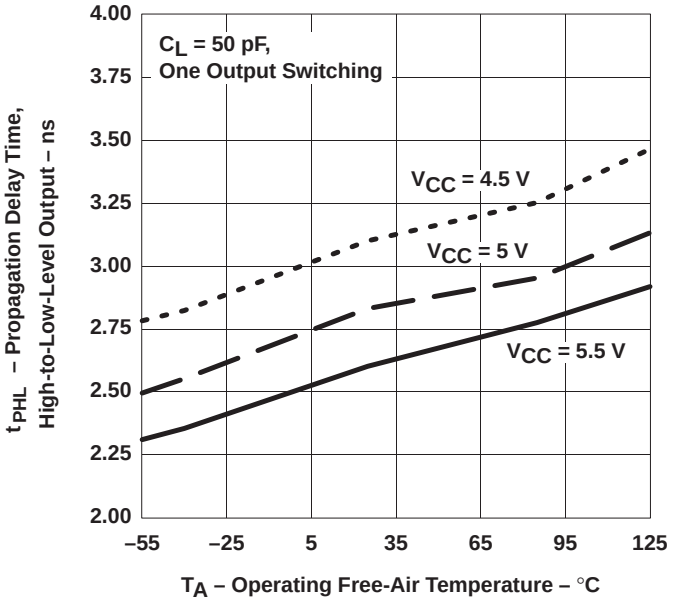


Propagation Delay Time vs Temperature

PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{\text{CLKAB}}$ TO B

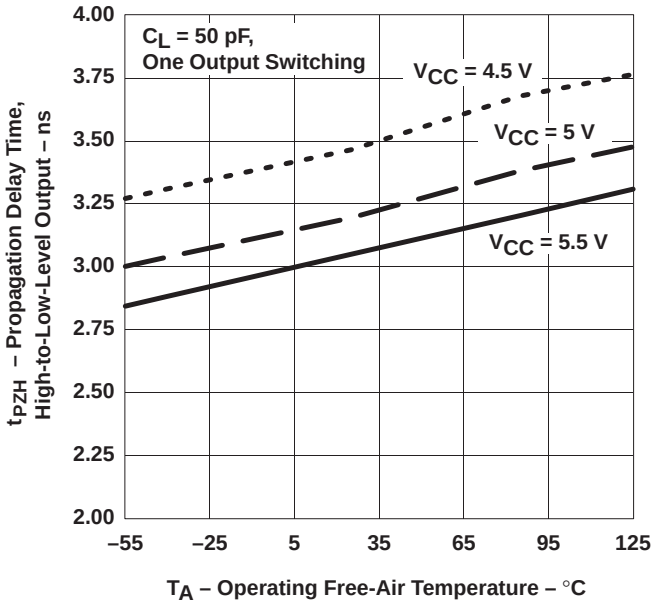


PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{\text{CLKAB}}$ TO B

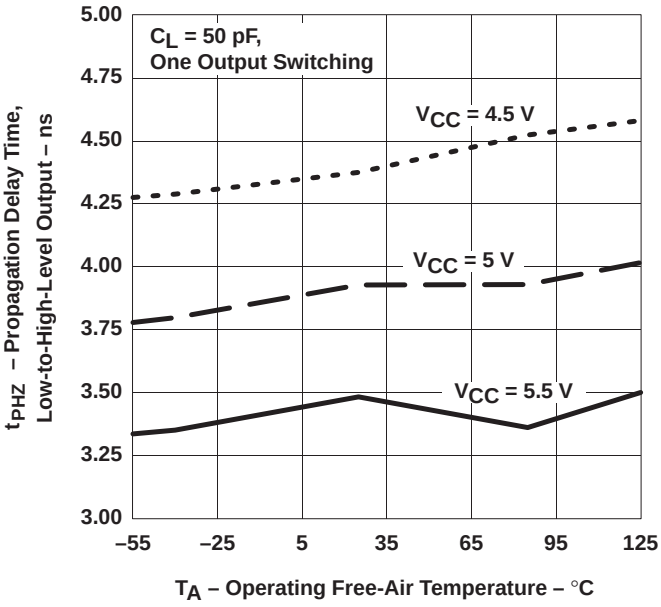


Propagation Delay Time vs Temperature

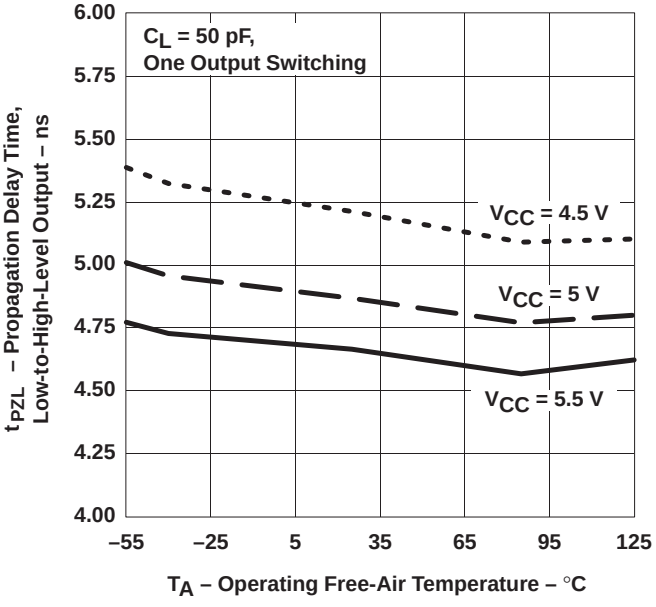
**PROPAGATION DELAY TIME
ENABLE-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
OEAB TO B**



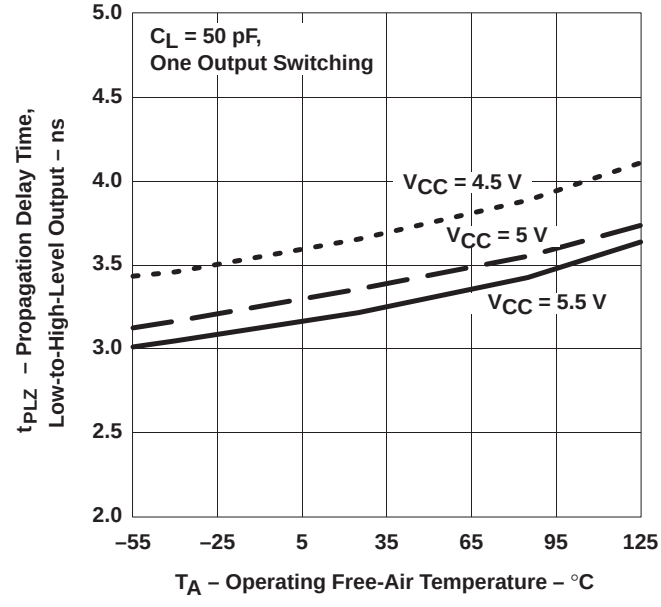
**PROPAGATION DELAY TIME
DISABLE-FROM-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
OEAB TO B**



**PROPAGATION DELAY TIME
ENABLE-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
OEAB TO B**

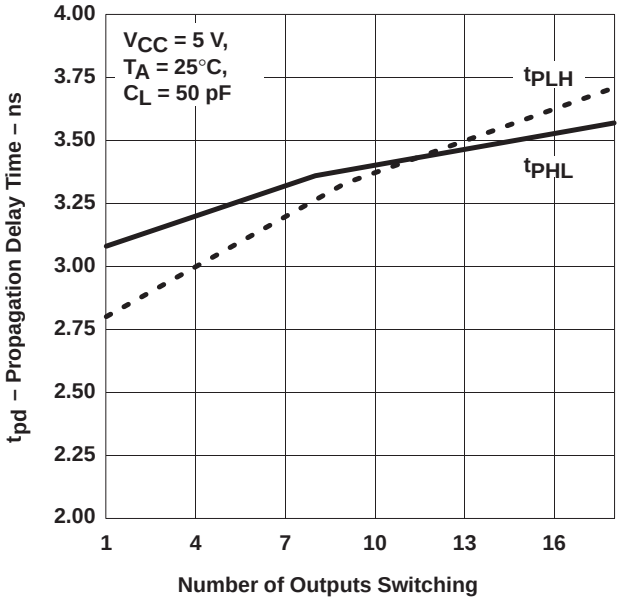


**PROPAGATION DELAY TIME
DISABLE-FROM-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
OEAB TO B**

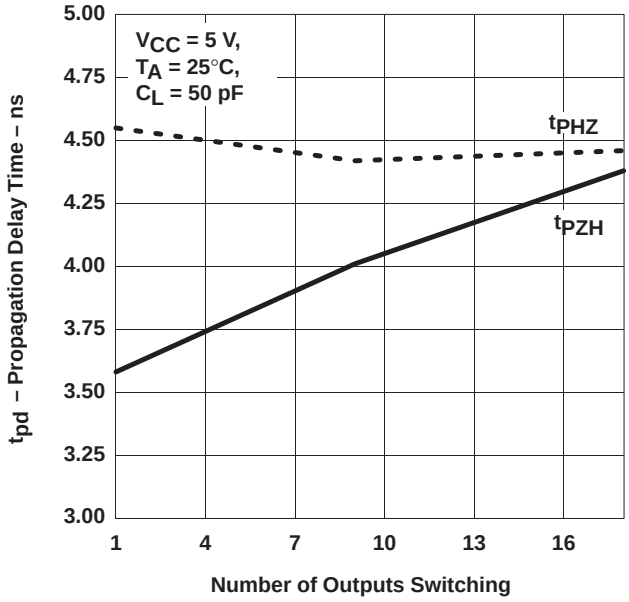


Propagation Delay Time vs Number of Outputs Switching

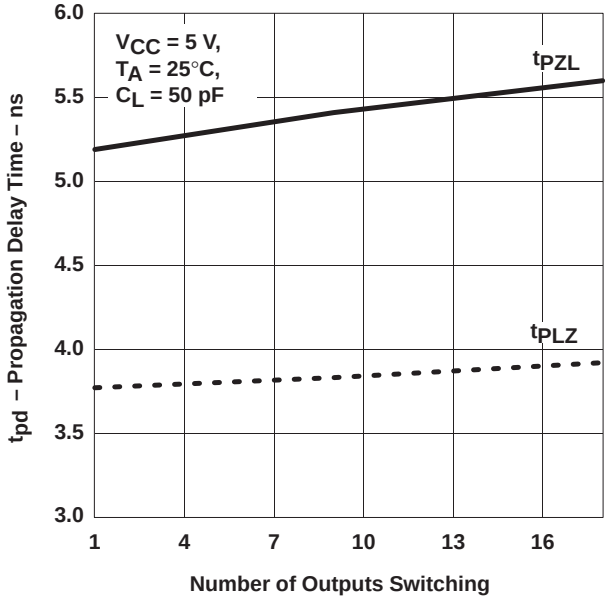
PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
A TO B



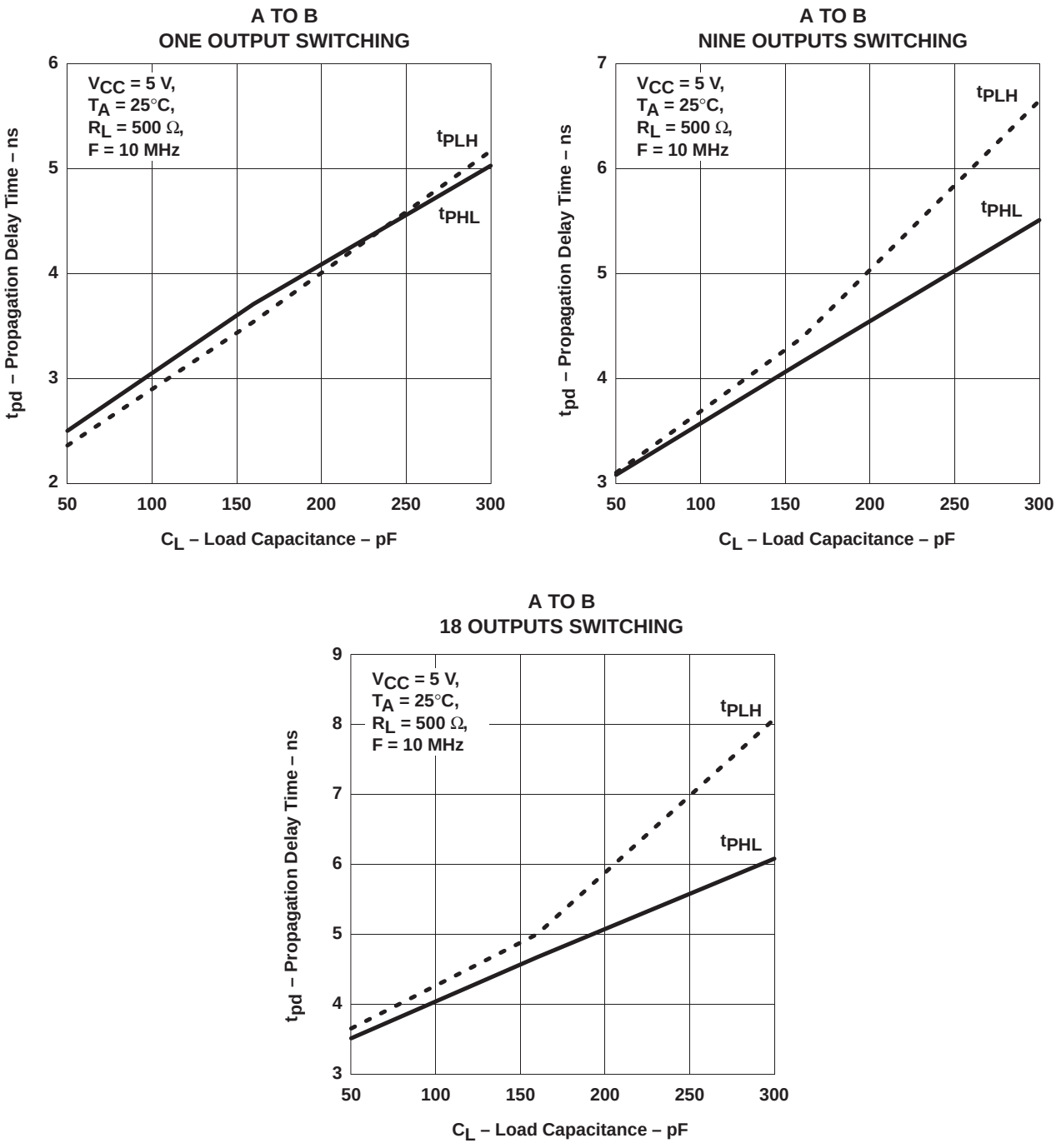
PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
OEAB TO B



PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
OEAB TO B

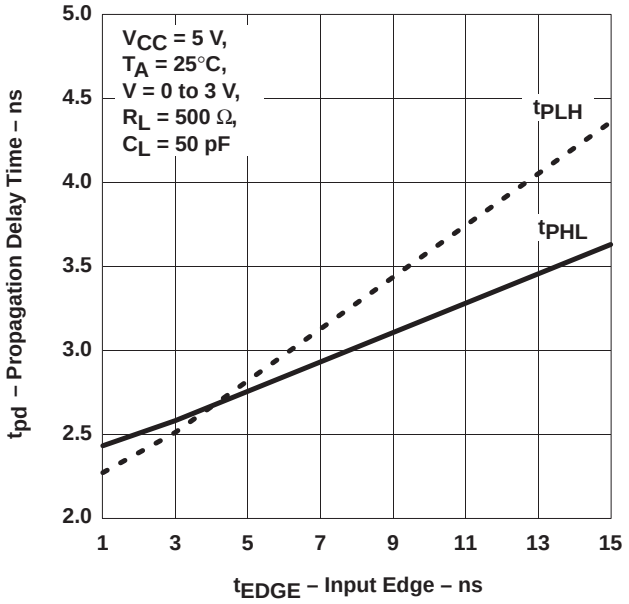


Propagation Delay Time vs Load Capacitance

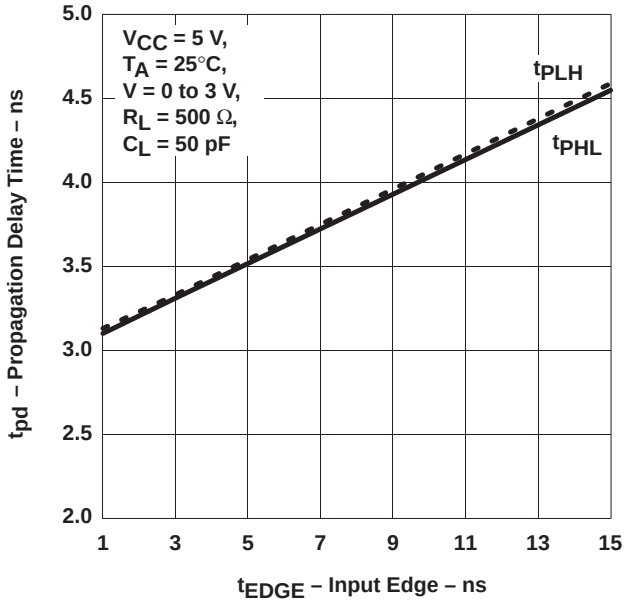


Propagation Delay Time vs Input Edge

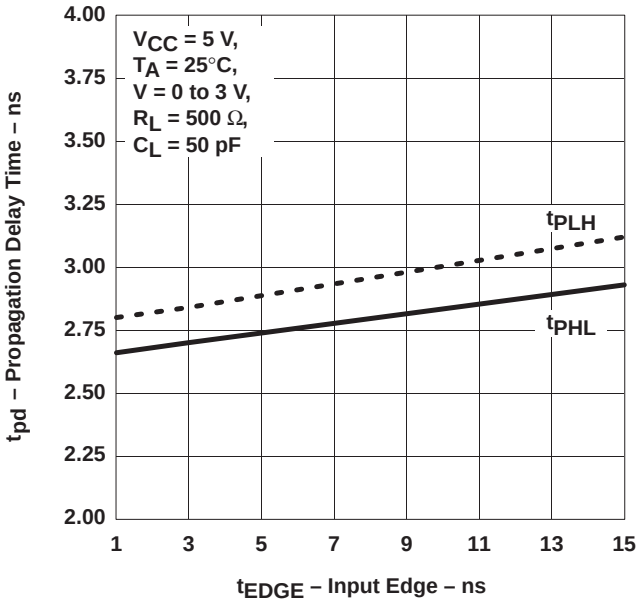
PROPAGATION DELAY TIME vs INPUT EDGE A TO B



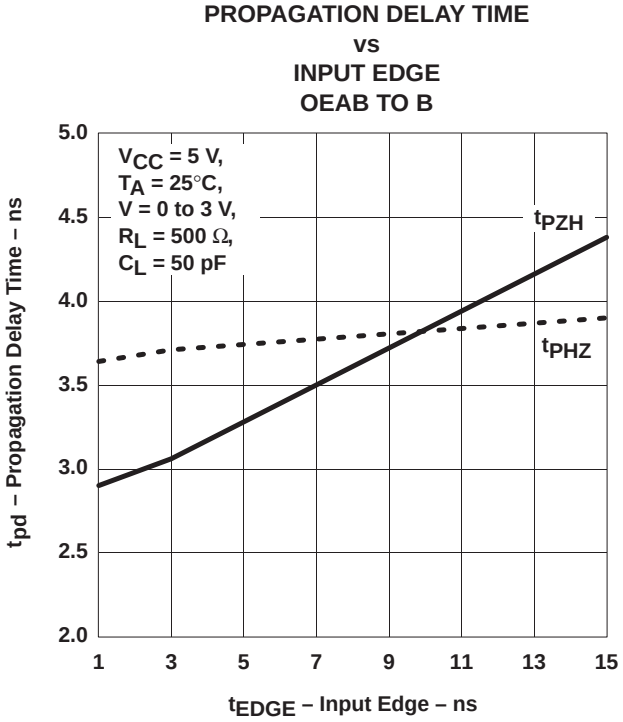
PROPAGATION DELAY TIME vs INPUT EDGE LEAB TO B

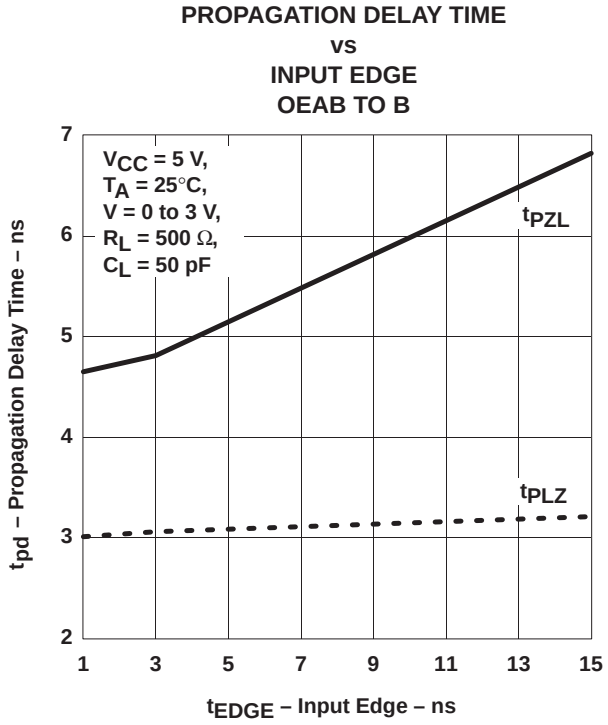


PROPAGATION DELAY TIME vs INPUT EDGE CLKAB TO B



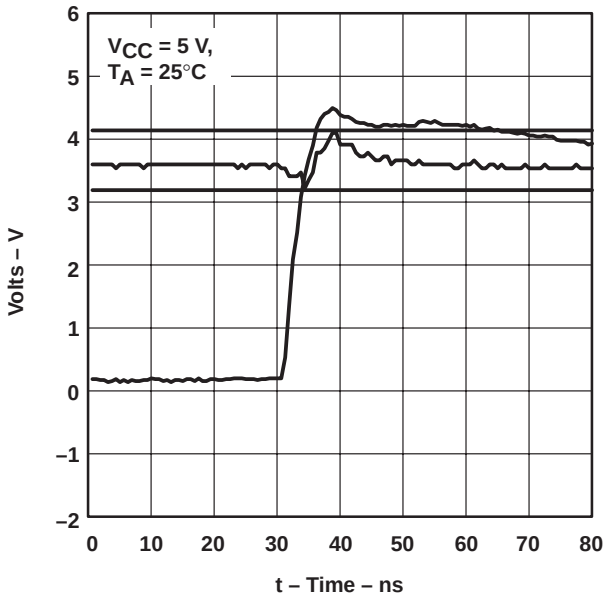
Propagation Delay Time vs Input Edge



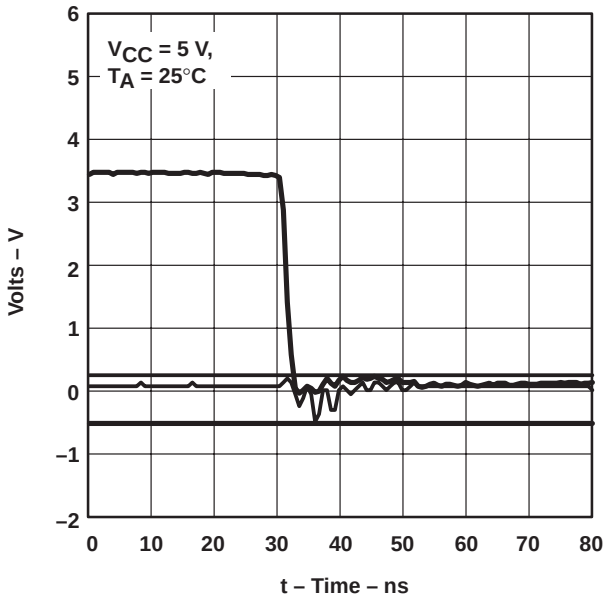


V_{OHV} and V_{OLP}

17 SWITCHING 1 HIGH LH B → A



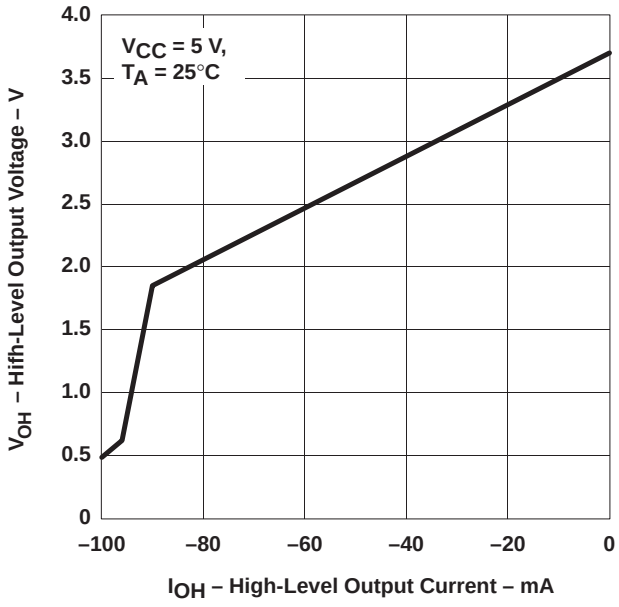
17 SWITCHING 1 LOW HL B → A



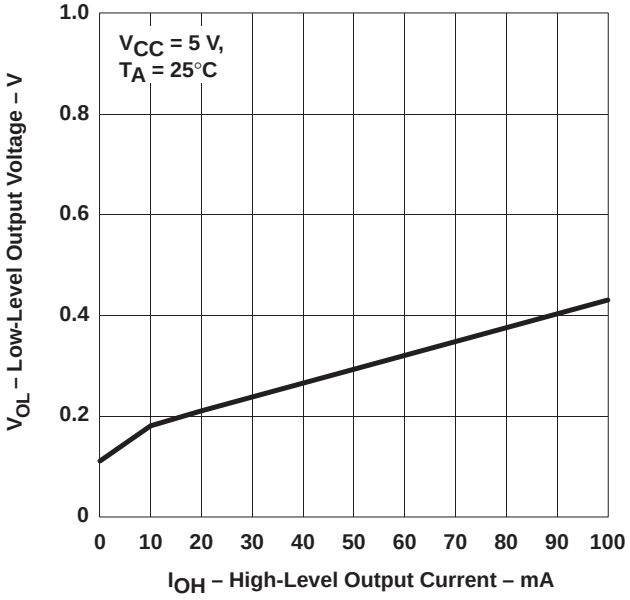
V_{OHV} = Minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs.
V_{OLP} = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.

Typical Characteristics

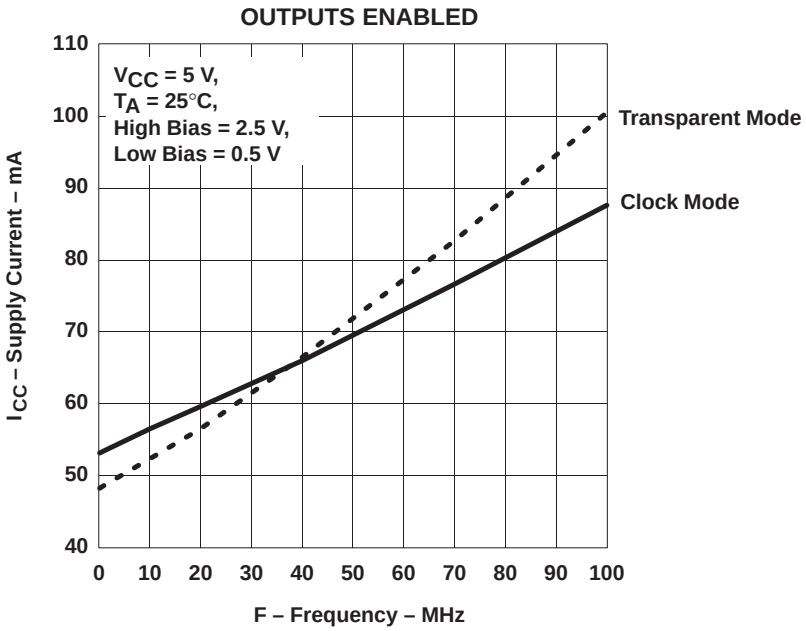
HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT



LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

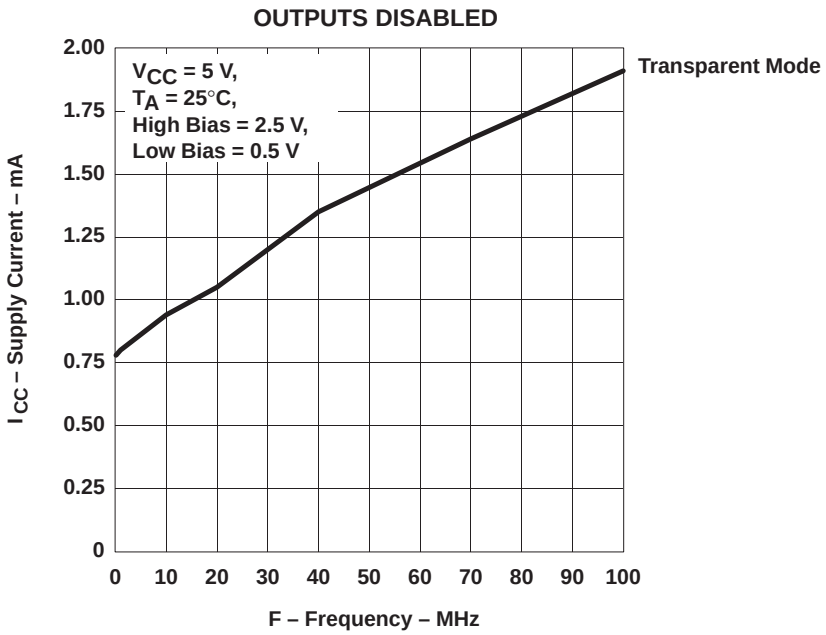


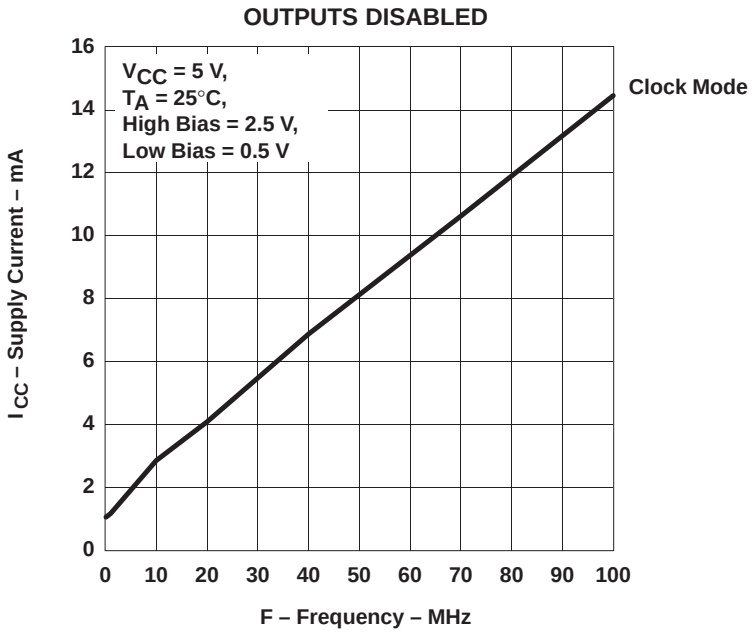
Supply Current vs Frequency



NOTE: Characteristics for latch mode are similar to those when in clock mode.

Supply Current vs Frequency





NOTE: Characteristics for latch mode are similar to those when in clock mode.