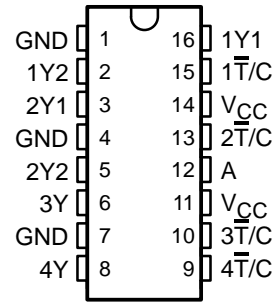


CDC329 1-LINE TO 6-LINE CLOCK DRIVER WITH SELECTABLE POLARITY

SCBS117A–D4501, JANUARY 1991–REVISED NOVEMBER 1992

- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- State-of-the-Art *EPIC-IIB*™ BiCMOS Design Significantly Reduces Power Dissipation
- TTL-Compatible Inputs and CMOS-Compatible Outputs
- Distributes One Clock Input to Six Clock Outputs
- Polarity Control Selects True or Complementary Outputs
- Distributed V_{CC} and GND Pins Reduce Switching Noise
- High-Drive Outputs (–15-mA I_{OH}, 64-mA I_{OL})
- Packaged in Plastic Small-Outline Package

D PACKAGE
(TOP VIEW)



description

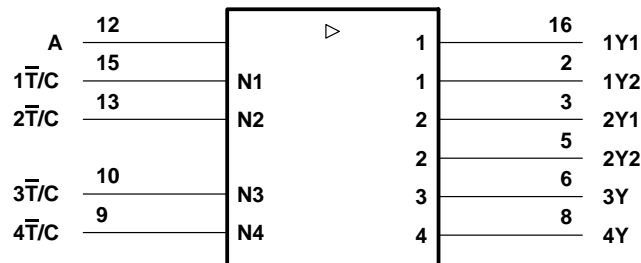
The CDC329 contains a clock driver circuit that distributes one input signal to six outputs with minimum skew for clock distribution. Through the use of the polarity control inputs ($\overline{T/C}$), various combinations of true and complementary outputs can be obtained.

The CDC329 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

| INPUTS | | OUTPUT |
|------------------|---|--------|
| $\overline{T/C}$ | A | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

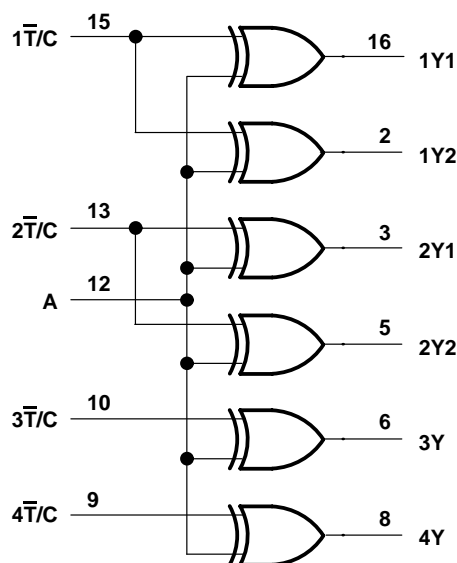
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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -1.2 V to 7 V |
| Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) | -0.5 V to $V_{CC} + 0.5$ V |
| Current into any output in the low state, I_O | 128 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | -18 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) | 1000 mW |
| Storage temperature range | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. For operation above 25°C free-air temperature, derate to 478 mW at 85°C at the rate of 8.7 mW/°C.

recommended operating conditions (see Note 3)

| | MIN | NOM | MAX | UNIT |
|--|------|-----|----------|------|
| V_{CC} Supply voltage | 4.75 | 5 | 5.25 | V |
| V_{IH} High-level input voltage | 2 | | | V |
| V_{IL} Low-level input voltage | | | 0.8 | V |
| V_I Input voltage | 0 | | V_{CC} | V |
| I_{OH} High-level output current | | | -15 | mA |
| I_{OL} Low-level output current | | | 64 | mA |
| $\Delta t/\Delta v$ Input transition rise or fall rate | | | 5 | ns/V |
| T_A Operating free-air temperature | -40 | | 85 | °C |

NOTE 3: Unused inputs must be held high or low.

CDC329

1-LINE TO 6-LINE CLOCK DRIVER WITH SELECTABLE POLARITY

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|-----------|---|--------------------------|--------------|------|---------|---------------|
| V_{IK} | $V_{CC} = 4.75\text{ V}$, | $I_I = -18\text{ mA}$ | | | -1.2 | V |
| V_{OH} | $V_{CC} = 4.75\text{ V}$, | $I_{OH} = -15\text{ mA}$ | 3.85 | | | V |
| V_{OL} | $V_{CC} = 4.75\text{ V}$, | $I_{OL} = 64\text{ mA}$ | | | 0.55 | V |
| I_I | $V_{CC} = 5.25\text{ V}$, | $V_I = V_{CC}$ or GND | | | ± 1 | μA |
| I_{CC} | $V_{CC} = 5.25\text{ V}$, $V_I = V_{CC}$ or GND | $I_O = 0$, | Outputs high | | 50 | μA |
| | | | Outputs low | | 20 | 30 |
| C_i | $V_I = 2.5\text{ V}$ or 0.5 V | | | 3 | | pF |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

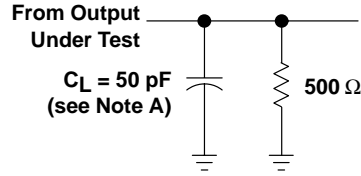
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP | MAX | UNIT |
|-------------|--------------|--------------------|-----|-----|-----|------|
| t_{PLH} | A | Any Y | 2 | | 6.6 | ns |
| t_{PHL} | | | 1.7 | | 5.4 | |
| t_{PLH} | \bar{T}/C | Any Y | 1.6 | | 7.4 | ns |
| t_{PHL} | | | 1.7 | | 6.3 | |
| $t_{sk(o)}$ | A | Any Y (same phase) | | | 0.5 | ns |
| | | Any Y (any phase) | | | 2.5 | |
| t_r | | | | 2 | | ns |
| t_f | | | | 1.3 | | ns |

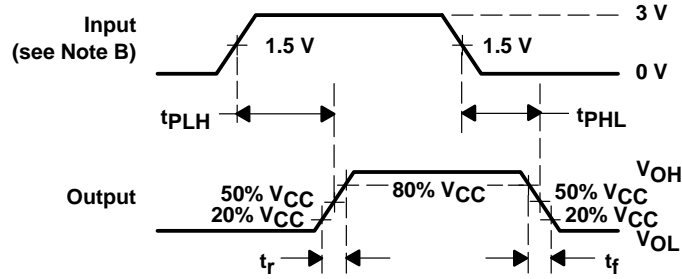
switching characteristics, $V_{CC} = 5\text{ V} \pm 0.25\text{ V}$, $T_A = 25^\circ\text{C}$ to 70°C (see Figures 1 and 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | MAX | UNIT |
|-------------|--------------|--------------------|-----|-----|------|
| t_{PLH} | A | Any Y | 2.3 | 5.9 | ns |
| t_{PHL} | | | 1.7 | 4.8 | |
| $t_{sk(o)}$ | A | Any Y (same phase) | | 0.5 | ns |
| | | Any Y (any phase) | | 2 | |

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS

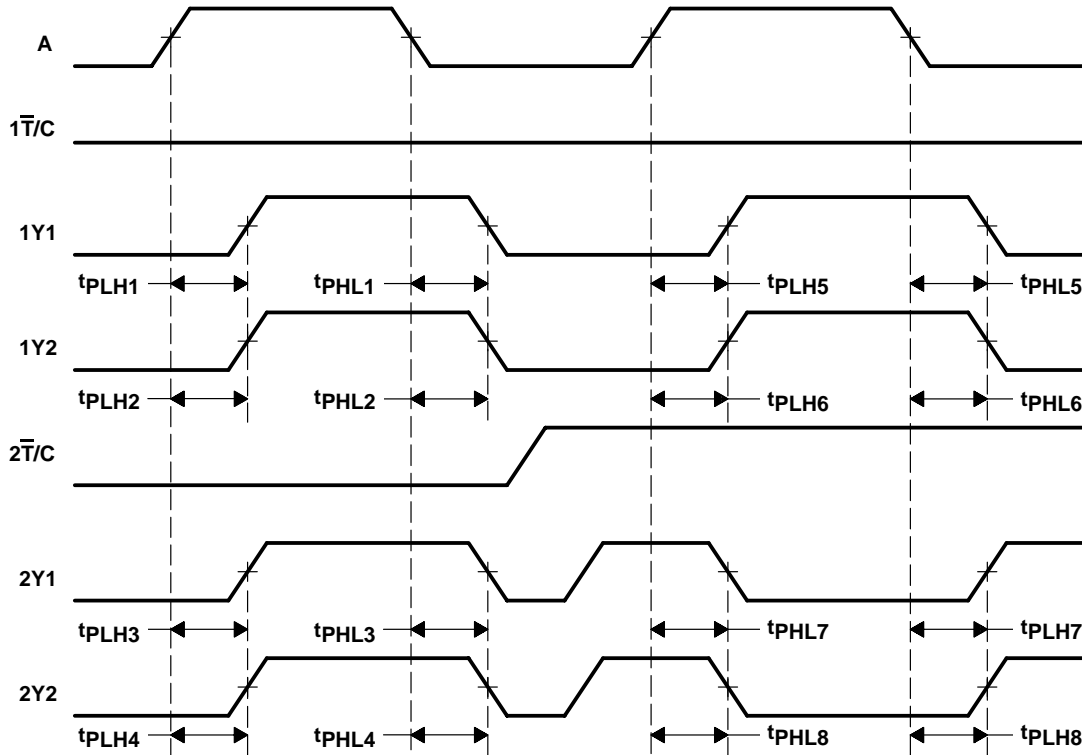


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

Figure 1. Load Circuit and Voltage Waveforms

WAVEFORMS FOR CALCULATION OF $t_{sk(o)}$



Output skew, $t_{sk(o)}$, from A to any Y (same phase), can be measured only between outputs for which the respective polarity control inputs (\bar{T}/C) are at the same logic level. It is calculated as the greater of:

- the difference between the fastest and slowest of t_{PLH} from $A\uparrow$ to any Y (e.g., t_{PLHn} , $n = 1$ to 4; or t_{PLHn} , $n = 5$ to 6),
- the difference between the fastest and slowest of t_{PHL} from $A\downarrow$ to any Y (e.g., t_{PHLn} , $n = 1$ to 4; or t_{PHLn} , $n = 5$ to 6),
- the difference between the fastest and slowest of t_{PLH} from $A\downarrow$ to any Y (e.g., t_{PLHn} , $n = 7$ to 8), and
- the difference between the fastest and slowest of t_{PHL} from $A\uparrow$ to any Y (e.g., t_{PHLn} , $n = 7$ to 8).

Output skew, $t_{sk(o)}$, from A to any Y (any phase), can be measured between outputs for which the respective polarity control inputs (\bar{T}/C) are at the same or different logic levels. It is calculated as the greater of:

- the difference between the fastest and slowest of t_{PLH} from $A\uparrow$ to any Y or t_{PHL} from $A\uparrow$ to any Y (e.g., t_{PLHn} , $n = 1$ to 4; or t_{PLHn} , $n = 5$ to 6, and t_{PHLn} , $n = 7$ to 8), and
- the difference between the fastest and slowest of t_{PHL} from $A\downarrow$ to any Y or t_{PLH} from $A\downarrow$ to any Y (e.g., t_{PHLn} , $n = 1$ to 4; or t_{PHLn} , $n = 5$ to 6, and t_{PLHn} , $n = 7$ to 8).

Figure 2. Skew Waveforms and Calculations

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