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# PCI1131 CardBus Controller Power Considerations

## Application Report

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# PCI1131 CardBus Controller Power Considerations

**ABSTRACT**

The Texas Instruments (TI™) PCI1131 is a high-performance PCI-to-PC Card controller that supports two independent PC Card sockets. This application report addresses the TI CardBus controller family and how it meets the ever-increasing demands for power savings in mobile PCs using legacy power management methods. It assists mobile system designers who use the PCI1131 to develop power management applications.

## 1 Introduction

The Texas Instruments PCI1131 is a high-performance PCI-to-PC Card controller that supports two independent PC Card™ sockets and is compliant with the *1995 PC Card Standard* [1]. PCI-to-PC Card controllers provide features that make them ideal for bridging peripheral component interconnect (PCI) and PC Cards in both notebook and desktop computers. The *1995 PC Card Standard* [1] retains the 16-bit PC Card specification defined in the *Personal Computer Memory Card International Association (PCMCIA) Specification, Release 2.1* [2], and defines the new 32-bit PC Card called CardBus, which is capable of full 32-bit data transfers at 33 MHz. The PCI1131 supports any combination of 16-bit and CardBus PC Cards in its two sockets, powered at 3.3 V or 5 V, as required.

These features come at a price, however, because battery technology has not kept pace with other technologies. The mobile system designer must account for each watt and go to great lengths to conserve power wherever possible. All system components are under industry scrutiny and the PCMCIA subsystem is no exception.

One of the key goals of the PCMCIA subsystem is the *plug and play* concept. To realize this concept, PC Cards and host systems from different vendors must be designed for power compatibility. There are currently industry efforts to reach this goal, which include power-management standards such as the *Advanced Power Management (APM) Specification* [3] and PCI Power-Management Working Group adoptions.

Currently, the industry is in the midst of a transition in power management. The challenge for semiconductor vendors is to design to these evolving standards and yet strike a balance between power, performance, and features.

Despite the challenges, the mobile platform has made tremendous advances in recent years. Larger and high-resolution active-matrix screens, faster microprocessors, and high-capacity hard disk drives have brought meaning to the term *desktop replacement*. The PCMCIA subsystem is designed to meet these new developments.

# 2 Power Consumption in the PCMCIA Subsystem

Figure 1 is a functional block diagram of a PCMCIA subsystem. The PCMCIA subsystem includes the PC Card slots A and B, the power switch, and the PCI-based PC Card controller. Figure 1 illustrates TI's PCMCIA implementation using the PCI1131 and TPS2206. To minimize the power of the PCMCIA subsystem, the power interface for each of these components must be examined carefully.

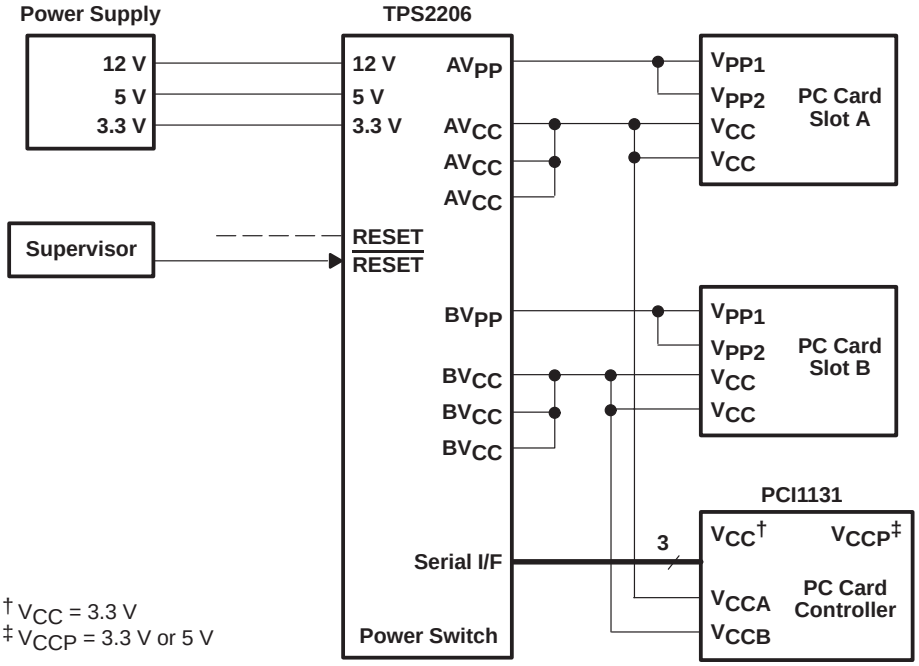



**Figure 1. PCMCIA Subsystem**

## 2.1 PC Card Power Considerations

The largest sources of power dissipation shown in Figure 1 are the PC Card slots. The common interpretation of the *1995 PC Card Standard* [1] is that the card can draw a maximum of 1 amp through the $V_{CC}$ terminals and 100 mA through the $V_{PP}$ terminals. In practice, few cards actually draw current that high for sustained periods; rotating media and hard disk drives can approach this limit for brief periods while spinning up cylinders.

PC Card16 or R2 cards offer few opportunities for power management at the signal level. The PCMCIA subsystem addresses power management of these cards at the metaformat level by incorporating a power-down state that card and socket services can control. CardBus PC Cards offer some relief, first by requiring $V_{CC}$ of 3.3 V or lower. Also, the wake-up procedure for the CardBus cards allows the entire card to be powered off and yet wake the host, unlike the PC Card16 cards, which use a ring-indicate signal while still powered. Further, the inclusion of clock run ($\overline{\text{CLKRUN}}$) allows the host to dynamically control the CardBus card clock, which is effective in reducing the card's power dissipation.

## 2.2 TI Power Switch

The TI power switch, TPS2206, is a companion chip to the TI CardBus controller family, and it offers an integrated power-switching solution for the PCMCIA subsystem. The power switch consumes power only through its $V_{DD}$ supply and through FET-on resistance. The switch $V_{DD}$ supply powers only a small portion of the digital logic, drawing less than 150 μA. For the FET on resistance, a value of zero is desirable but impractical. The typical on-resistance of the TPS2206 is low at 110–140 mΩ, which makes the TPS2206 an industry leader in switch performance.

## 2.3 TI CardBus Controller

The CardBus controller has several voltage supply pins, $V_{CCP}$, $V_{CCA}$, $V_{CCB}$, and $V_{CC.}$ as shown in Figure 1. $V_{CCP}$, $V_{CCA}$, and $V_{CCB}$ are not voltage supply pins in the traditional sense, in that they only indicate the signaling environment of the PCI, PC card A, and PC Card B buses, respectively. $V_{CCP}$ must be fixed at either 5 V or 3.3 V, depending on the PCI signaling environment used. The $V_{CCA}$ and $V_{CCB}$ pins must change dynamically depending on the type of PC Card in use. These pins are connected directly to the PC Card $V_{CC}$ pin of the appropriate slot. This configuration means that the switching environment is set automatically when a PC Card is powered. Each of the voltage supplies, $V_{CCP}$, $V_{CCA}$, and $V_{CCB}$, contribute only minimally to the CardBus controller power dissipation, and each exhibits an average current draw of less than 100 nA.

The primary source of power consumption in the TI CardBus controller family is through the $V_{CC}$ terminals. These terminals supply power to the device and to its output buffers. This draw of current varies according to the particular CardBus controller and its operating conditions. The maximum power consumption of the PCI1131 is approximately 80 mA. This measurement is made under the highest performance, worst-case conditions when operating with CardBus burst transfers and using no dynamic clock control.

Like all complementary metal-oxide semiconductor (CMOS)-based digital technologies, power consumption for TI PCI card controllers is linearly related to the clock rate. The primary clock in the TI PCI1131 CardBus controller is the PCI clock, which operates at a maximum rate of 33 MHz. PCI clock control can be an effective means of saving power. A fine-grained clock-control mechanism (PCI $\overline{\text{CLKRUN}}$) is described in the *PCI Mobile Design Guide, Revision 1.0* [4].

# 3 $\overline{\text{CLKRUN}}$ Featured on the PCI1131

Figure 2 is a functional block diagram of the PCI clocking agents. The *PCI Mobile Design Guide, Revision 1.0* [4] describes the $\overline{\text{CLKRUN}}$ protocol and its use to enable optimum power savings in a PCI-based mobile computer. Using $\overline{\text{CLKRUN}}$, a chipset may stop or slow the PCI clock during periods of inactivity, and peripherals may request that the clock be restarted upon a change of status. The routing of the $\overline{\text{CLKRUN}}$ signal is shown in Figure 2.

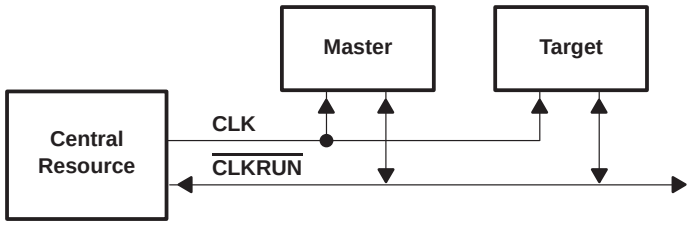



**Figure 2. PCI Clocking Agents**

The three PCI clocking agents shown are the central resource, master, and target devices. The roles of these clocking agents are:

- The central resource controls the clock and drives the $\overline{\text{CLKRUN}}$ signal line according to the clocking protocol. The $\overline{\text{CLKRUN}}$ driver for the central resource requires high- and low-drive capability.
- The master interprets the clocking protocol and drives the $\overline{\text{CLKRUN}}$ signal low to request a clock running state for the purpose of receiving ownership of the bus and asserting the REQ signal. Since the master requires only low-drive capability, the $\overline{\text{CLKRUN}}$ driver for this agent is an open-drain output.
- The target drives the $\overline{\text{CLKRUN}}$ signal low to request the clock running state for a certain time. Like the master, the target requires only open-drain output on the $\overline{\text{CLKRUN}}$ signal.

Figure 3 illustrates the clock-run ($\overline{\text{CLKRUN}}$) protocol routing example for a PCI1131 bridge implementation. The clock-control protocol is implemented on the primary PCI bus interface using PCI clock (PCLK) and $\overline{\text{CLKRUN}}$ signals, and on the secondary CardBus interface using A_CCLK and B_CCLK signals.

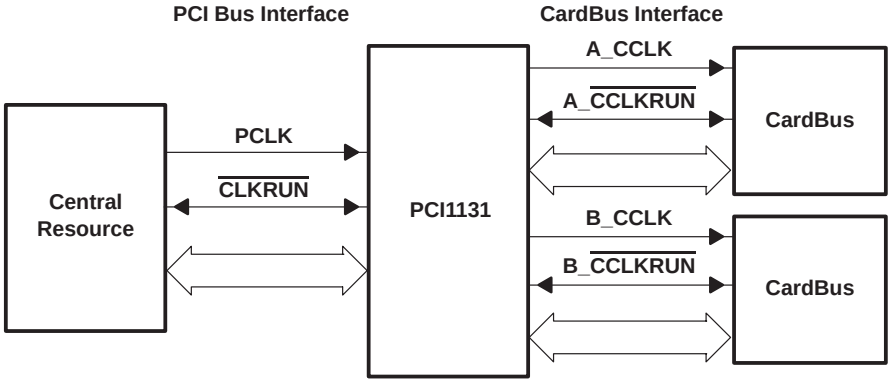
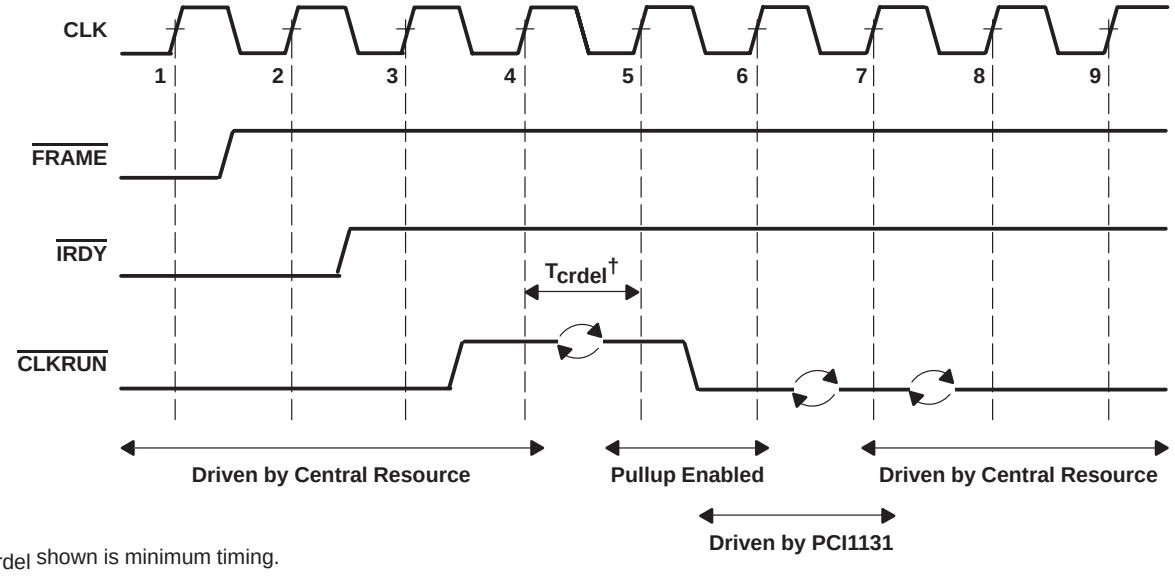



**Figure 3. PCI1131 Clock-Routing Example**

## 3.1 PCI Bus $\overline{\text{CLKRUN}}$

The PCI1131 does not perform the central resource function on the primary bus. Instead, it acts as a mastering agent. The mastering agent performs the functions of maintaining the clock during a clock-stop request from the central resource and restarting the clock when the central resource stops the clock.

To maintain the primary PCI clock (see Figure 4), the PCI1131 drives the $\overline{\text{CLKRUN}}$ signal low after it is detected as high for two clock cycles. For example, in the scenario where the central resource requests a clock stop while the PCI1131 state machine is still busy, the $\overline{\text{CLKRUN}}$ signal is driven low within a time window of $T_{crdel}$ as specified in the protocol. The maximum timing allowed for $T_{crdel}$ is two clock cycles. This ensures that the PCI1131 internal processes are completed without interrupting the clock.




† $T_{crdel}$ shown is minimum timing.

**Figure 4. Maintaining the Clock**

Figure 5 illustrates the request from the PCI1131 to restart the primary PCI clock. The CardBus controller asynchronously drives the $\overline{\text{CLKRUN}}$ signal low and it is held low until two rising edges of CLK are detected. For example, if during a clock-stop condition, a CardBus card arbitrates for the secondary bus by restarting the CCLK and using $\overline{\text{CREQ}}$, then $\overline{\text{CLKRUN}}$ on the primary bus is driven low by the PCI1131 to restart the PCI clock.

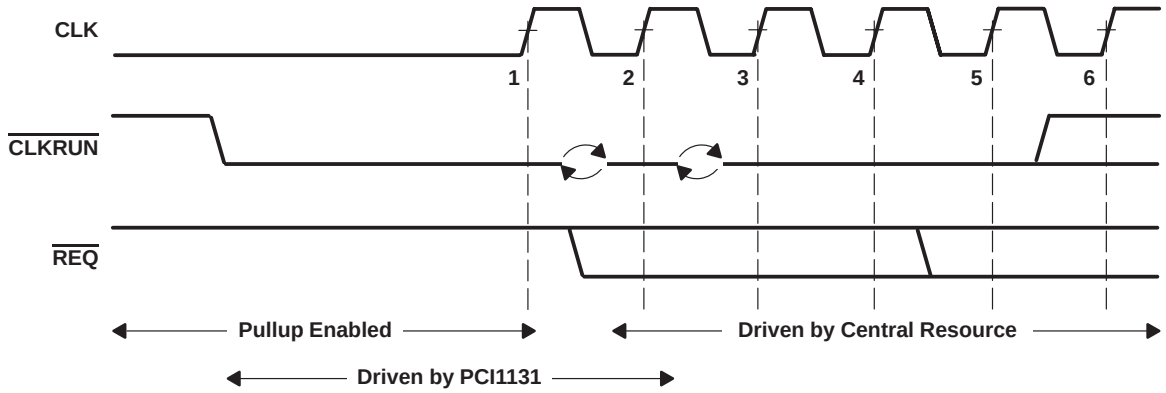



**Figure 5. Clock-Start Request**

## 3.2 CardBus CLKRUN

The PCI1131 CardBus controller contains the central resource function for the secondary bus. The PCI1131 drives the CLKRUN signal (A_CLKRUN, B_CLKRUN) low during normal operation. During bus idle periods, the PCI1131 determines that the secondary bus clock can be stopped. It then synchronously drives the CLKRUN signal high for one PCI clock, then sets the driver to a high-impedance state. After CLKRUN is deasserted, the clock continues to run for a minimum of four clock cycles. Figure 6 illustrates this scenario. If no requests for maintaining the clock are detected from the PC Cards, the clock can be stopped.

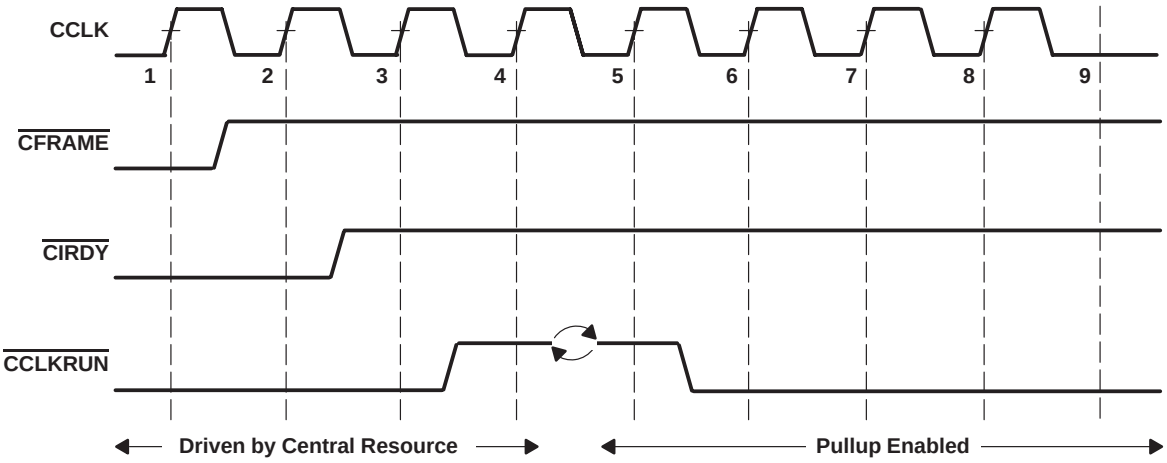



**Figure 6. Clock-Stop Request**

By using the CLKRUN protocol to stop the clock during periods of inactivity and by eliminating any unnecessary power consumption, dramatic power savings can be obtained in mobile computer designs. For systems implementing the CLKRUN protocol, the power consumption is a direct function of bus utilization time. This means that if the bus is used 40 percent of the time, the power consumption is reduced to 40 percent of the original power.

# 4 The PCI1131 CardBus Controller

The $\overline{\text{CLKRUN}}$ signal can be used only if all the master devices on the PCI bus participate in the clock-run protocol. Since many legacy devices do not implement this protocol, alternate methods of power savings must be considered and TI has developed its own power-saving methods.

As shown in Figure 7, TI designed the PCI1131 with aggressive goals for power dissipation. Through proprietary circuit design, the PCI1131 reduces the power consumption in the CardBus mode operation by 40 percent over the previous generation controller without sacrificing the benchmark performance of the PCI1130.

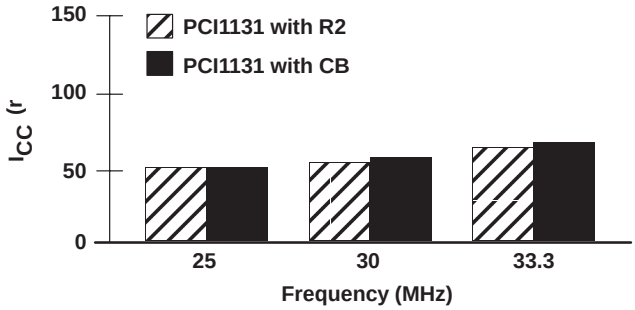



**Figure 7. Supply Current Versus Frequency**

If all of the components in the PCMCIA subsystem support the $\overline{\text{CLKRUN}}$ protocol, further power savings for the PCI1131 can be accomplished using this protocol to dynamically control the clock. Figure 7 shows that the PCI1131 consumes 76 mA with a free-running clock at 33 MHz. In the typical case where the bus is utilized by the PCI1131 for only 10 to 20 percent of the time, the system designer can take advantage of the clock-stop request during inactive periods and reduce the PCI1131 power consumption to 7–14 mA. Thus, the PCI1131 responds to the demands of the system by delivering world-class performance when required, but reducing power consumption to very low levels during idle periods between PC Card cycles.

Further, even in the case where the PCI bus does not support $\overline{\text{CLKRUN}}$, the PCI1131 CardBus controller can be enabled to use $\overline{\text{CLKRUN}}$ independently on the PC Card. In the case of transactions from the PCI target, the PC Card automatically restarts the board clock. Also, if the PC Card cannot handle the clock-stop condition, the PCI1131 saves power by slowing the secondary clock to divide by 16, and automatically restores the clock to normal clock frequency when a transaction is initiated from either interface.

# 5 Summary

Dramatic power savings can be realized when PCI $\overline{\text{CLKRUN}}$ is implemented in a mobile system. The TI PCI1131 provides this power saving feature, but proprietary power-saving techniques are implemented in the device to further reduce power consumption. Future TI CardBus controller products will continue this aggressive power reduction features.

Opportunities for further reductions in power consumption will come from several sources. The greatest benefit will be realized with improved PC Card power management. The PC Card16, and particularly CardBus cards designed with advanced power-management features, will soon enter the market. Further improvements in the TI CardBus controller family will come, as well, through advanced CMOS processes, innovative circuit design techniques, and by taking advantage of system-level initiatives such as OnNow™.

Operating system-directed power management (OSPM), soon to become a reality, opens up many opportunities for smarter power budgeting. Several industry initiatives are focused on achieving OSPM, such as the advanced configuration and power interface (ACPI) and the PCI Power-Management Working Group within the PCI Special Interest Group (SIG). TI has worked closely as a contributor and reviewer of both of these specifications, ensuring that these technologies are introduced quickly and effectively. TI intends to maintain its leadership position by driving these industry standards and introducing new products to support them.

OnNow is a trademark of Microsoft Corporation.

# 6 References


1. *1995 PC Card Standard*, PCMCIA, San Jose, Calif.
2. *PCMCIA Specification, Release 2.1*, PCMCIA, San Jose, Calif.
3. *Advanced Power Management (APM) Specification*, Intel and Microsoft
4. *PCI Mobile Design Guide, Revision 1.0*, PCI SIG. Portland, Ore.