HPC3130 PCI Hot Plug Controller User's Guide

Evaluation Module

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Read This First

About This Manual

This manual is provided to assist the platform developer in designing the HPC3130 in a system which incorporates hot-pluggable PCI slots.

Related Documentation From Texas Instruments

HPC3130 PCI Hot Plug Controller Hardware Data Sheet

HPC3130 PCI Hot Plug Controller Hardware Implementation Guide

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Contents

Tables

Chapter 1

Introduction

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1.1 Introduction

The HPC3130 EVM board has three 32-bit slots of which two are hot-plugable. All three slots reside behind a PCI-to-PCI bridge (the Texas Instruments PCI2031). The two hot-plugable slots are isolated using eight 16-bit bus isolation switches (CBT16244) and two 1-bit isolation switches (CBT1G125). The power to the hot-plugable slots is controlled by using one of the two power switches available on the EVM board. All communication with the HPC3130 is done using two of the PCI2031's general-purpose I/Os (GPIOs). One of the GPIOs is used for the SCLK and the other GPIO is used for SDA.

Chapter 2

HPC3130 Feature Set

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2.1 HPC3130 Feature Set

The HPC3130 provides the following features:

- ❑ PCI Hot Plug Specification, Revision 1.0 compliant
- ❑ Up to four independently controlled hot plug slots
- ❑ Register accessing through both generic parallel bus and two-wire serial interface
- ❑ Interrupt and event status/enable compliant with ACPI Specification 1.0
- ❑ An automatic bus connection sequencing feature
- ❑ 66 MHz PCI clock frequency
- ❑ Two attention indicators with variable LED blinking rates per slot
- ❑ An easy scheme to cascade the HPC3130 for CompactPCI applications
- ❑ Card detection mechanism independent of PCI present signals for advanced card protection
- ❑ Path to guarantee idle state during PCI bus connections
- ❑ A CBT switch control feature for REQ64# implementation
- ❑ 120-pin QFP package
- ❑ 128-pin TQFP package

Chapter 3

Hot-Plugable Slots

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3.1 Hot-Plugable Slots

The EVM board has two 32-bit hot-plugable slots, P3 and P4. Slot P3 is located on the back side of the board and slot P4 is located on the front side of the board. Because only two hot-plug slots are implemented on the board, two of the four functions on the HPC3130 are not used. By default, function 0 and 1 is used. Function 0 is used to control slot P3, and function 1 is used to control slot P4. If functions 2 and 3 need to be used instead of 0 and 1, the resistors for the appropriate slots must be removed and installed as outlined in Table 3–1. Never have both functions 0 and 2 or functions 1 and 3 installed at the same time.

Table 3–1. Resistors for Each Function

HPC3130 Function	Resistors Needed to be Installed
0	R81 – R90 (Installed by default)
1	R91 – R100 (Installed by default)
2	R101 – R110
3	R111 – R120

Chapter 4

Communicating with the HPC3130

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4.1 Communicating with the HPC3130

The only way to communicate with the HPC3130 on the EVM board is through the serial interface. The clock signal for the serial interface is connected to S_GPIO0 on the PCI2031 through J8, and the data signal for the serial interface is connected to S_GPIO1 on the PCI2031 through J7. If another I2C or SMBus master is available, the SCL and SDA signals from the master can be connected to J8 and J7, but make sure that you cut the trace underneath the jumpers.

In order to communicate with the HPC3130, the software must toggle the GPIOs so that the signals mimic the serial interface described in the HPC3130 datasheet. Texas Instruments provides with your EVM two diagnostic programs that communicate with the HPC3130 by toggling the GPIOs. One of these programs functions only under DOS, while the other program functions under Windows 95 and Windows NT for x86 architectures.

By default, the EVM board is set up so that the HPC3130 address is at A0h. To change the address of the HPC3130, toggle the appropriate DIP on U10. Table 4–1 shows the default settings of U10.

Table 4–1. Default Setting for U10

Pin #	Signal Name	Default Setting
1	ADD0	0
2	ADD1	0
3	ADD2	0
4	ADD3	0
5	ADD4	1
6	ADD5	0
7	ADD6	1
8	SMODE	1
9	DETECT1#0	0
10	DETECT2#0	0

Chapter 5

Power Switches

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5.1 Power Switches

The HPC3130 EVM board has two power switch options. One option uses the HIP1011 by Harris Semiconductor. The other option uses the LTC1643 by Linear Technologies. Only one of these options will be installed on your EVM board. The following two tables indicate what components must be installed on the EVM for each power switch option.

Table 5–1. HIP1011 Option

Reference #	Part Name	Reference #	Part Name
U16	HIP1011	U22	HIP1011
U11	RF1K49211	U17	RF1K49211
U12	RF1K49211	U18	RF1K49211
U13	RF1K49211	U19	RF1K49211
U14	RF1K49211	U20	RF1K49211
U15	IRF7413	U21	IRF7413
R121	0.01 Ω	R126	0.01 Ω
R122	0.01 Ω	R127	0.01 Ω
R123	0.01 Ω	R128	0.01 Ω
R125	12.1 kΩ	R130	12.1 kΩ
C109	0.033 µF	C113	0.033 µF
C110	0.033 µF	C114	0.033 µF
C111	100 pF	C115	100 pF
C112	0.033 µF	C116	0.033 µF

Table 5–2. LTC1643 Option

Reference #	Part Name	Reference #	Part Name
U30	LTC1643	U33	LTC1643
U28	IRF7413	U31	IRF7413
U29	IRF7413	U32	IRF7413
U15	IRF7413	U21	IRF7413
R131	0.005 Ω	R138	0.005 Ω
R132	10 Ω	R139	0.005 Ω
R133	0.005 Ω	R140	10 Ω
R134	1 kΩ	R141	10 Ω
R136	10 Ω	R144	1 kΩ
R124	10 Ω	R129	10 Ω
C134	0.047 µF	C136	0.047 µF
C135	0.1 µF	C137	0.1 µF

Chapter 6

Power and Attention Indicators

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6.1 Power and Attention Indicators

Six LEDs are installed on your board. Table 6–1 depicts the purpose for each LED.

Table 6–1. LEDs

LED	Purpose
D1	Power indicator for socket P3
D2	Attention indicator (ATTN1) for socket P3
D3	Power indicator for socket P4
D4	Attention indicator (ATTN1) for socket P4
D5	Attention indicator (ATTN0) for socket P3
D6	Attention indicator (ATTN0) for socket P4

Chapter 7

Definition of Jumpers

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7.1 Definition of Jumpers

Table 7–1 describes the purpose of each jumper on the EVM board.

Table 7–1. Jumper Definitions

Jumper	Purpose
J1	Output of 3.3-V regulator (U2) provides power to U1 and U4. By default, this jumper is shorted.
J2	5-V input into U3. By default, this jumper is shorted.
J3	Provides power from an external supply to the EVM board. This connector provides both 5 V and 12 V.
J4	This jumper is used to switch 12 V from either the external power supply (J3) or the 12 V on the PCI connector (P1). By default, the J4 is set up to provide 12 V from the PCI connector.
J5	–12 V from the PCI connector (P1). By default, this jumper is shorted.
J6	Provides 3 V to the power switches.
J7	SDA for the serial interface. By default, this jumper is shorted.
J8	SCL for the serial interface. By default, this jumper is shorted.
J9	V_{CC} for the HPC3130. This jumper is used to measure the power consumed by the HPC3130 through the V_{CC} pins. By default, this jumper is shorted.
J10	V_{CCP} for the HPC3130. This jumper is used to measure the power consumed by the HPC3130 through the V_{CCP} pin. By default, this jumper is shorted.
J11	$V_{CC}5V$ for the HPC3130. This jumper is used to measure the power consumed by the HPC3130 through the $V_{CC}5V$ pins. By default, this jumper is shorted.
J12	INTR# interrupt from HPC3130
J13	INTR interrupt from HPC3130
J14	HP probe connector
J15	3.3 V for socket P3. By default, this jumper is shorted.
J16	3.3 V for socket P4. By default, this jumper is shorted.
J20	3.3 V from the PCI connector (P1). By default, this jumper is shorted.
J21	3.3 V from voltage regulator (U3).
J22	5 V from the PCI connector (P1). By default, this jumper is shorted.
J23	5 V from the external power supply (J3).

Table 7–2. Pin Definitions for J3

Pin	Description
1	5 V
2	GND
3	GND
4	12 V

Table 7–3. Pin Definitions for J14

Pin	Description	Pin	Description
1	No Connection	2	No Connection
3	Clock to HPC3130	4	IDLEGNT#
5	SYSM66EN	6	M66EN0
7	IDLEREQ#	8	REQ64ON#
9	SLOTREQ64# for socket P3	10	ATTN0 for socket P3
11	PWRON/OFF# for socket P3	12	PWRFAULT# for socket P3
13	PWRGOOD# for socket P3	14	PRSNT1# for socket P3
15	PRSNT2# for socket P3	16	SLOTRST# for socket P3
17	BUSON# for socket P3	18	CLKON# for socket P3
19	ATTN1 for socket P3	20	GND

Appendix A

Reference Schematic for the HPC3130 EVM

This appendix presents the schematic diagram for the 32-bit HPC3130PBK EVM.

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Figure A–1. HPC3130 EVM Schematic Diagram

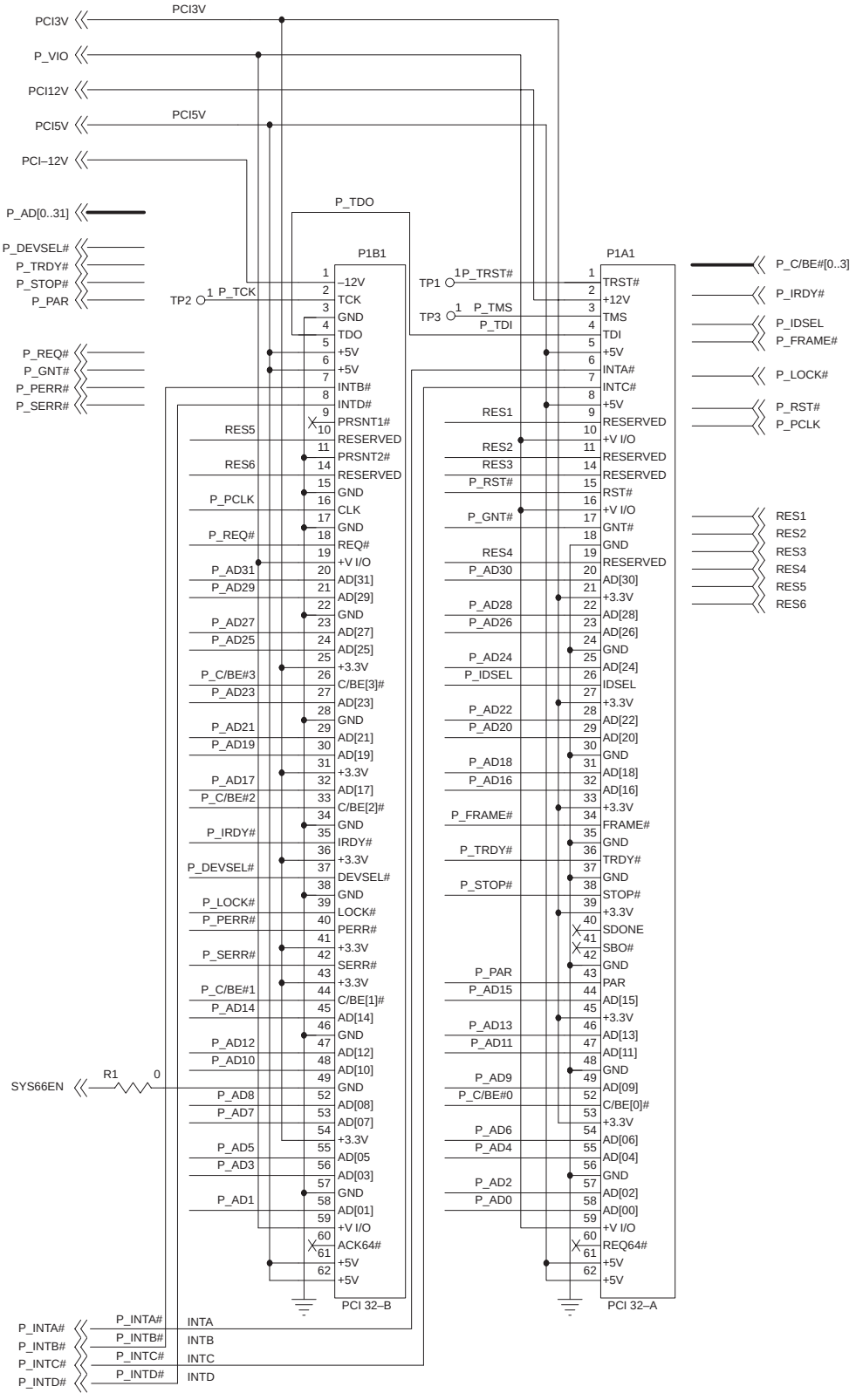
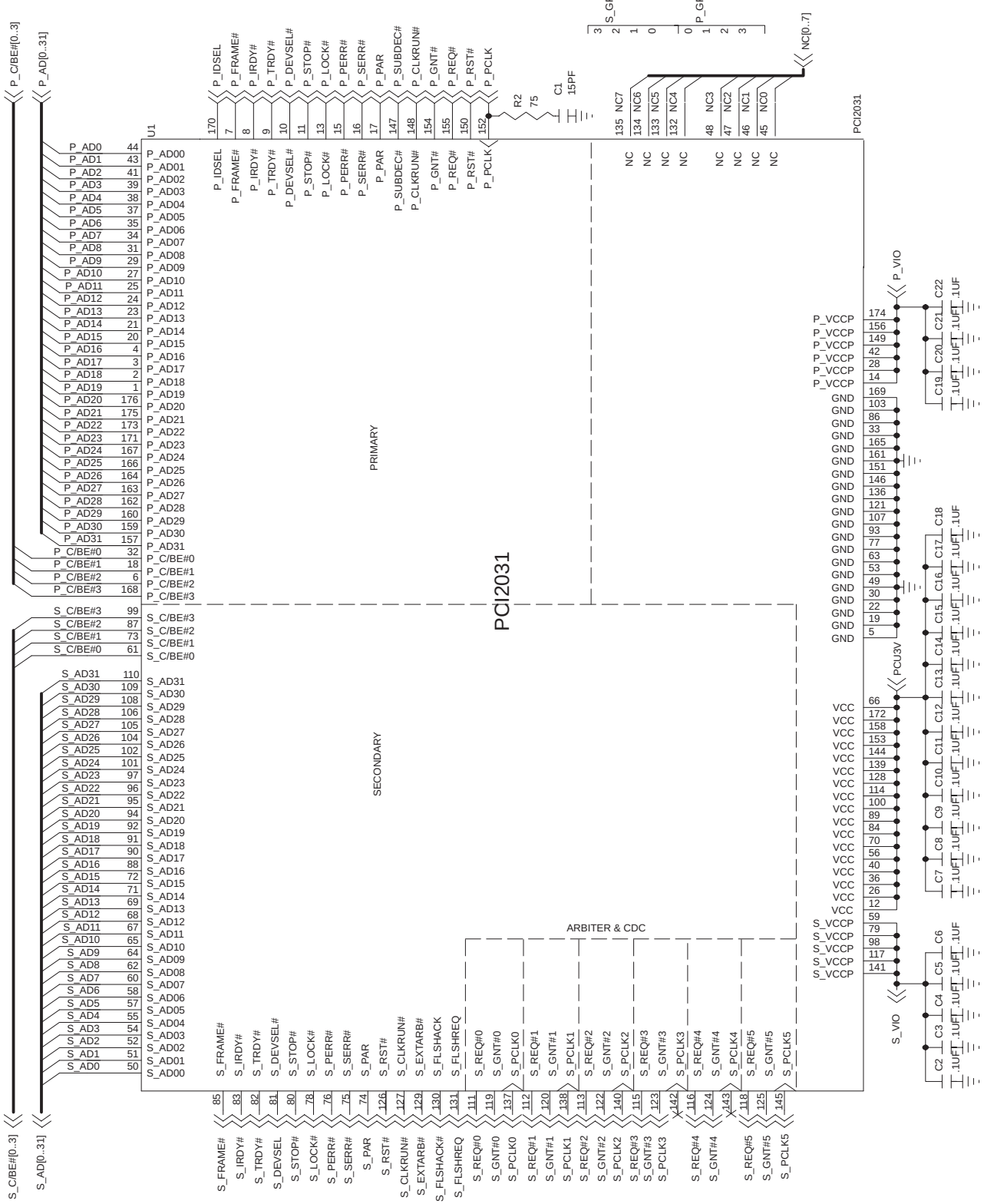


Figure A–1. HPC3130 EVM Schematic Diagram (Continued)



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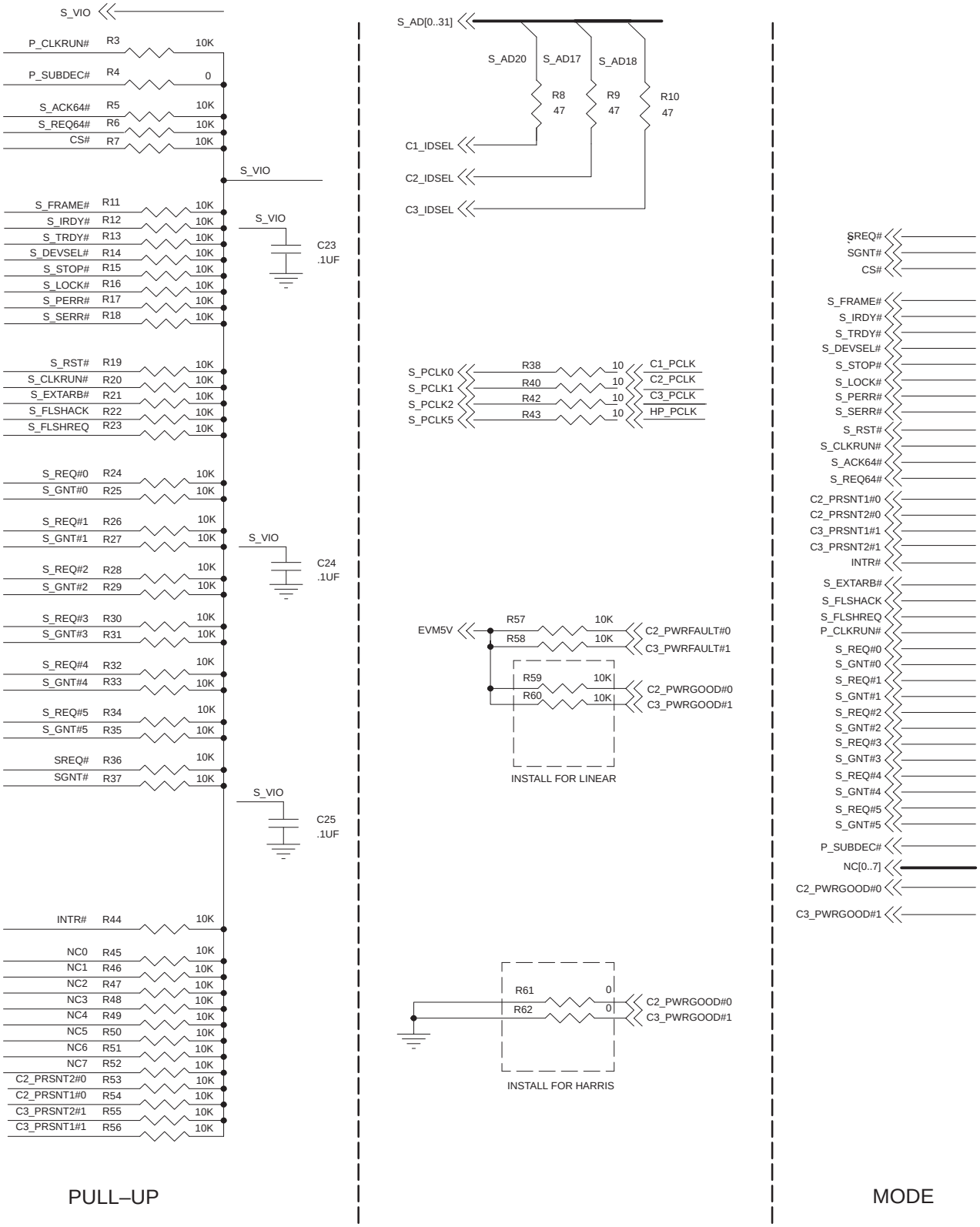

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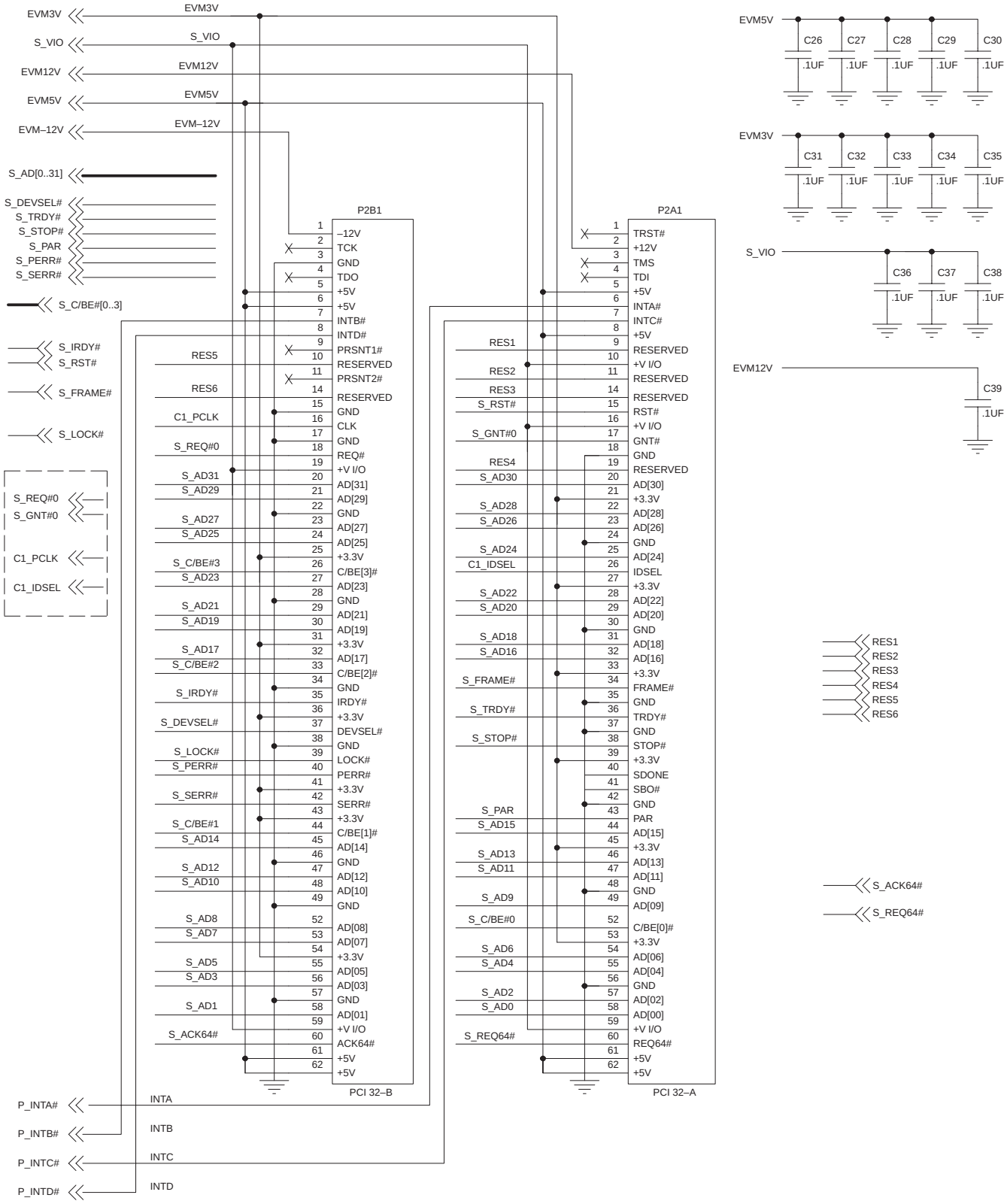

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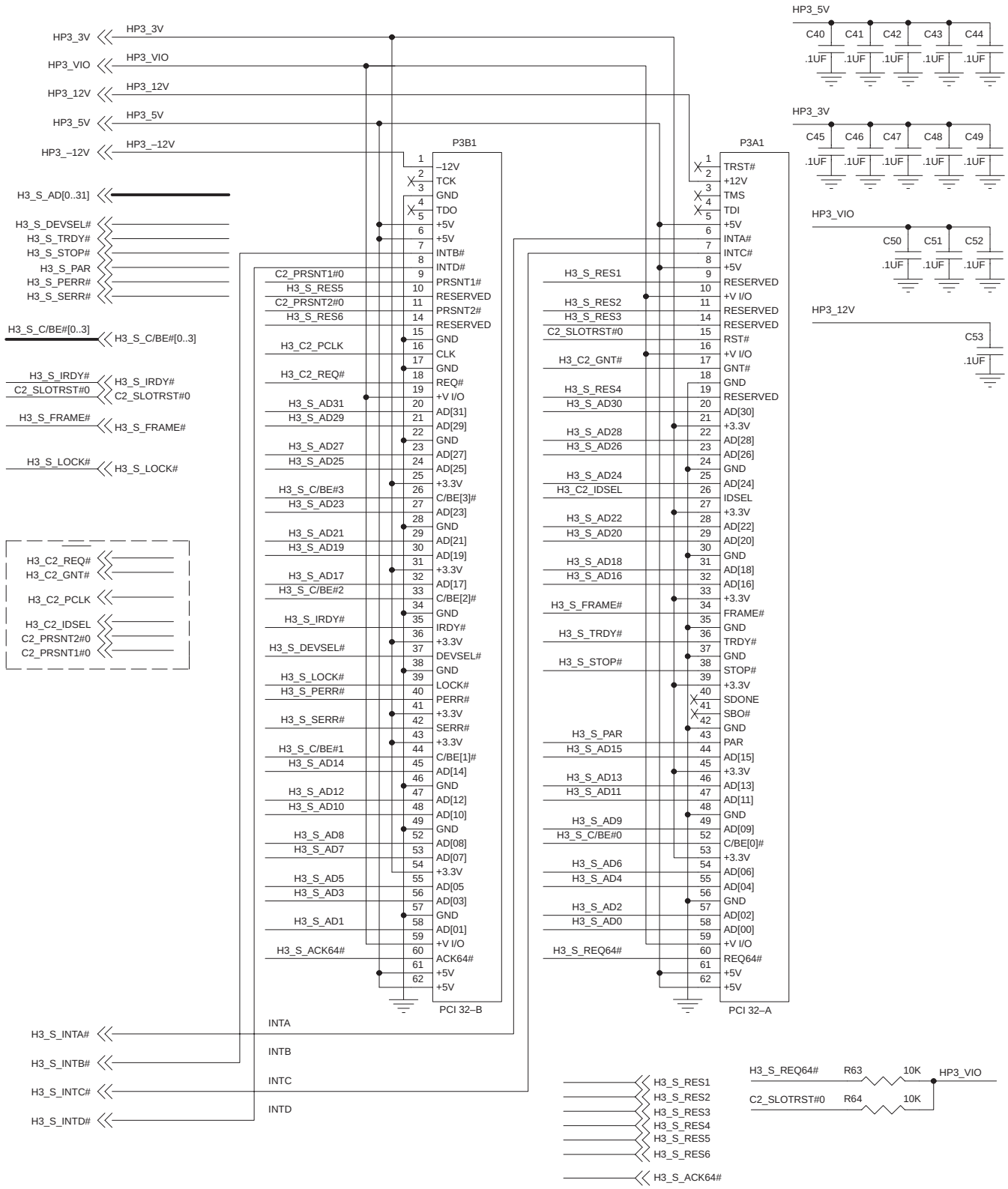

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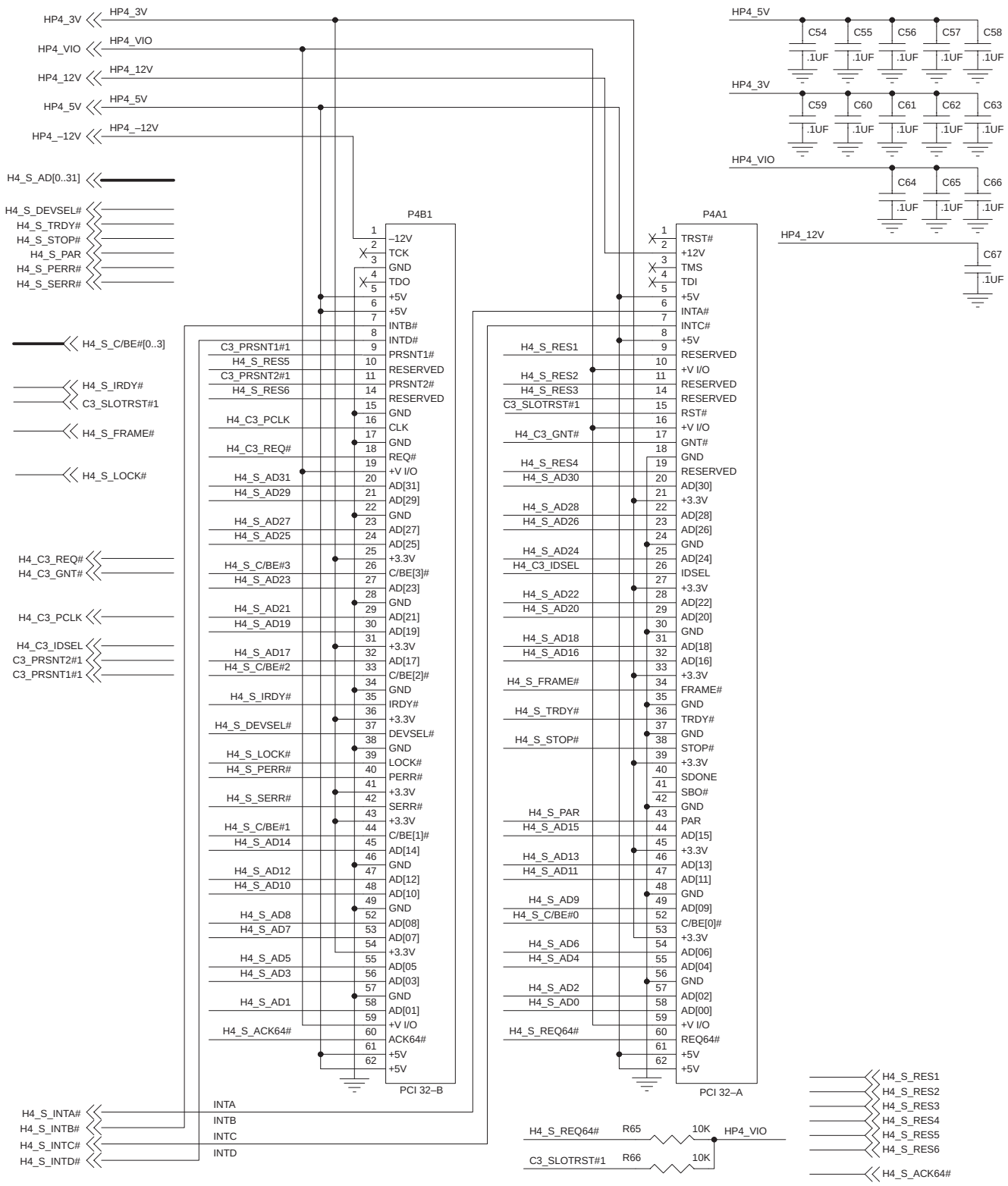

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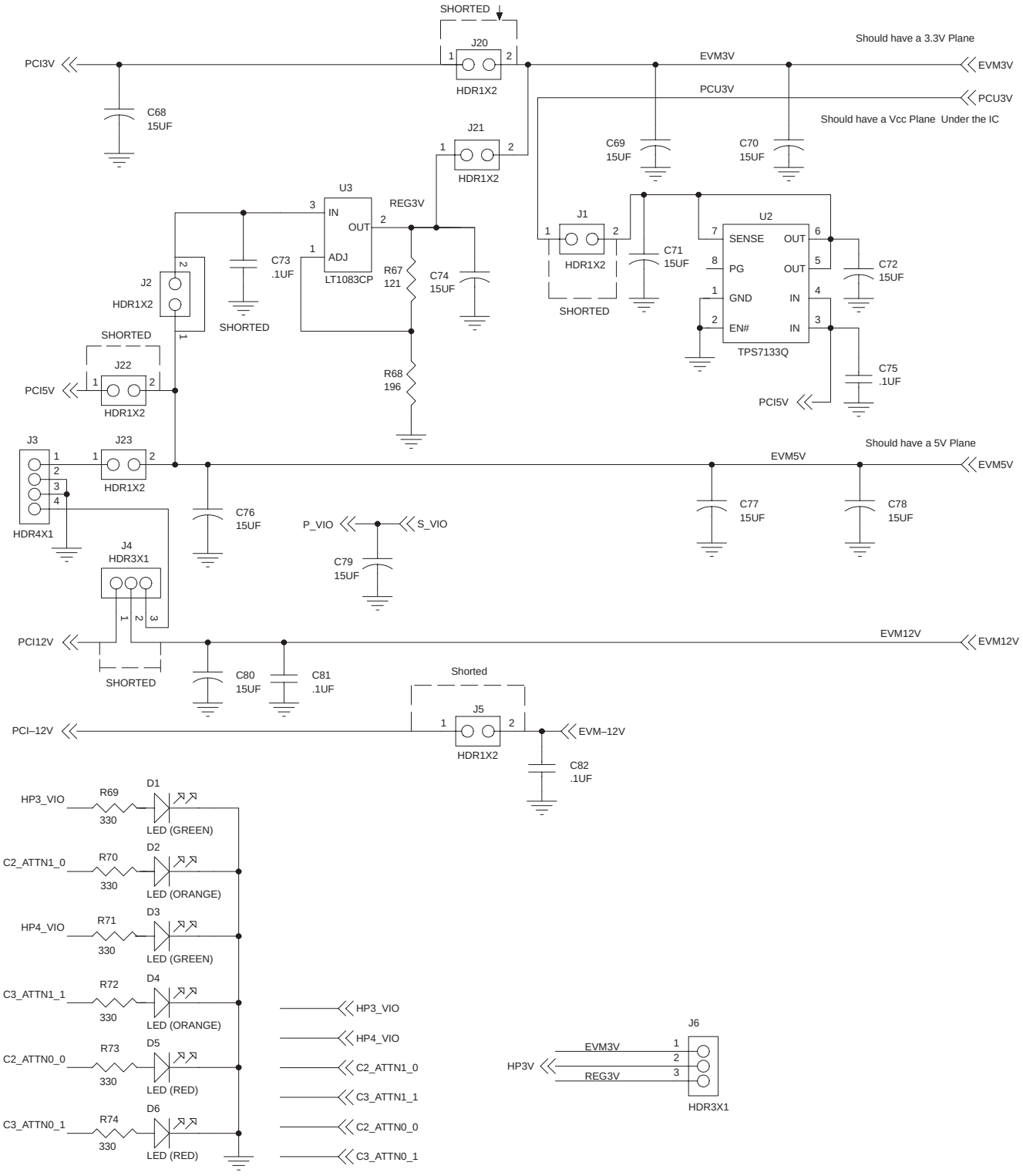

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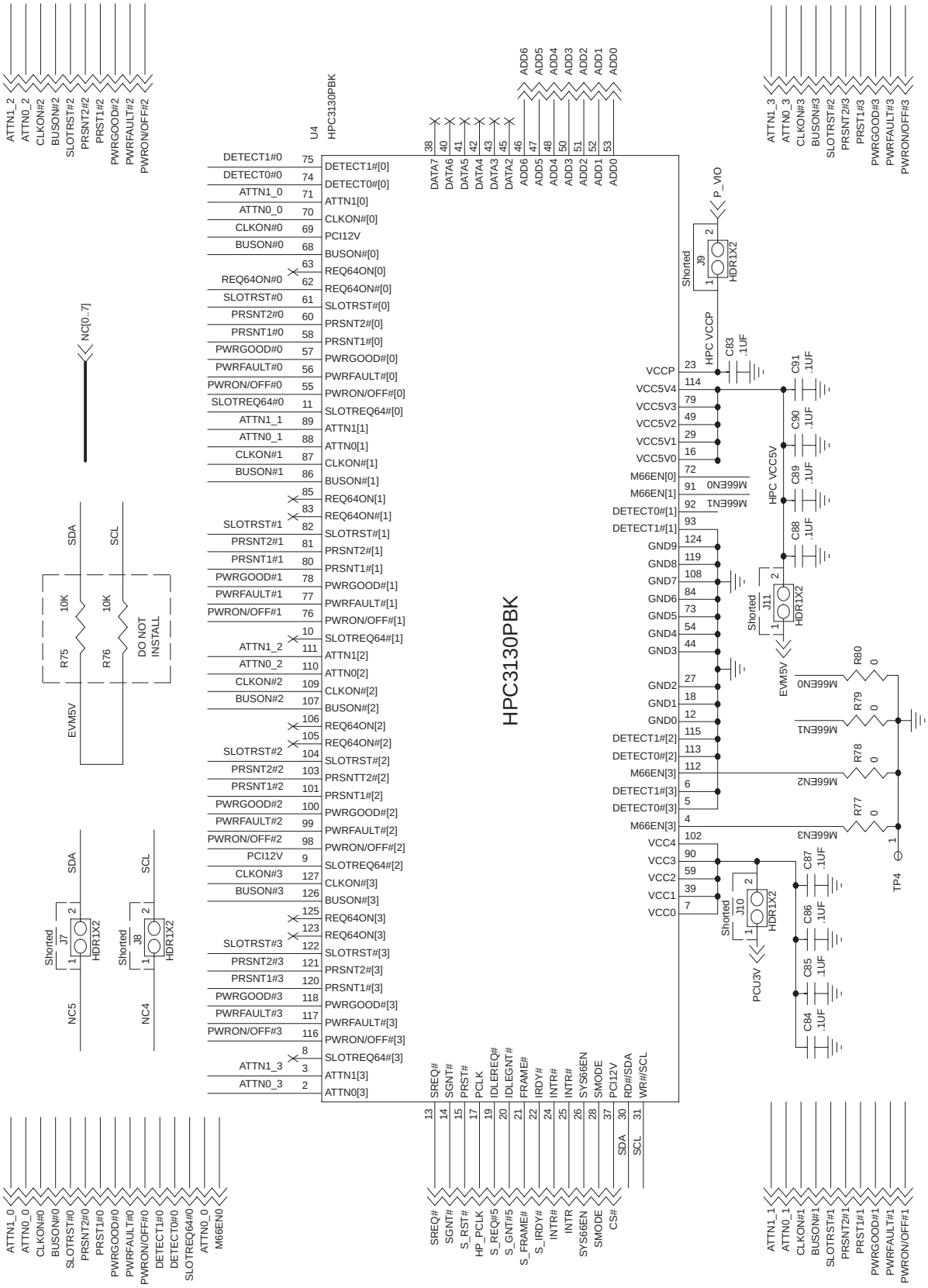

Figure A–1. HPC3130 EVM Schematic Diagram (Continued)

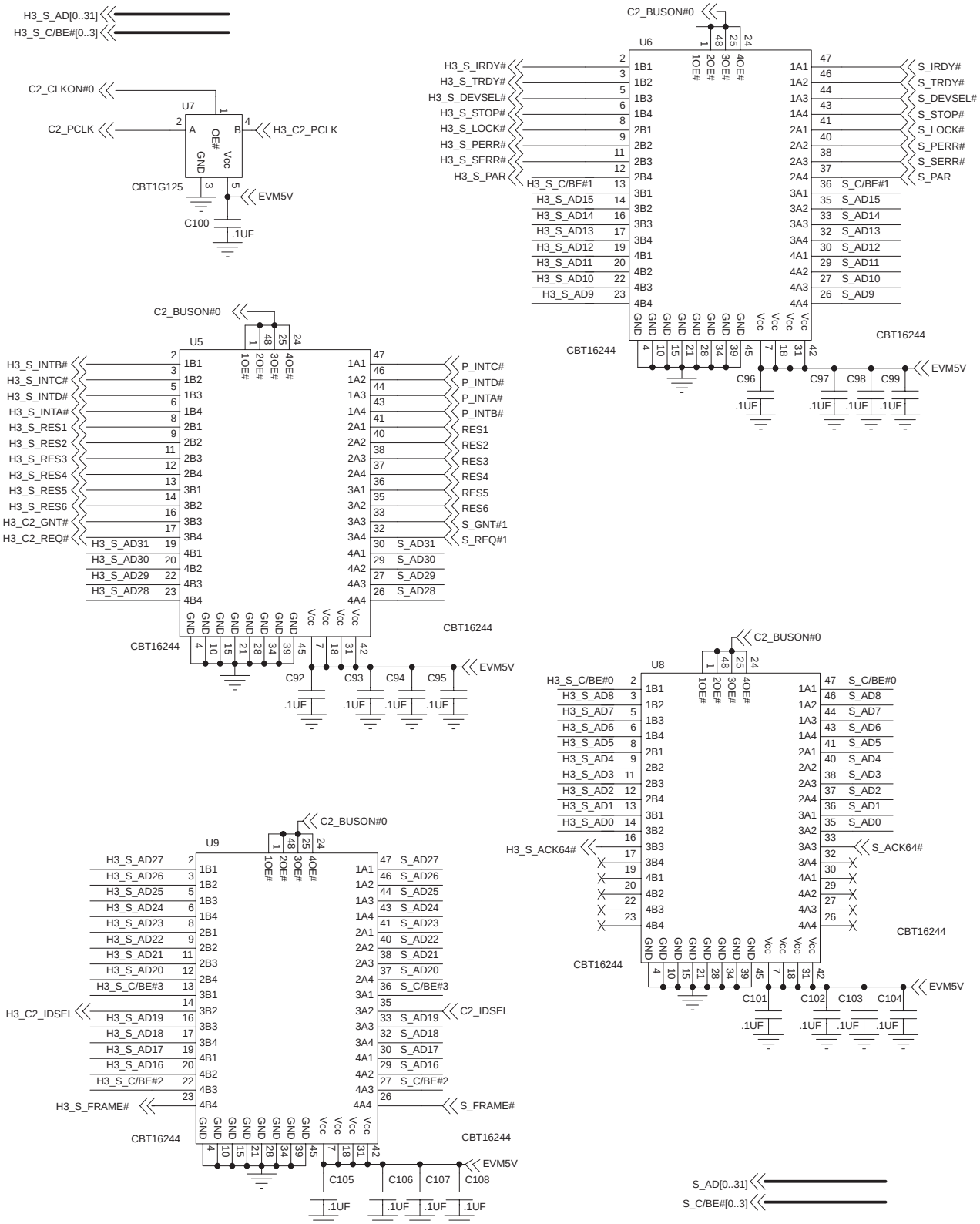

Figure A–1. HPC3130 EVM Schematic Diagram (Continued)

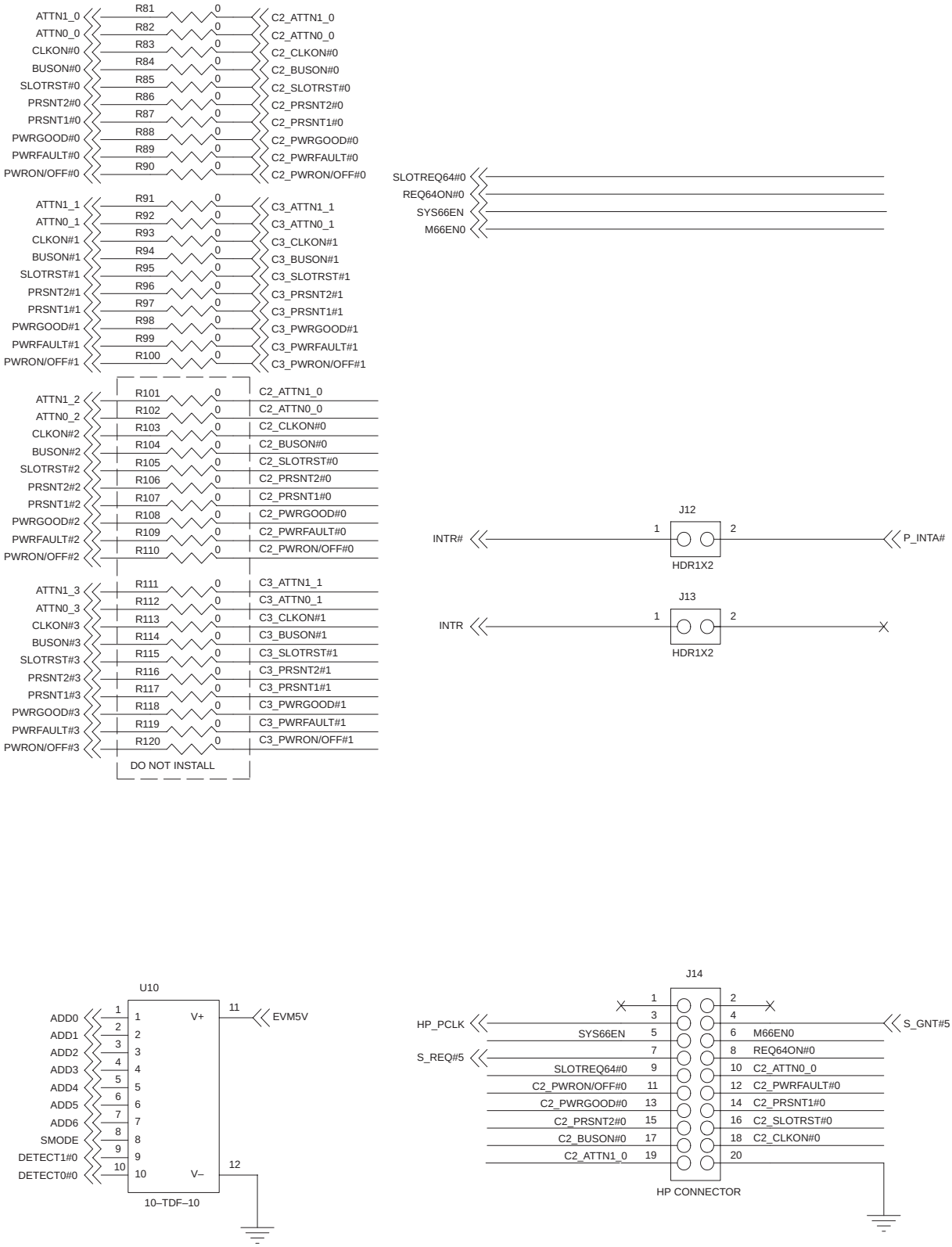

Figure A–1. HPC3130 EVM Schematic Diagram (Continued)

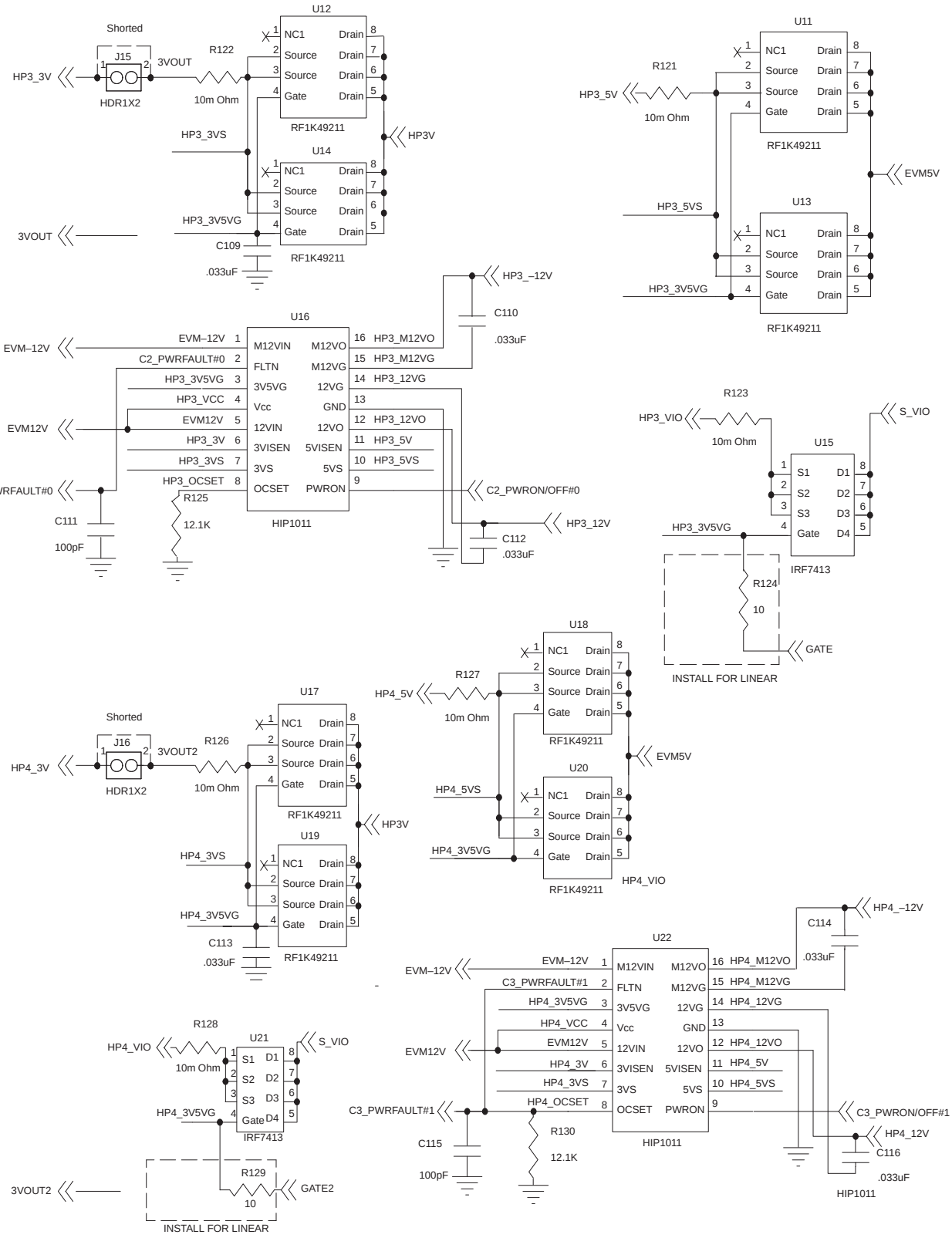

Figure A–1. HPC3130 EVM Schematic Diagram (Continued)

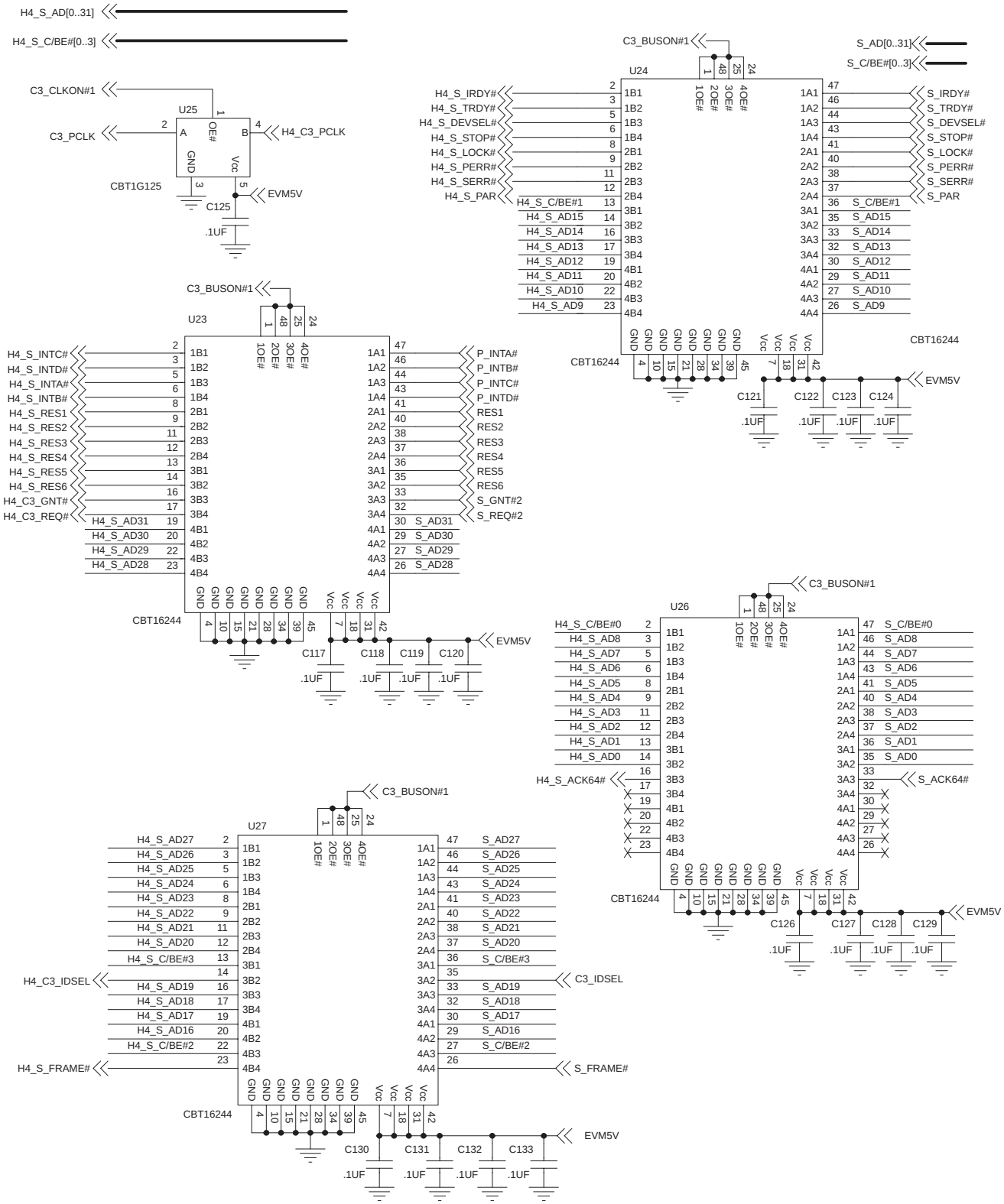

Figure A–1. HPC3130 EVM Schematic Diagram (Continued)