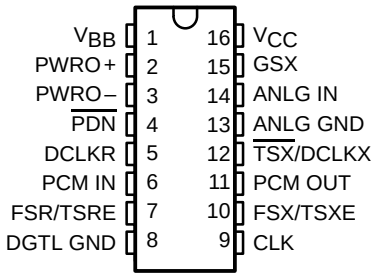
SCTS021D –AUGUST 1987 –REVISED OCTOBER 1996

- **Reliable Silicon-Gate CMOS Technology**
- **Low Power Consumption**
  - **Operating Mode . . . 80 mW**
  - **Power-Down Mode . . . 5 mW**
- **μ-Law Coding**
- **Excellent Power-Supply Rejection Ratio Over Frequency Range of 0 Hz to 50 kHz**
- **No External Components Needed for Sample, Hold, and Autozero Functions**
- **Precision Internal Voltage Reference**
- **Single Chip Contains A/D, D/A, and Associated Filters**

**DW OR N PACKAGE**
**(TOP VIEW)**




**FEATURES TABLE**

| |
|---|
| Number of Pins:<br>16 |
| Coding Law:<br>μ-Law |
| Variable Mode:<br>64 kHz to 2.048 MHz |
| Fixed Mode:<br>2.048 MHz (TCM29C18, TCM129C18),<br>1.536 MHz (TCM29C19, TCM129C19) |
| 8-Bit Resolution<br>12-Bit Dynamic Range |

## description

The TCM29C18, TCM29C19, TCM129C18, and TCM129C19 are low-cost single-chip PCM codecs (pulse-code-modulated encoders and decoders) and PCM line filters. These devices incorporate both the A/D and D/A functions, an antialiasing filter (A/D), and a smoothing filter (D/A). They are ideal for use with the TMS320 DSP family members, particularly those featuring a serial port such as the TMS32020, TMS32011, and TMS320C25.

Primary applications include:

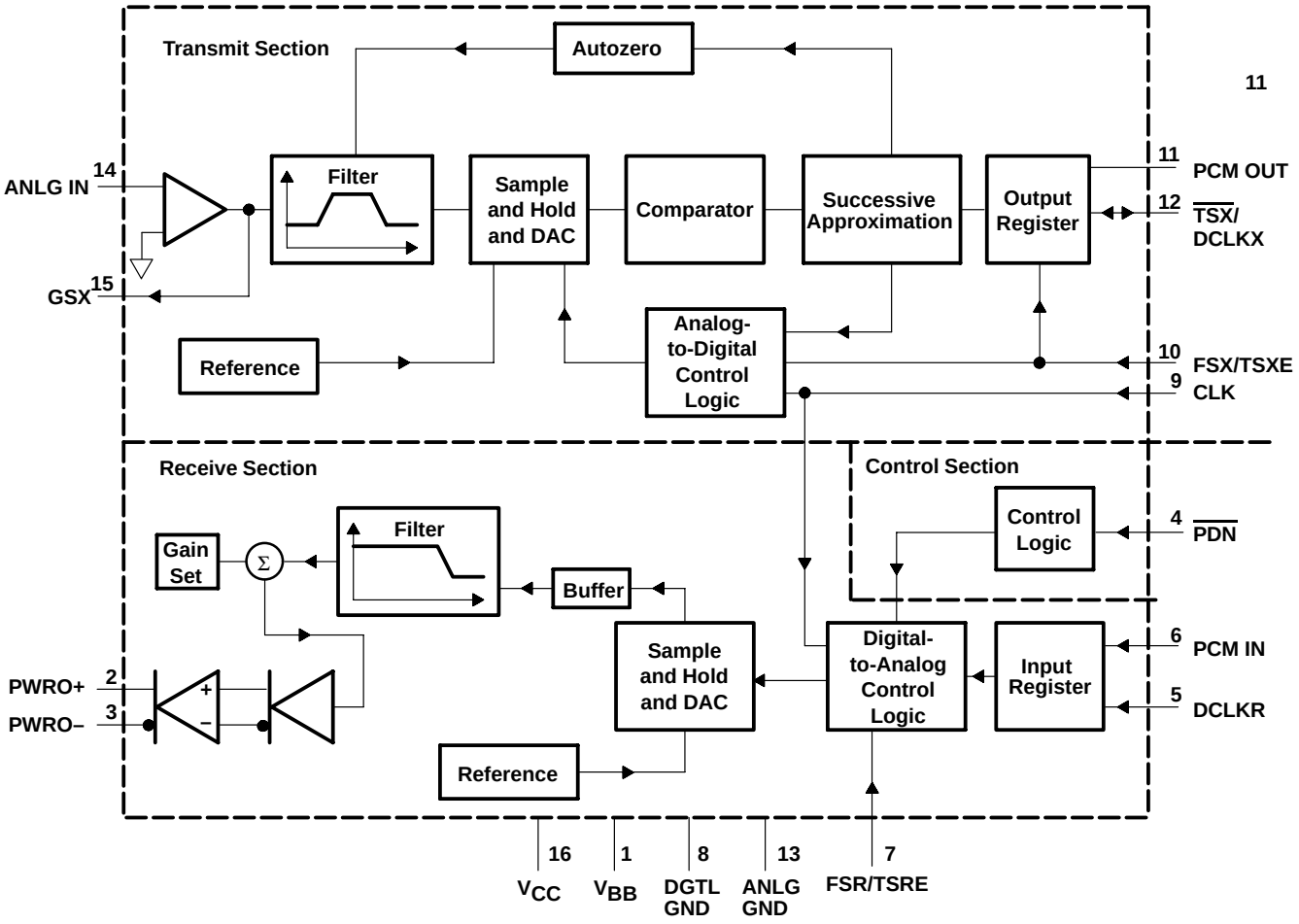
- Digital encryption systems
- Digital voice-band data storage systems
- Digital signal processing

These devices are designed to perform encoding of analog input signals (A/D conversion) and decoding of digital PCM signals (D/A conversion). They are useful for implementation in the analog interface of a digital signal processing system. Both devices also provide band-pass filtering of the analog signals prior to encoding, and smoothing after decoding.

The TCM29C18 and TCM29C19 are characterized for operation over the temperature range of 0°C to 70°C. The TCM129C18 and TCM129C19 are characterized for operation over the temperature range of –40°C to 85°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## functional block diagram



## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| ANLG IN | 14 | I | Inverting analog input to uncommitted transmit operational amplifier. |
| ANLG GND | 13 | | Analog ground return for all voice circuits. ANLG GND is internally connected to DGTL GND. |
| CLK | 9 | I | Master clock and data clock input for the fixed-data-rate mode. Master (filter) clock only for variable-data-rate mode. CLK is used for both the transmit and receive sections. |
| DCLKR | 5 | I | Fixed-data-rate mode — variable-data-rate mode select. When DCLKR is connected to $V_{BB}$, the device operates in the fixed-data-rate mode. When DCLKR is not connected to $V_{BB}$, the device operates in the variable-data-rate mode and DCLKR becomes the receive data clock, which operates at frequencies from 64 kHz to 2.048 MHz. |
| DGTL GND | 8 | | Digital ground for all internal logic circuits. DGTL GND is internally connected to ANLG GND. |
| FSR/TSRE | 7 | I | Frame-synchronization clock input/time-slot enable for the receive channel. In the variable-data-rate mode, this signal must remain high for the duration of the time slot. The receive channel enters the standby state when FSR is TTL low for 30 ms. |
| FSX/TSXE | 10 | I | Frame-synchronization clock input/time-slot enable for transmit channel. FSX/TSXE operates independently of, but in an analogous manner to FSR/TSRE. The transmit channel enters the standby state when FSX is low for 300 ms. |
| GSX | 15 | O | Output terminal of internal uncommitted operational amplifier. Internally, this is the voice signal input to the transmit filter. |
| PCM IN | 6 | I | Receive PCM input. PCM data is clocked in on eight consecutive negative transitions of the receive data clock, which is CLKR in fixed-data-rate timing and DCLKR in variable-data-rate timing. |
| PCM OUT | 11 | O | Transmit PCM output. PCM data is clocked out of pcm out on eight consecutive positive transition of the transmit data clock, which is CLKX in fixed-data-rate timing and DCLKX in variable-data-rate timing. |
| $\overline{\text{PDN}}$ | 4 | I | Power-down select. On the TCM29C18 and the TCM129C18, the device is inactive with a TTL low-level input and active with a TTL high-level input to the terminal. On the TCM29C19 and the TCM129C19, this terminal must be connected to a TTL high level. |
| PWRO+ | 2 | O | Noninverting output of power amplifier. PWRO+ can drive transformer hybrids or high-impedance loads directly in either a differential or single-ended configuration. |
| PWRO– | 3 | O | Inverting output of power amplifier. PWRO– is functionally identical to PWRO+. |
| $\overline{\text{TSX}}$/DCLKX | 12 | I/O | Transmit channel time-slot strobe (output) or data clock (input). In the fixed-data-rate mode, this is an open-drain output to be used as an enable signal for a 3-state buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock, which operates at TTL levels from 64 kHz to 2.048 MHz. |
| $V_{BB}$ | 1 | | Negative supply voltage. Input is –5 V ±5%. |
| $V_{CC}$ | 16 | | Positive supply voltage. Input is 5 V ±5%. |

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1) . . . . . –0.3 V to 15 V
Output voltage range, $V_O$ . . . . . –0.3 V to 15 V
Input voltage range, $V_I$ . . . . . –0.3 V to 15 V
Digital ground voltage range . . . . . –0.3 V to 15 V
Operating free-air temperature range, $T_A$: TCM29C18, TCM29C19 . . . . . 0°C to 70°C
TCM129C18, TCM129C19 . . . . . –40°C to 85°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values for maximum ratings are with respect to $V_{BB}$.

### recommended operating conditions (see Note 2)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage (see Note 3) | | 4.75 | 5 | 5.25 | V |
| $V_{BB}$ | Supply voltage | | –4.75 | –5 | –5.25 | V |
| | DGTL GND voltage with respect to ANLG GND | | | 0 | | V |
| $V_{IH}$ | High-level input voltage, all inputs except ANLG IN | | 2.2 | | | V |
| $V_{IL}$ | Low-level input voltage, all inputs except ANLG IN | | | | 0.8 | V |
| $V_{I(PP)}$ | Peak-to-peak analog input voltage (see Note 4) | | | | 4.2 | V |
| $R_L$ | Load resistance | GSX | 10 | | | kΩ |
| | | PWRO+ and/or PWRO– | 300 | | | Ω |
| $C_L$ | Load capacitance | GSX | | | 50 | pF |
| | | PWRO+ and/or PWRO– | | | 100 | |
| $T_A$ | Operating free-air temperature | TCM29C18 or TCM29C19 | 0 | | 70 | °C |
| | | TCM129C18 or TCM129C19 | –40 | | 85 | |

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up procedure described in the device power-up sequence paragraphs later in this document should be followed.
3. Voltages at analog inputs and outputs and $V_{CC}$ and $V_{BB}$ terminals are with respect to ANLG GND. All other voltages are referenced to DGTL GND unless otherwise noted.
4. Analog inputs signals that exceed 4.2 V peak to peak may contribute to clipping and preclude correct A/D conversion. The digital code representing values higher than 4.2 V is 10000000. For values more negative than 4.2 V, the code is 0000000.

### electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

#### supply current, $f_{DCLK}$ = 2.048 MHz, outputs not loaded

| PARAMETER | | | TEST CONDITIONS | TCM29Cxx | | TCM129Cxx | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| $I_{CC}$ | Supply current from $V_{CC}$ | Operating | | | 10 | | 14 | mA |
| | | Standby | FSX or FSR at $V_{IL}$ after 300 ms | | 1.2 | | 1.5 | |
| | | Power down | $\overline{PDN}$ at $V_{IL}$ after 10 μs | | 1 | | 1.2 | |
| $I_{BB}$ | Supply current from $V_{BB}$ | Operating | | | –10 | | –14 | mA |
| | | Standby | FSX or FSR at $V_{IL}$ after 300 ms | | –1.2 | | –1.5 | |
| | | Power down | $\overline{PDN}$ at $V_{IL}$ after 10 μs | | –1 | | –1.2 | |

### ground terminals

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| DC resistance between ANLG GND and DGTL GND | | | 34 | | Ω |

### digital interface

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage at PCM OUT | $I_{OH}$ = –9.6 mA | 2.4 | | | V |
| | | $I_{OH}$ = –0.1 mA | 3.5 | | | |
| $V_{OL}$ | Low-level output voltage at $\overline{TSX}$ | $I_{OL}$ = 3.2 mA | | | 0.5 | V |
| $I_{IH}$ | High-level input current, any digital input | $V_I$ = 2.2 V to $V_{CC}$ | | | 12 | µA |
| $I_{IL}$ | Low-level input current, any digital input | $V_I$ = 0 to 0.8 V | | | 12 | µA |
| $C_i$ | Input capacitance | | | 5 | 10 | pF |
| $C_o$ | Output capacitance | | | 5 | | pF |

† All typical values are at $V_{BB}$ = –5 V, $V_{CC}$ = 5 V, and $T_A$ = 25°C.

### transmit side (A/D) characteristics

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| Input offset voltage at ANLG IN | $V_I$ = –2.17 V to 2.17 V | | | | ±25 | mV |
| Input offset current at ANLG IN | $V_I$ = –2.17 V to 2.17 V | | | 1 | | pA |
| Input bias current | $V_I$ = –2.17 V to 2.17 V | | | | ±100 | nA |
| Open-loop voltage amplification at GSX | | | 5000 | | | |
| Unity-gain bandwidth at GSX | | | | 1 | | MHz |
| Input resistance at ANLG IN | | | 10 | | | MΩ |
| Gain-tracking error with sinusoidal input (see Notes 5, 6, and 7) | –3 ≥ dBm0 input level ≥ –40 dBm0, | Ref level = –10 dBm0 | | | ±0.5 | dB |
| | –40 > dBm0 input level ≥ –50 dBm0, | Ref level = –10 dBm0 | | | ±25 | |
| Transmit gain tolerance | $V_I$ = 1.06 V, | f = 1.02 kHz | 0.95 | | 1.19 | Vrms |
| Noise | Ref max output level: 200 Hz to 3 kHz | | | | –70 | dB |
| Supply-voltage rejection ratio, $V_{CC}$ to $V_{BB}$ | f = 0 Hz to 30-kHz (measured at PCM OUT) idle channel, Supply signal = 200 mV peak to peak | | –20 | | | dB |
| Crosstalk attenuation, transmit to receive (single ended) | ANLG IN = 0 dBm, PCM IN = lowest decode level, | f = 1-kHz, unity gain, Measured at PWRO+ | 62 | | | dB |
| Signal-to-distortion ratio, sinusoidal input (see Note 8) | 0 dBm0 ≥ ANLG IN ≥ –30 dBm0 | | 33 | | | dB |
| | –30 dBm0 > ANLG IN ≥ –40 dBm0 | | 27 | | | |
| | –40 dBm0 > ANLG IN ≥ –45 dBm0 | | 22 | | | |
| Absolute delay time to PCM OUT | Fixed-data rate, Input to ANLG IN = 1 kHz at 0 dB | $f_{CLKX}$ = 2.048 MHz, | | 245 | | µs |

† All typical values are at $V_{BB}$ = –5 V, $V_{CC}$ = 5 V, and $T_A$ = 25°C.

NOTES: 5. Unless otherwise noted, the analog input is a 0-dBm0, 1020-Hz sine wave, where 0 dBm0 is defined as the zero-reference point of the channel under test. This corresponds to an analog signal input of 1.064 Vrms or an output of 1.503 Vrms.

6. The input amplifier is set for unity gain. The digital input is a PCM bit stream generated by passing a 0-dBm0, 1020-Hz sine wave through an ideal encoder.
7. The TCM29C18, TCM29C19, TCM129C18, and TCM129C19 are internally connected to set PWRO+ and PWRO– to 0 dBM. All output levels are (sin x)/x corrected.
8. CCITT G.712 – Method 2

### receive side (D/A) characteristics (see Note 9)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| Output offset voltage PWRO+ and PWRO– (single ended) | Relative to ANLG GND | | | | ±200 | mV |
| Output resistance at PWRO+ and PWRO– | | | | 1 | 2 | Ω |
| Gain-tracking error with sinusoidal input (see Notes 5, 6, and 7) | –3 dBm0 ≥ input level ≥ –40 dBm0, | Ref level = –10 dBm0 | | | ±0.5 | dB |
| | –40 dBm0 > input level ≥ –50 dBm0, | Ref level = –10 dBm0 | | | ±25 | |
| Receive gain tolerance | $V_I$ = 1.06 V, | f = 1.02 kHz | 1.34 | | 1.69 | Vrms |
| Noise | Ref max output level: 200 Hz to 3 kHz | | | | –70 | dB |
| Supply voltage rejection ratio, $V_{CC}$ to $V_{BB}$ (single-ended) | f = 0 Hz to 30-kHz,<br>Supply signal = 200 mV peak to peak,<br>Frequency at PWRO+ | Idle channel,<br>Narrow band, | –20 | | | dB |
| Crosstalk attenuation, receive to transmit (single ended) | PCM IN = 0 dB,<br>Frequency = 1 kHz at PCM OUT | | 60 | | | dB |
| Signal-to-distortion ratio, sinusoidal input (see Note 8) | 0 dBm0 ≥ ANLG IN ≥ –30 dBm0 | | 33 | | | dB |
| | –30 dBm0 > ANLG IN ≥ –40 dBm0 | | 27 | | | |
| | –40 dBm0 > ANLG IN ≥ –45 dBm0 | | 22 | | | |
| Absolute delay time to PWRO+ | Fixed data rate, | $f_{CLKX}$ = 2.048 MHz | | 190 | | µs |

† All typical values are at $V_{BB}$ = –5 V, $V_{CC}$ = 5 V, and $T_A$ = 25°C.

NOTES: 5. Unless otherwise noted, the analog input is a 0-dBm0, 1020-Hz sine wave, where 0 dBm0 is defined as the zero-reference point of the channel under test. This corresponds to an analog signal input of 1.064 Vrms or an output of 1.503 Vrms.
6. The input amplifier is set for unity gain. The digital input is a PCM bit stream generated by passing a 0-dBm0, 1020-Hz sine wave through an ideal encoder.
7. The TCM29C18, TCM29C19, TCM129C18, and TCM129C19 are internally connected to set PWRO+ and PWRO– to 0 dBM. All output levels are (sin x)/x corrected.
8. CCITT G.712 – Method 2
9. The receive side (D/A) characteristics are referenced to a 600-Ω termination.

## timing requirements

### clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 3 and 4)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{c(CLK)}$ | Clock period for CLK (2.048-MHz systems) | 488 | | | ns |
| $t_r$, $t_f$ | Rise and fall times for CLK | 5 | | 30 | ns |
| $t_{w(CLK)}$ | Pulse duration for CLK | 220 | | | ns |
| $t_{w(DCLK)}$ | Pulse duration, DCLK ($f_{DCLK}$ = 64 kHz to 2.048 MHz) | 220 | | | ns |
| | Clock duty cycle, $[t_{w(CLK)}/t_{c(CLK)}]$ for CLK | 45% | 50% | 55% | |

### transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 3)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{d(FSX)}$ | Frame-sync delay time | 100 | $t_{c(CLK)}$ – 100 | ns |

### receive timing requirements over recommended ranges of supply voltages and operating free-air temperature, fixed-data-rate mode (see Figure 4)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{d(FSR)}$ | Frame-sync delay time | 100 | $t_{c(CLK)}$–100 | ns |

### transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 5)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{d(TSDX)}$ | Delay time, time-slot from DCLKX (see Note 10) | 140 | $t_{d(DCLKX)}$–140 | ns |
| $t_{d(FSX)}$ | Delay time, frame sync | 100 | $t_{c(CLK)}$–100 | ns |
| $t_{c(DCLKX)}$ | Pulse duration, DCLKX | 488 | 15620 | ns |

NOTE 10: $t_{FSLX}$ minimum requirement overrides the $t_{d(TSDX)}$ maximum requirement for 64-kHz operation.

### receive timing requirements over recommended ranges of supply voltages and operating free-air temperature, variable-data-rate mode (see Figure 6)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{d(TSDR)}$ | Delay time, time slot from DCLKR (see Note 11) | 140 | $t_{w(DCLKR)}$–140 | ns |
| $t_{d(FSR)}$ | Delay time, frame sync $T_{C(CLK)}$ | 100 | $t_{c(CLK)}$–100 | ns |
| $t_{su(PCM\ IN)}$ | Setup time before bit 7 falling edge | 10 | | ns |
| $t_{h(PCM\ IN)}$ | Hold time after bit 8 falling edge | 60 | | ns |
| $t_{w(DCLKR)}$ | Pulse duration, DCLKR | 488 | 15620 | ns |
| $t_{SER}$ | Time-slot end receive time | 0 | | ns |

NOTE 11: $t_{FSLR}$ minimum requirement overrides the $t_{c(TSDR)}$ maximum requirement for 64-kHz operation.

### 64 k-bit operation over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{FSLX}$ | Transmit frame sync, minimum down time | FSX = TTL high for remainder of frame | 488 | | ns |
| $t_{FSLR}$ | Receive frame sync, minimum down time | FSR = TTL high for remainder of frame | 1952 | | ns |
| $t_{w(DCLK)}$ | Pulse duration, data clock | | | 10 | μs |

## switching characteristics

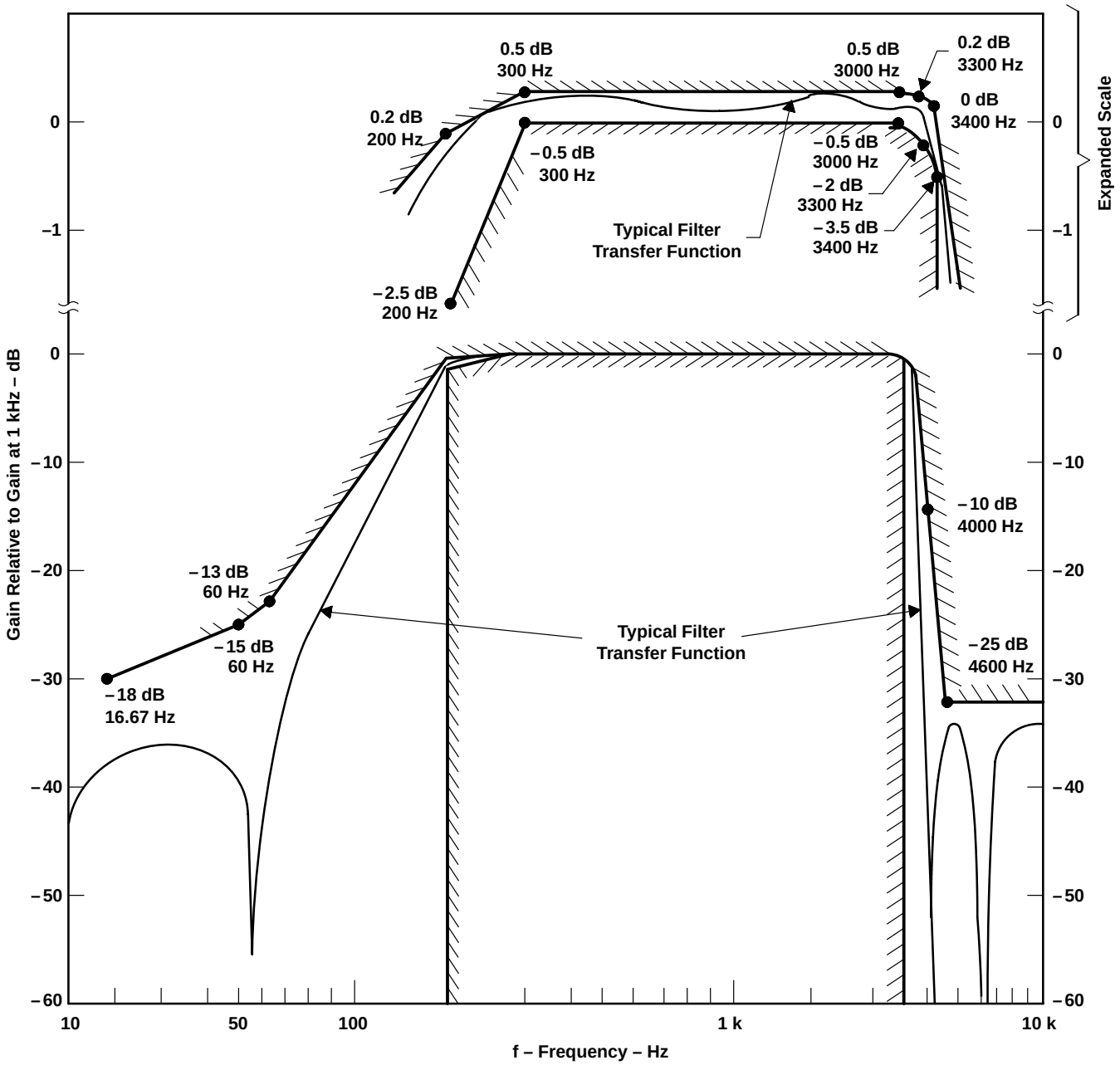
### propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode (see timing diagrams)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{pd1}$ | Delay time from rising edge of transmit clock to bit 1 data valid at PCM OUT (data enable time on time-slot entry) | $C_L$ = 0 to 100 pF | 0 | 145 | ns |
| $t_{pd2}$ | Delay time from rising edge of transmit clock bit n to bit n data valid at PCM OUT (data valid time) | $C_L$ = 0 to 100 pF | 0 | 145 | ns |
| $t_{pd3}$ | Delay time from falling edge of transmit clock bit 8 to bit 8 Hi-Z at PCM OUT (data float time on time-slot exit) | $C_L$ = 0 | 60 | 215 | ns |
| $t_{pd4}$ | Delay time from rising edge of transmit clock bit 1 to TSX active (low) (time-slot enable time) | $C_L$ = 0 to 100 pF | 0 | 145 | ns |
| $t_{pd5}$ | Delay time from falling edge of transmit clock bit 8 to TSX inactive (high) (time-slot disable time) | $C_L$ = 0 | 60 | 190 | ns |

### propagation delay times over recommended ranges of operating conditions, variable-data-rate mode

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{pd6}$ | Delay time from DCLKX | $C_L$ = 0 to 100 pF | 0 | 100 | ns |
| $t_{pd7}$ | Delay time from time-slot enable to PCM OUT | | 0 | 50 | ns |
| $t_{pd8}$ | Delay time from time-slot disable to PCM OUT | | 0 | 80 | ns |
| $t_{pd9}$ | Delay time from FSX | $t_{d(TSDX)}$ = 140 ns | 0 | 140 | ns |

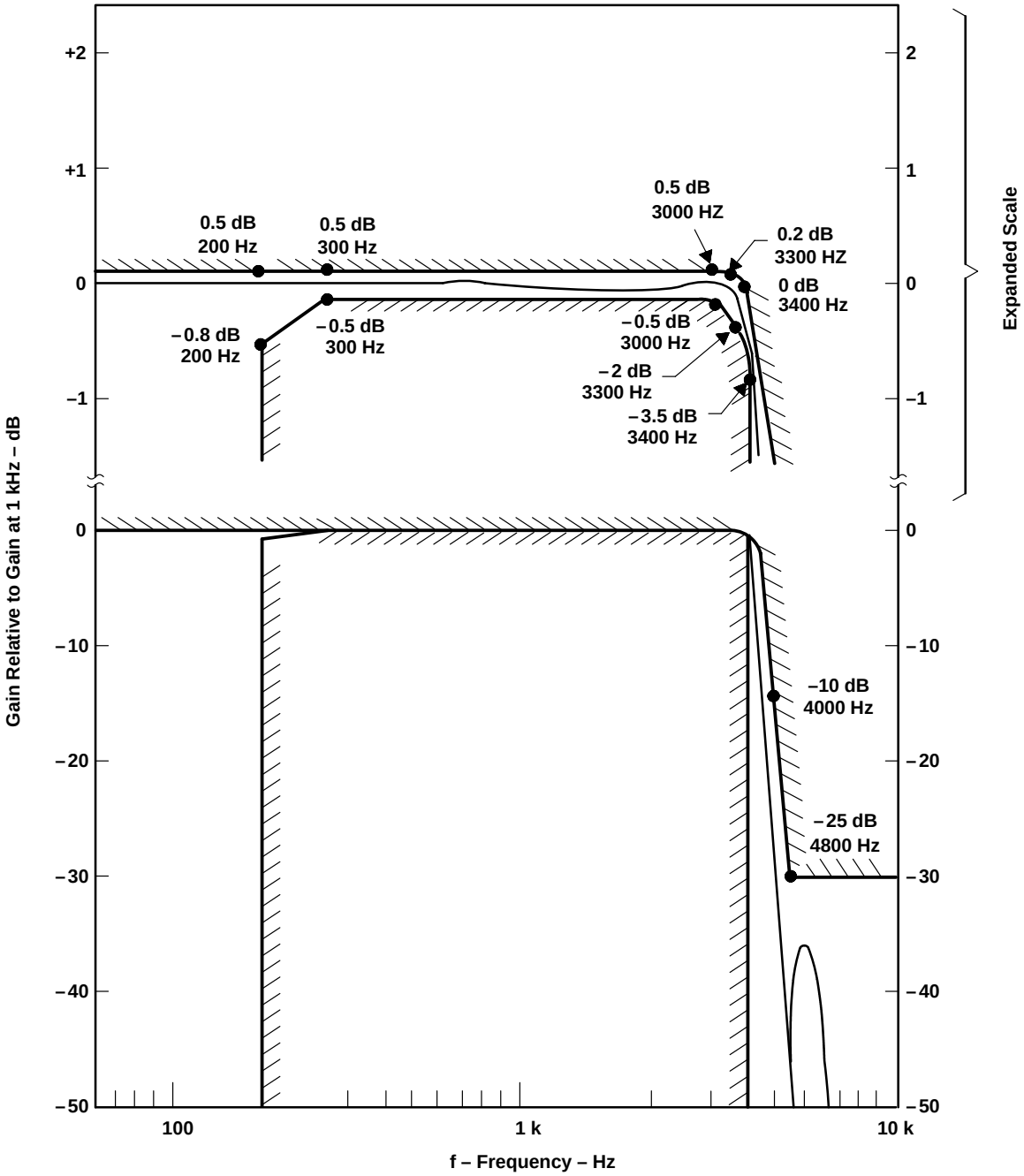
## PARAMETER MEASUREMENT INFORMATION




NOTE A: This is a typical transfer function of the receiver filter component.

**Figure 1. Transmit Filter Transfer Characteristics**

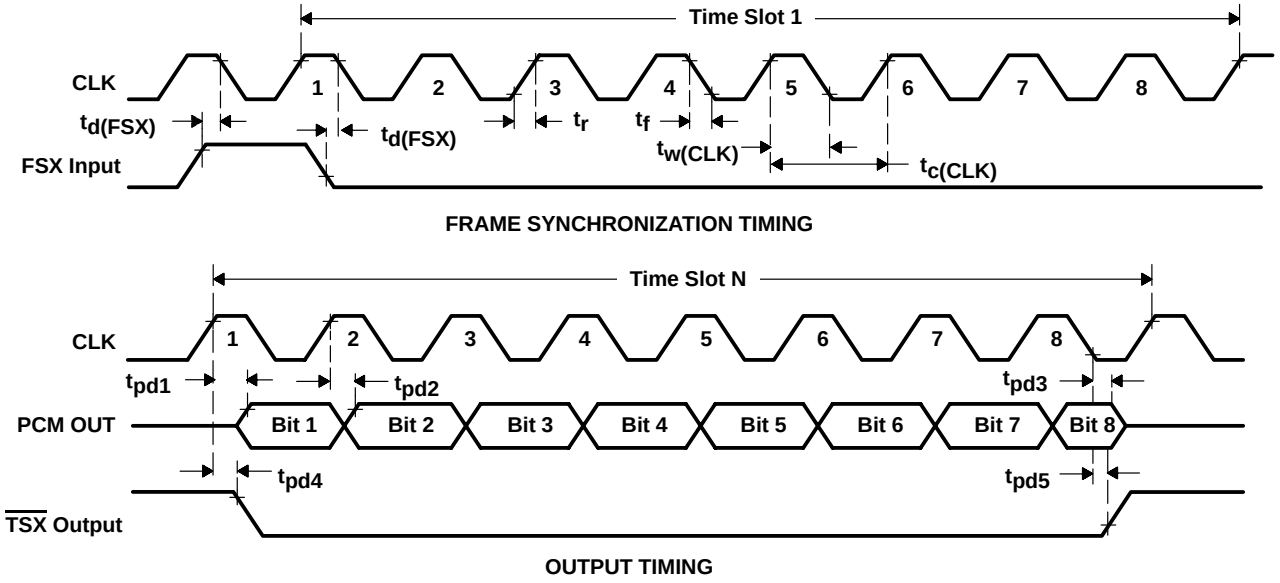
## PARAMETER MEASUREMENT INFORMATION




NOTE A: This is a typical transfer function of the receive filter component.

**Figure 2. Receive Filter Transfer Characteristics**

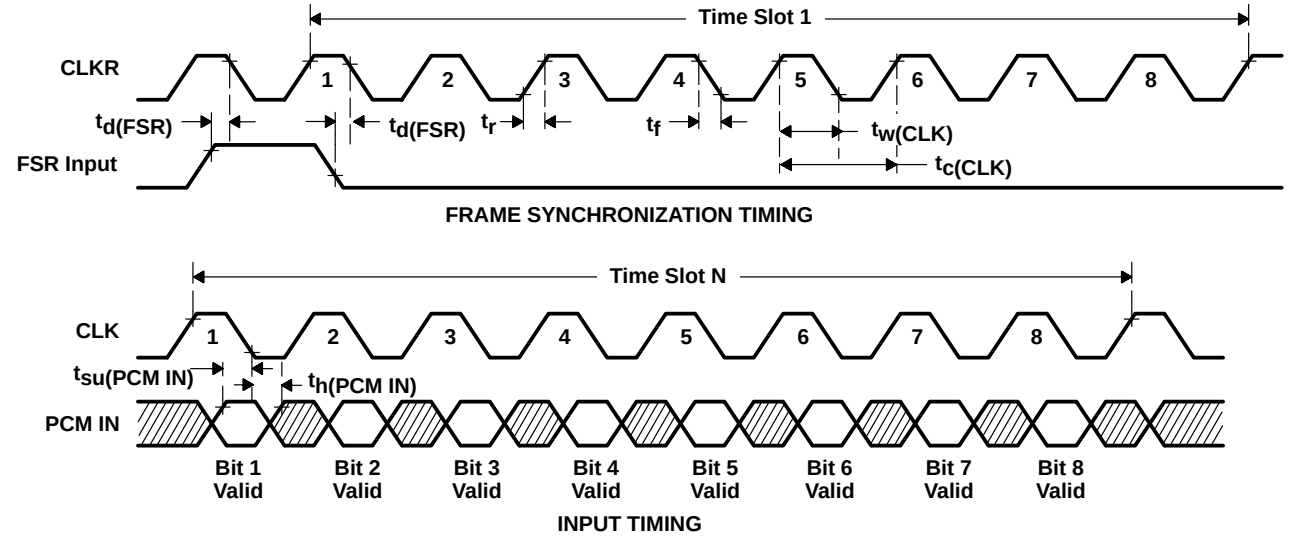
## PARAMETER MEASUREMENT INFORMATION




NOTES: A. Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

B. Bit 1 is the most significant bit (MSB) and is clocked in first on the PCM IN input or is clocked out first on the PCM OUT output. Bit 8 is the least significant bit (LSB) and is clocked in last on the PCM IN input or is clocked out last on the PCM OUT output.

**Figure 3. Transmit Timing (Fixed-Data Rate)**

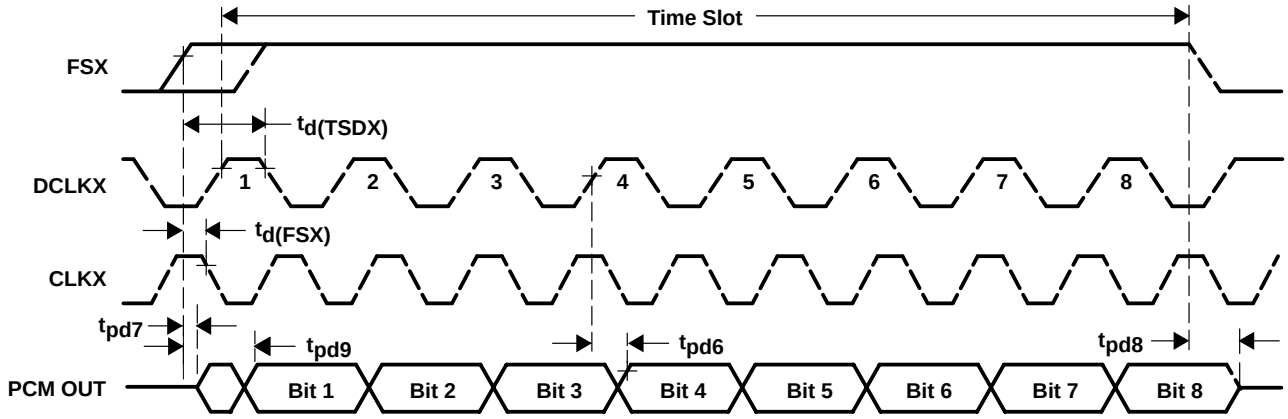



NOTES: A. Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

B. Bit 1 is the most significant bit (MSB) and is clocked in first on the PCM IN input or is clocked out first on the PCM OUT output. Bit 8 is the least significant bit (LSB) and is clocked in last on the PCM IN input or is clocked out last on the PCM OUT output.

**Figure 4. Receive Timing (Fixed-Data Rate)**

## PARAMETER MEASUREMENT INFORMATION

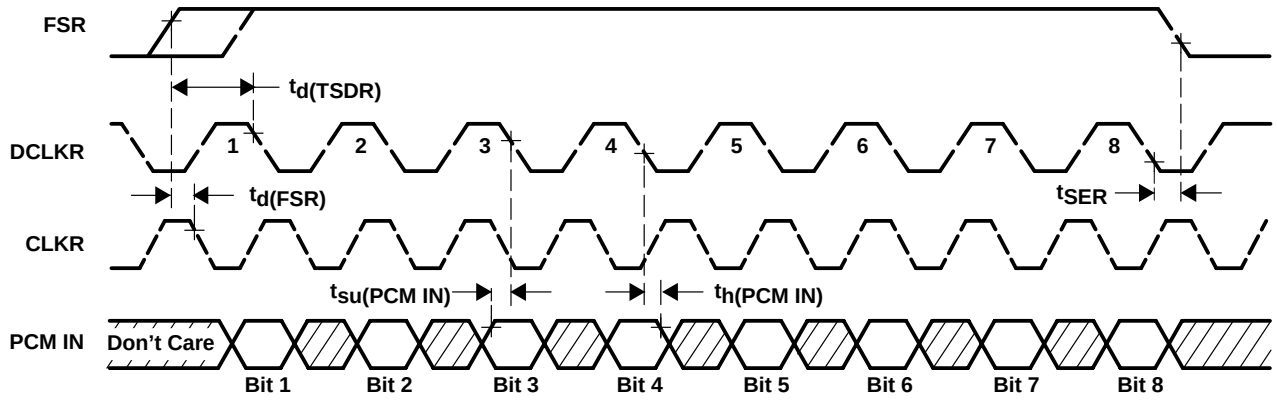



NOTES: A. Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

B. Bit 1 is the most significant bit (MSB) and is clocked in first on the PCM IN input or is clocked out first on the PCM OUT output. Bit 8 is the least significant bit (LSB) and is clocked in last on the PCM IN input or is clocked out last on the PCM OUT output.

C. All timing parameters referenced to $V_{IH}$ and $V_{IL}$ except $t_{pd7}$ and $t_{pd8}$, which references the high-impedance state.

**Figure 5. Transmit Timing (Variable-Data Rate)**




NOTES: A. Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

B. Bit 1 is the most significant bit (MSB) and is clocked in first on the PCM IN input or is clocked out first on the PCM OUT output. Bit 8 is the least significant bit (LSB) and is clocked in last on the PCM IN input or is clocked out last on the PCM OUT output.

C. All timing parameters referenced to $V_{IH}$ and $V_{IL}$ except $t_{pd7}$ and $t_{pd8}$, which references the high-impedance state.

**Figure 6. Receive Timing (Variable-Data Rate)**

## PRINCIPLES OF OPERATION

### system reliability and design considerations

TCM29C18, TCM29C19, TCM129C18, and TCM129C19 system reliability and design considerations are described in the following paragraphs.

#### latch-up

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic SCR that is present due to the inherent nature of CMOS. When a latch-up occurs, the device draws excessive amounts of current and will continue to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current to the device is not limited.

Even though these devices are heavily protected against latch-up, it is still possible to cause latch-up under certain conditions in which excess current is forced into or out of one or more terminals. Latch-up can occur when the positive supply voltage drops momentarily below ground, when the negative supply voltage rises momentarily above ground, or possibly if a signal is applied to a terminal after power has been applied but before the ground is connected. This can happen if the device is hot-inserted into a card with the power applied, or if the device is mounted on a card that has an edge connector and the card is hot-inserted into a system with the power on.

To help ensure that latch-up does not occur, it is considered good design practice to connect a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V – 1N5711 or equivalent) between the power supply and GND (see Figure 7). If it is possible that a TCM29C18-, TCM29C19-, TCM129C18-, or TCM129C19-equipped card that has an edge connector could be hot-inserted into a powered-up system, it is also important to ensure that the ground edge connector traces are longer than the power and signal traces so that the card ground is always the first to make contact.

#### device power-up sequence

Latch-up can also occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device and as a safeguard against this sort of latch-up, it is recommended that the following power-up sequence always be used:

1. Ensure that no signals are applied to the device before the power-up sequence is complete.
2. Connect GND.
3. Apply $V_{BB}$ (most negative voltage).
4. Apply $V_{CC}$ (most positive voltage).
5. Force a power down condition in the device.
6. Connect clocks.
7. Release the power down condition.
8. Apply FS synchronization pulses.
9. Apply the signal inputs.

When powering down the device, this procedure should be followed in the reverse order.

## PRINCIPLES OF OPERATION

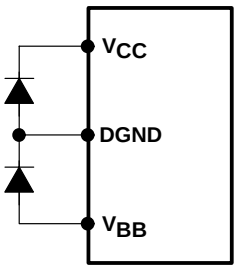



**Figure 7. Latch-Up Protection Diode Connection**

### internal sequencing

On the transmit channel, digital outputs PCM OUT and $\overline{\text{TSX}}$ are held in the high-impedance state for approximately four frames (500 μs) after power up or application of $V_{BB}$ or $V_{CC}$. After this delay, PCM OUT, $\overline{\text{TSX}}$, and signaling are functional and occur in the proper time slot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. Thus valid digital information, such as on/off hook detection, is available almost immediately while analog information is available after some delay.

To further enhance system reliability, PCM OUT and $\overline{\text{TSX}}$ are placed in the high-impedance state approximately 20 μs after an interruption of CLKX. These interruptions could possibly occur with some kind of fault condition.

### power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to $\overline{\text{PDN}}$. In the absence of a signal, $\overline{\text{PDN}}$ is internally pulled up to a high logic level and the device remains active. In the power-down mode, the average power consumption is reduced to 5 mW.

Three standby modes give the user the options of placing the entire device on standby, placing only the transmit channel on standby, or placing only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held low. For transmit-only operation (receive channel on standby), FSX is high and FSR is held low. For receive-only operation (transmit section on standby), FSR is high and FSX is held low. When the entire device is in standby mode, power consumption is reduced to 12 mW. See Table 1 for power-down and standby procedures.

**Table 1. Power-Down and Standby Procedures**

| DEVICE STATUS | PROCEDURE | TYPICAL POWER CONSUMPTION | DIGITAL OUTPUT STATUS |
|---|---|---|---|
| Power down | $\overline{\text{PDN}}$ = TTL low | 5 mW | $\overline{\text{TSX}}$ and PCM OUT are in the high-impedance state |
| Entire device on standby | FSX and FSR are TTL low | 12 mW | $\overline{\text{TSX}}$ and PCM OUT are in the high-impedance state |
| Only transmit on standby | FSX is TTL low,<br>FSR is TTL high | 70 mW | $\overline{\text{TSX}}$ and PCM OUT are placed in the high-impedance state within 300 ns |
| Only receive on standby | FSR is TTL low,<br>FSX is TTL high | 110 mW | |

## PRINCIPLES OF OPERATION

### fixed-data-rate timing (see Figures 3 and 4)

Fixed-data-rate timing is selected by connecting DCLKR to $V_{BB}$ and uses master clock CLK, frame-synchronizer clocks FSX and FSR, and output $\overline{TSX}$. FSX and FSR are 8-kHz inputs that set the sampling frequency. Data is transmitted on PCM OUT on the first eight positive transitions of CLK following the rising edge of FSX. Data is received on PCM IN on the first eight falling edges of CLK following FSX. A digital-to-analog (D/A) conversion is performed on the received digital word and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter.

The TCM29C18 and TCM129C18 operate at 2.048 MHz only. The TCM29C19 and TCM129C19 operate at 1.536 MHz only.

### variable-data-rate timing

Variable-data-rate timing is selected by connecting DCLKR to the bit clock for the receive PCM highway rather than to $V_{BB}$. It uses master clock CLK, bit clocks DCLKX and DCLKR, and frame-synchronization clocks FSX and FSR.

Variable-data-rate timing allows for a flexible data frequency. The frequency of the bit clocks can be varied from 64 kHz to 2.048 MHz. The bit clocks must be asynchronous; however, the master clock is restricted to 2.048 MHz.

When FSX/TSXE is high, PCM data is transmitted from PCM OUT onto the highway on the next eight consecutive positive transitions of DCLKX. Similarly, while the FSR/TSRE input is high, the PCM word is received from the highway by PCM IN on the next eight consecutive negative transitions of DCLKR.

The transmitted PCM word is repeated in all remaining time slots in the 125-μs frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the PCM word to be transmitted to the PCM highway more than once per frame if desired, is available only with variable-data-rate timing.

### asynchronous operation

In either timing mode, the master clock, data clock, and time slot-strobe must be synchronized at the beginning of each frame. Specifically, in the variable-rate mode, the falling edge of CLKX must occur within $t_{d(FSX)}$ ns after the rise of FSX, and the falling edge of DCLKX must occur within $t_{TSDX}$ ns after the rise of FSX. CLK and DCLKX are synchronized once per frame but may be of different frequencies. The receive channel operates in a similar manner and is completely independent of the transmit timing (see Figure 6).

## PRINCIPLES OF OPERATION

### transmit operation

#### transmit filter

The input section provides gain adjustment in the pass band by means of an on-chip uncommitted operational amplifier. The load impedance to ground (ANLG GND) at the amplifier output (GSX) must be greater than 10 kΩ in parallel with less than 50 pF. The input signal on ANLG IN can be either ac or dc coupled.

A low-pass antialiasing filter section is included on the device. This section provides 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched-capacitor section of the transmit filter.

The pass band section provides flatness and stopband attenuation that fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The device specifications meet or exceed digital class 5 central office switching-systems requirements.

A high-pass section configuration was chosen to reject low-frequency noise from 50- and 60-Hz power lines, 17-Hz European electric railroads, ringing frequencies and their harmonics, and other low-frequency noise. Even with the high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

#### encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample-and-hold capacitor. The encoder performs an analog-to-digital conversion on a switched-capacitor array. Digital date representing the sample is transmitted on the first eight data clock bits of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder. The autozero circuit uses the sign bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder. All dc offset is removed from the encoder input waveform.

The analog input is encoded into an 8-bit digital representation by using the μ-law encoding scheme (CCITT G.711) that equates to 12 bits of resolution for low amplitude signals. Similarly, the decoding section converts 8-bit PCM data into an analog signal with 12 bits of dynamic range. The filter characteristics (band pass) for the encoder and decoder are determined by a single clock input (CLK). The filter roll off (–3 dB) is derived by:

$f_{co} = k \bullet f_{CLK}/256$ for the TCM29C18 and TCM129C18
$f_{co} = k \bullet f_{CLK}/192$ for the TCM29C19 and TCM129C19

where k has a value of 0.44 for the high-frequency roll-off point and a value of 0.019 for the low-frequency roll-off point.

The sampling rate of the ADC is determined by the transmit frame-sync clock (FSX); the sampling rate of the DAC is determined by the receive frame-sync clock (FSR). Once a conversion is initiated by FSX or FSR, data is clocked in or out on the next eight consecutive clock pulses in the fixed-rate-mode. Likewise, data may also be transferred on the next eight consecutive clock pulses of the data clocks (DCLKX and DCLKR) in the variable-data-rate mode. In the variable-data-rate mode, DCLKX and DCLKR are independent but must be in the range from $f_{CLK}/32$ to $f_{CLK}$.

## PRINCIPLES OF OPERATION

### receive operation

#### decoding

The serial PCM word is received at PCM IN on the first eight data clock bits of the frame. Digital-to-analog conversion is performed and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

#### receive filter

The receive section of the filter provides pass band flatness and stop band rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

#### receive output power amplifiers

A balanced-output amplifier is provided to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (i.e., referenced to ANLG GND) to drive single-ended loads. Alternatively, the differential output directly drives a bridged load. The output stage is capable of driving loads as low as 300 Ω single ended to a level of 12 dBm or 600 Ω differentially to a level of 15 dBm.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions (i.e., when the digital input at PCM IN is the eight-code sequence specified in CCITT recommendation G.711).

#### output gain

The devices are internally connected to set PWRO+ and PWRO– to 0 dBm.

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