Recent Advancements in Bus-Interface Packaging and Processing

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Introduction

Over the past several years, advancements in semiconductor processing have been combined with advanced surface-mount packages to offer solutions to board area concerns, as well as providing for increased system performance. Figure 1 compares the reduction of the package lead pitch to that of both CMOS and BiCMOS transistor geometries. This paper examines the different types of fine-pitch logic packages and the bus-interface solutions provided when they are combined with submicron semiconductor processes.

Transistor Geometries in μm
Lead Pitch in mm
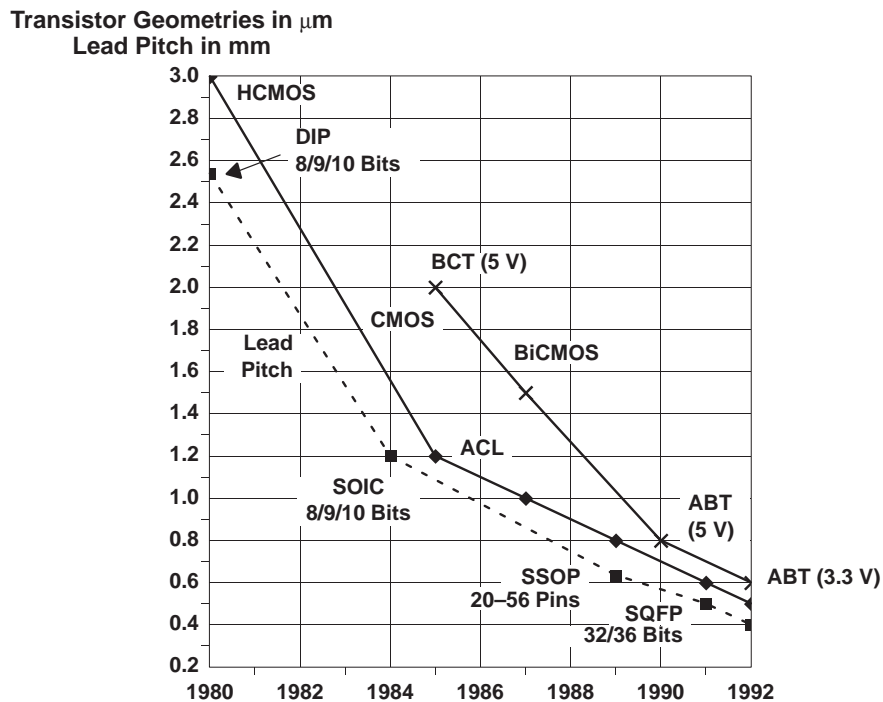
Figure 1. Packaging/Processing Evolution

Evolutions in Device Packaging

With the need for increased functionality in less board area has come the consolidation of much of the board's logic into more complex devices. In many cases, the discrete logic parts that remain, primarily interface/bus drivers, must occupy the board area left over after the higher level chips, i.e., microprocessor, ASICs, memory, etc., have been laid out. To meet this task, the standard small-outline integrated circuit (SOIC) has evolved in two distinct paths. One path reduces the package's area and volume (see Figure 2), and the other increases the bit density of the device (see Figure 3).

One method to increase bit density is to keep the number of pins constant while reducing both the lead pitch and package area. The 20-/24-pin SSOPs utilize a 0.65-mm lead pitch to achieve over a 50% reduction in area, compared to their standard SOIC counterparts. The package height is also reduced from 2.65 mm for the SOIC to 2 mm for the 20-/24-pin SSOPs. This reduction in volume translates into tighter board-to-board spacing, allowing for denser memory arrays.

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The advent of the Personal Computer Memory Card International Association (PCMCIA) standard has required that the package height be reduced even further, thus spawning the thin small-outline package (TSOP). This package utilizes a 0.65-mm lead pitch and has a maximum device height of 1.1 mm. With an area of 59 mm^2, this package occupies 86% less volume than the standard 24-pin SOIC, facilitating the use of logic functions on these cards.

24-Pin SOIC
Area = 165 mm^2

24-Pin SOIC
Height = 2.65 mm
Volume = 437 mm^3
Lead Pitch = 1.27 mm

24-Pin SSOP
Area = 70 mm^2

24-Pin SSOP
Height = 2 mm
Volume = 140 mm^3
Lead Pitch = 0.65 mm

24-Pin TSOP
Area = 54 mm^2

24-Pin TSOP
Height = 1.1 mm
Volume = 59 mm^3
Lead Pitch = 0.65 mm
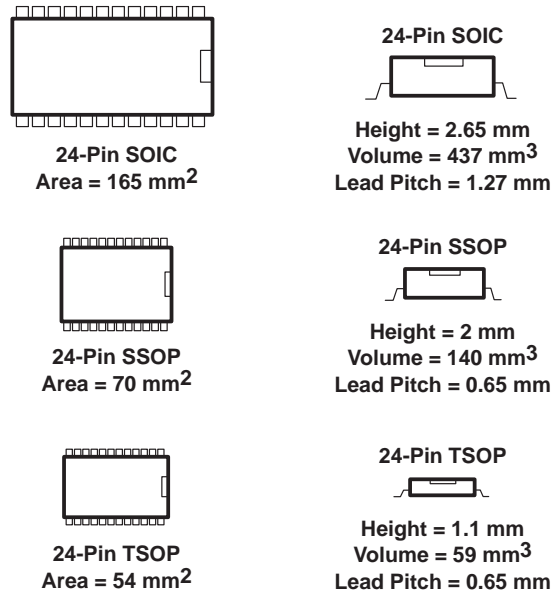
Figure 2. 24-Pin Surface-Mount Comparison

24-Pin SOIC
Area = 165 mm^2

24-Pin SOIC
Height = 2.65 mm
Volume = 437 mm^3
Lead Pitch = 1.27mm

48-Pin SSOP
Area = 171 mm^2

48-Pin SSOP
Height = 2.74 mm
Volume = 469 mm^3
Lead Pitch = 0.635 mm

100-Pin SQFP
Height = 1.5 mm
Volume = 399 mm^3
Lead Pitch = 0.5 mm

100-Pin Cavity SQFP
Height = 2.3 mm
Volume = 612 mm^3
Lead Pitch = 0.5 mm

100-Pin SQFP and
100-Pin Cavity SQFP
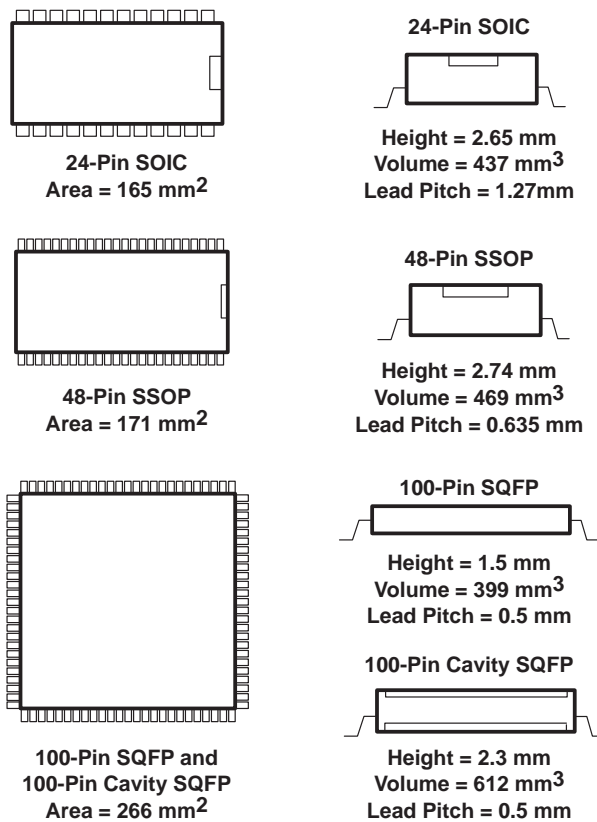**Area = 266 mm^2**

Figure 3. High Pin-Count Comparison

Another way to increase bit density is to reduce the lead pitch of the package. The 48-/56-pin shrink small-outline package (SSOP) halves the lead pitch of the SOIC package from 1.27 mm to 0.635 mm, allowing for twice the number of I/O pins in the same board area. The 8-, 9-, and 10-bit functions now become 16-, 18-, and 20-bit devices. The 100-pin shrink quad flat package (SQFP), along with the high-power cavity SQFP, further reduces the lead pitch to 0.5 mm. These packages double the bit density over the 48-pin SSOP with only a 50% increase in area. Both of these high pin-count packages allow for 32- and 36-bit logic functions, providing for efficient buffering of today's 32- and 64-bit bus widths.

Thermal Impedances of Bus-Interface Packages

By far the most common measure of package thermal performance is θ_{JA}, the thermal impedance measured (or modeled) from junction to ambient. θ_{JA} values are also the most subject to interpretation. Factors that can greatly influence the measurement and calculation of θ_{JA} are:

- Board mounted: yes/no?
- Traces: size, composition, thickness, and geometry
- Orientation: horizontal or vertical?
- Ambient: volume
- Proximity: any other surfaces near the device being measured?

In August 1996, the Electronics Industries Association released Standard EIA/JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*. This standard provides guidelines for design of the test board used in taking thermal-impedance measurements of integrated-circuit packages. Prior to release of this standard, thermal-impedance data for similar packages varied greatly across the industry because of the use of different test-board designs. In particular, the characteristics of the test board have a dramatic impact on the measured θ_{JA}. As the industry begins using this standard test-board design, the variation in thermal-resistance data caused by the board should be minimized.

Key features of the standard test-board design are:

- Board thickness: 0.062 in.
- Board dimension: 3.0 in. × 4.5 in. for packages < 27.0 mm in length
- Board dimension: 4.0 in. × 4.5 in. for packages > 27.0 mm in length
- Trace thickness: 0.0028 in.
- Trace length: 0.984 in. (25.0 mm)

The ASL product group is now using the EIA/JESD51-3 standard to design the test boards used for thermal-impedance measurements. Also, the parameters outlined in this standard are used to set up thermal models. Thermal-impedance (θ_{JA}) data is now available for all ASL leaded surface-mount packages using the new JEDEC standard. Actual data has been generated on several ASL packages, and thermal models have been run on the remaining packages. Please refer to *Thermal Characteristics of SLL Packages and Devices*, literature number SCZA005, for additional information.

Evolutions in Device Processing

With the improvements to microprocessor clock rates and memory access times, bus-interface devices have become a larger percentage of the total bus cycle time. To keep pace with the need for faster logic, many semiconductor manufacturers are using submicron BiCMOS processes with shorter gate lengths and thinner gate oxide for device speed improvements. The reductions in transistor area result in less intrinsic capacitance, allowing faster internal gate delays, as well as lowering the output capacitance (C_{io}). With a lower C_{io}, ABT devices minimize their impact on system loading.

In a transmission-line environment, when the driver's edge rate is less than twice the line's propagation delay, distributed output loading has the effect of reducing the characteristic impedance (Z_O) of the transmission line. The higher the distributed capacitive load, the lower the apparent impedance, making it harder for the driver to switch the line on the incident wave. This well-known transmission-line loading equation is:

$$ Z'_O = \frac{Z_O}{\sqrt{1 + \frac{C_d}{C_o}}} \tag{1} $$

Where:

> Z_O = line's unloaded characteristic impedance, C_o
> C_o = line's intrinsic capacitance per unit length
> C_d = distributed capacitive load per unit length

Figure 4 shows how device output capacitance can lower line impedance, as in the case of a backplane. If the effects of the other board capacitance contributors — connectors, vias, and trace stubs — are assumed to be constant regardless of the device used, and thus ignored, a comparison of transmission-line loading between different technologies can be made.
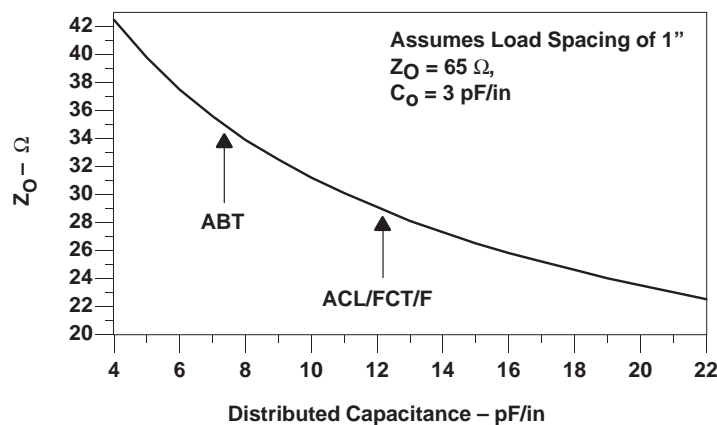

Figure 4. Loaded Z_O Versus Distributed Capacitance

3.3-V Operation

As process geometries move toward gate lengths of 0.5 μm and below, coupled with the desire for lower power consumption, 3.3-V operation becomes necessary. Because the migration to 3.3 V will be gradual, gated by the availability of semiconductor functions, the need for mixed signal-level operation will be critical for bus-interface devices. That is, the input and I/O pins will have input voltage levels up to 5.5 V without any conduction paths to V_{CC}. The outputs should also be capable of driving a standard 5-V backplane, which translates into drive currents of at least –15 mA of I_{OH} and 64 mA of I_{OL}.

Advanced Bus-Interface Solutions

Memory-Driver Usages for the SSOP

As noted previously, any of the SSOPs can be used as buffers in high-density memory arrays. In many instances, series damping termination is chosen due for its ease of implementation and power savings. Numerous logic devices are available that incorporate the series damping resistor on chip, as in the BCT2XXX series of products, simplifying this type of termination. When these parts are packaged in the 20-pin SSOP, as in the 'BCT2240DB, a tremendous board real-estate savings is realized over a discrete approach using external resistors and SOIC devices. For PCMCIA cards, the driver also must offer low-power consumption necessary for battery operation. The 'AC11244PW (TSOP package) can be used in these applications due to its low static-power CMOS characteristics.

Many times, when an output switches a large memory array, the capacitive load is localized in close proximity to the driver and can be treated as a simple lumped load. In these instances, it is useful to know how the propagation delay (t_{pd}) of the driver changes with the additional capacitive load. The change in the driver's t_{pd} is due to the interaction of its source impedance (R_{on}) with the capacitive load (C_L). Figures 5, 6, and 7 show these phenomena for the 'AC11244, 'BCT2240, 'ABT16244, and 'ABT32245 for both single- and multiple-outputs switching.
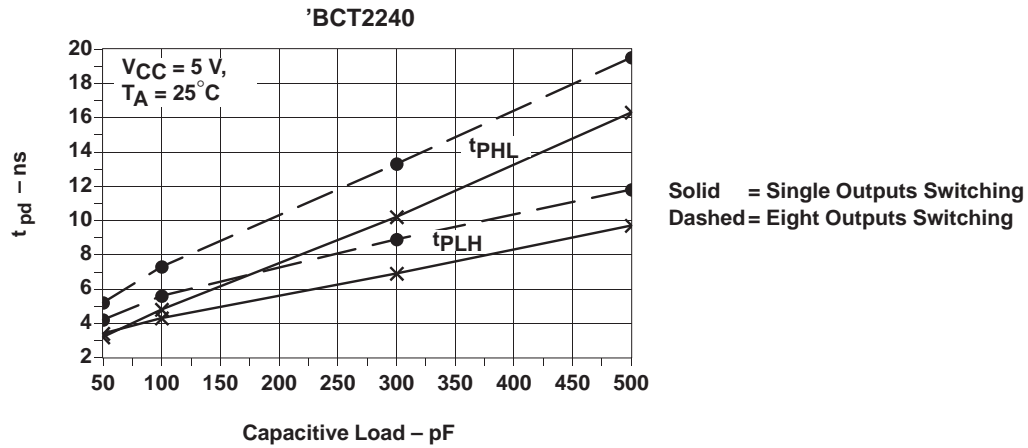
'BCT2240

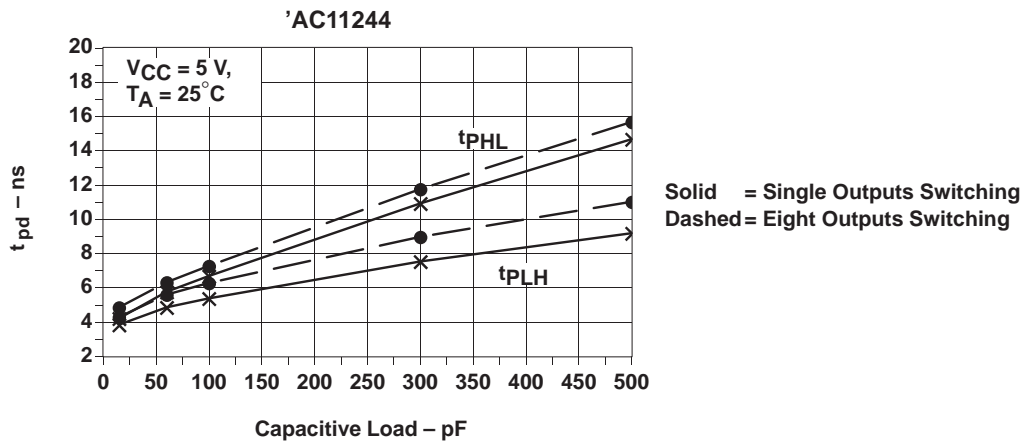Figure 5. Typical t_{pd} Versus Capacitive Load

'AC11244

Figure 6. Typical t_{pd} Versus Capacitive Load
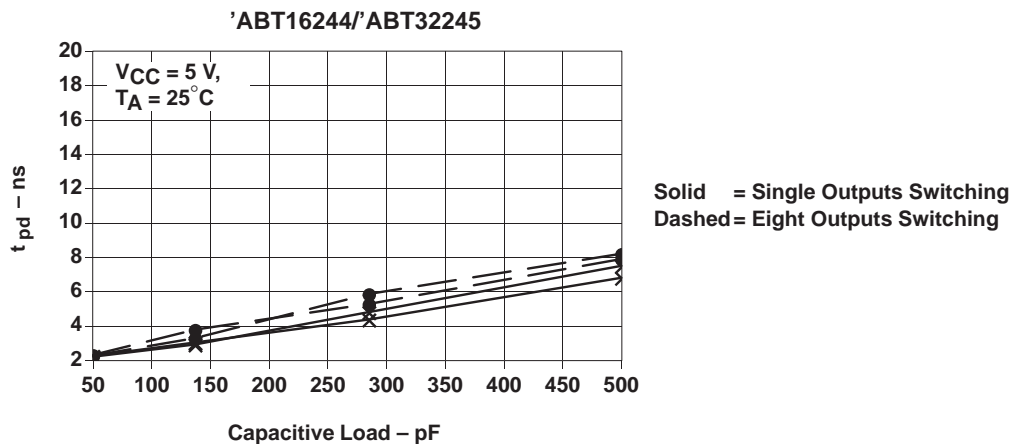
'ABT16244/'ABT32245

Figure 7. Typical t_{pd} Versus Capacitive Load

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Figures 5 through 7 illustrate the effect that the output impedance of the driver has over t_{pd} degradation. Figure 5 shows that, even though the 'AC11244 has symmetrical high and low output-drive current ratings of 24 mA, t_{PHL} shows more degradation versus capacitive loading due to the graded turn on of the output to minimize simultaneous switching noise (ground bounce). Many advanced CMOS logic devices use this graded turn on, but not without the penalty of slower propagation delays at higher capacitive loads. Figure 6 shows a similar asymmetrical t_{PHL} performance, but now it is due to the inclusion of a 33-Ω series output resistor. In contrast to Figures 5 and 6, Figure 7 highlights the high-drive capability of the ABT16XXX and ABT32XXX devices, along with the symmetrical t_{pd} performance that the –32-mA/64-mA outputs deliver.

Bus-Interface Usages for the SSOP

The gains made by using devices with faster propagation delays can be lost if the propagation delay degrades when multiple outputs on a package are switched simultaneously. This effect is greatly reduced when a device is packaged in the 48-/56-pin SSOP, because this package allows the signal-to-ground ratio of a standard 8-bit function to be improved from 8:1 to 2:1, and the signal-to-V_{CC} ratio to be improved from 8:1 to 4:1. This multiple power-pin system translates into a quieter on-chip power system when multiple outputs switch, resulting in less propagation-delay degradation compared to a standard 8-bit function. The same is true for 100-pin SQFP and cavity SQFP that uses a 3:1 signal-to-ground ratio. Figure 8 compares the change in t_{pd} versus the number of outputs switching (in phase) of a typical '244 buffer-type function when packaged in a 48-pin SSOP and 100-pin SQFP to the performance in a 20-pin DIP and SOIC.
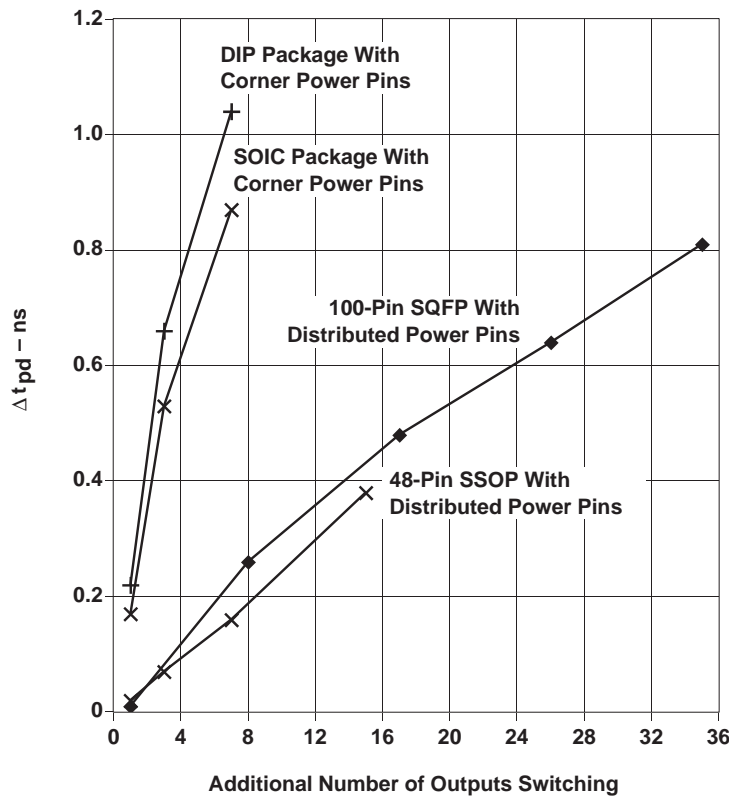
Figure 8. Typical Δt_{pd} Versus Outputs Switching

Summary

The various fine-pitch surface-mount packages give the designer a wide range of solutions to today's system area and volume constraints. The high pin-count SSOP and SQFP packages allow bus-interface devices to track the trend of wider data bus widths, while providing superior electrical performance when compared to the standard end-pin product. The cavity SQFP allows for higher power-dissipation applications, allowing the interface device to operate at higher frequencies. The low pin-count SSOPs occupy less volume than other surface-mount devices, facilitating their use in height-critical applications.

References

Transmission Lines

Advanced Schottky Family Applications, Texas Instruments Incorporated Advanced Schottky Data Book, 1986
Advanced CMOS Logic Designer's Handbook, Texas Instruments Incorporated, 1988

Power Dissipation

SSOP Designer's Handbook, Texas Instruments Incorporated, 1991