Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices

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Thermal Considerations for Standard Linear and Logic (SLL) Packages and Devices

Users of Texas Instruments (TI™) SLL products must consider device power dissipation, package power capability, and maximum ambient temperatures when designing with these products. The product users also need to be aware of the long-term reliability impact of maximum device-junction temperatures.

This application report is intended to help users understand and evaluate these factors. Three concepts — package thermal performance, device power dissipation, and reliability — are discussed in separate sections.

The first section, *Package Thermal Performance*, includes data about the recently developed EIA/JEDEC Standard JESD 51 for package thermal-impedance measurement. It discusses most SLL package types and lists θ_{JA} (thermal impedance) values for those packages.

The second section, *Power Calculation*, discusses the power consumption by CMOS and BiCMOS/bipolar semiconductors. Standard formulas are given that allow the user to calculate the maximum power dissipated by a device in a typical application using data-book specifications, operating frequency, and voltage. The only characteristic not readily known is the output loading of the devices under consideration.

The third section, *Benefits of Minimizing Power Consumption*, discusses ways to reduce power consumption and the benefits thereof.

The final section, *Reliability Implications*, discusses the effects of chip temperature on reliability and electromigration. Information presented in this section allows the user to make an informed judgment as to the maximum chip temperature versus device wearout acceptable in the particular application.

The recommended analysis procedure is to assume a maximum chip temperature (see *Reliability Implications*) then, using θ_{JA} values for the chosen package (see *Package Thermal Performance*) and the known environmental requirements, calculate the maximum permissible power for that package. The formula presented in the *Power Calculation* section can then be used to ensure the operating conditions do not exceed the power capability of the chosen package type. Of course, the user can choose to calculate the maximum power from the application, then select a package that can meet the power dissipation requirement.

Package Thermal Performance

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{JA} = \frac{T_j - T_a}{P} \quad \textbf{(1)}$$

Where:

T_j = chip junction temperature
T_a = ambient temperature
P = device power dissipation

θ_{JA} values are also the most subject to interpretation. Factors that can greatly influence the measurement and calculation of θ_{JA} are:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

JEDEC established the JC 15.1 committee, comprising industry representatives, to develop industry-standard specifications for thermal testing. The specifications include development of electrical test procedures, careful descriptions of appropriate test environments, guidelines for the design of thermal test chips, guidelines for thermal modeling, and specifications for component mounting. The specifications for component mounting are divided into a series for different package types. The specifications include test-board descriptions for low effective thermal-conductivity test boards with a single metal layer and high effective thermal-conductivity test boards with embedded solid copper planes simulating system power and ground planes.

In August 1996, the Electronics Industries Association released JESD 51-3 titled *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*. The standard describes guidelines with parameters for thermal-test-board design for low effective thermal conductivity (one signal layer in the trace fanout area) as differentiated from a multilayer printed-circuit board (PCB), which might include power and ground planes. The specified parameters include the area of the test board, the amount of copper traces on the test board, and the resulting trace fanout area, each important to the heat-sinking characteristics of the PCB. Prior to release of the standard, thermal-impedance data for similar packages varied widely within the industry due to the use of different test-board designs. As the industry adopts this standard methodology, thermal-impedance variations from test-board design should be minimized.

Key features of the standard test-board design are:

- Board thickness: 0.062 in.
- Board dimensions: 4.0×4.5 in. for packages > than 27 mm in length, 3.0×4.5 in. for packages $\leq$ 27 mm in length
- Trace thickness: 0.0028 in.
- Trace length: 25.0 mm (0.984 in.)

The SLL product group uses test boards designed to JESD 51-3 for thermal-impedance measurements. The parameters outlined in the standard also are used to set up thermal models. The thermal-model program used by SLL is ThermCAL, a finite-difference thermal-modeling tool.

Eleven SLL packages were tested using a JEDEC test-board design and compared to ThermCAL model results to validate the correlation between model results and data (see Table 1). This comparison shows that the models are accurate to within 10% of measured data. In many cases the model data varies from measured data by less than 5%.

Table 1. Package Comparison

PACKAGE TYPE (PINS, DESIGNATION)	DIE SIZE (mils)	θ_{JA} MEASURED (°C/W)	θ_{JA} MODELED (°C/W)	CHANGE (%)
56 DL	120 × 120	73.5	78.3	6.5
20 DW	62 × 62	96.6	90.9	–5.9
160 PCM	240 × 240	34.9	34.9	0
52 PAH†	120 × 120	87.2	92.2	5.7
52 PAH‡	120 × 120	72.7	75.2	3.4
100 PZ	360 × 360	45	42.8	–4.9
208 PDV	240 × 240	50.1	52.8	5.4
48 DGG	120 × 120	89.1	93.5	4.9
14 DGV	62 × 62	181.5	191.7	5.6
48 DGV	62 × 186	92.9	89.9	–3.2
100 PCA	240 × 240	33.3	34.9	4.8

† S-pad leadframe
‡ Conventional leadframe

After the accuracy of the model results was established, all other SLL packages could be modeled. θ_{JA} data based on JESD 51-3 is available for all SLL leaded surface-mount packages (see Table 2). The data is grouped by package type with values of θ_{JA} shown at different airflow levels. Leadframe pad size and die size are shown.

Junction-to-case thermal-impedance (θ_{JC}) data is shown with the junction-to-ambient data. Measured θ_{JC} data was generated for the packages tested using the JEDEC PCB. Previously published values of θ_{JC} are used for packages not yet tested using the PCB designed to JESD 51-3.

Table 2. SLL Package Thermal-Impedance Data

PIN COUNT	TI PACKAGE	JEDEC SPECIFICATION	PAD SIZE (mils)	CHIP SIZE (mils)	θ_{JA} (°C/W) AT AIRFLOW (LFM)				MEASURED/ MODELED	θ_{JC} (°C/W)
					0	150	250	500		
SOIC										
14	D	MS-012	70 × 70	32 × 37	126.6	104	96.4	87.4	Modeled	46
16	D	MS-012	90 × 90	44 × 65	112.6	91.2	83.9	74.8	Modeled	42
20	DW	MS-013	90 × 110	62 × 62	96.6	82.2	77.7	71.5	Measured	38.3
24	DW	MS-013	140 × 160	84 × 122	80.7	53.7	47.5	40.7	Modeled	25
28	DW	MS-013	120 × 140	90 × 128	78.2	54.3	48.4	41.9	Modeled	
SSOP										
14	DB	MO-150	71 × 71	43 × 52	158	128.6	118.9	106.5	Modeled	47
16	DB	MO-150	83 × 91	51 × 61	130.8	105.9	97.3	86.5	Modeled	47
20	DB	MO-150	87 × 106	61 × 65	114.6	92	84	74.7	Modeled	45
24	DB	MO-150	87 × 106	74 × 91	104.2	83.5	76.3	67.5	Modeled	42
20	DBQ	MS-137	96 × 140	61 × 75	118.1	95.3	86.9	76.7	Modeled	46
24	DBQ	MS-137	96 × 140	61 × 75	113	92	84.1	74.6	Modeled	42
28	DL	MO-118	150 × 180	97 × 142	97	77.2	70.9	63.1	Modeled	
48	DL	MO-118	120 × 180	73 × 128	93.5	69.9	63.8	57.1	Modeled	26
56	DL	MO-118	150 × 220	120 × 120	73.5	62.3	59	54.6	Measured	27.3
PLCC										
28	FN	MS-018	300 × 348	214 × 319	70.9	58.8	52.7	46	Modeled	26.7
44	FN	MS-018	270 × 270	235 × 235	46.2	38.6	35.4	31.6	Modeled	22
68	FN	MS-018	325 × 325	280 × 280	39.3	33	30.5	27.6	Modeled	14.5
84	FN	MS-018	275 × 275	188 × 185	39.7	33.9	31.8	29.4	Modeled	11.9
QFP										
52	RC	MS-022	210 × 210	120 × 120	78.9	48.4	43.6	38.1	Modeled	20
80	PH		265 × 265	232 × 240	76.1	67.9	61.4	53.6	Modeled	15.1
132	PQ	MO-069	315 × 315	272 × 272	46.3	34.5	31.6	28.3	Modeled	9.8
144	PCM	MS-022	433 × 433	338 × 338	38.8	27.3	25.1	22.4	Modeled	14.5
160	PCM	MS-022	511 × 511	433 × 433	34.9	29.9	28.3	24.7	Measured	11.4
208	PPM	MO-143	413 × 413	268 × 268	36.7	30.4	28.1	26.7	Modeled	
TQFP										
52	PAH	MO-136	S-Pad	120 × 120	87.2	76.1	71.5	67	Measured	28.3
52	PAH	MO-136	3.5 × 3.5 mm	120 × 120	72.7	62.6	59.2	53.8	Measured	24.0
64	PM	MO-136	6.75 × 6.75 mm	235 × 235	66.9	53.6	47.6	40.6	Modeled	10.4
64	PAG	MO-136	S-Pad	240 × 240	58.2	48.8	45.2	40.3	Measured	22.6
80	PN	MO-136	S-Pad	240 × 240	61.5	52.8	49.3	44.6	Measured	26.4
100	PZ	MO-136	S-Pad	360 × 360	45	38.3	35.3	27.9	Measured	7.6
100	PZ	MO-136	S-Pad	240 × 240	50.1	42.7	40.4	36.8	Measured	21.1
100	PCA	MO-136	6.5 × 6.5 mm	240 × 240	33.3	24.7	21.8	19.2	Measured	4.3
120	PCB	MO-136	6.5 × 6.5 mm	240 × 240	28.1	22.3	21	18	Modeled	3.3
144	PGE	MO-136	342 × 350	378 × 378	48.3	39.1	35.5	31	Modeled	9.9
208	PDV	MO-136	S-Pad	240 × 240	50.1	43.63	40.9	37.3	Measured	9.9

Table 2. SLL Package Thermal-Impedance Data (Continued)

PIN COUNT	TI PACKAGE	JEDEC SPECIFICATION	PAD SIZE (mils)	CHIP SIZE (mils)	θ_{JA} (°C/W) AT AIRFLOW (LFM)				MEASURED/ MODELED	θ_{JC} (°C/W)
					0	150	250	500		
SOP										
14	NS	EIAJ-TYPE-II	79 × 87	55 × 57	127.1	103.7	95.5	85.2	Modeled	95
16	NS	EIAJ-TYPE-II	87 × 142	76 × 86	111.3	89.3	81.4	71.5	Modeled	95
20	NS	EIAJ-TYPE-II	87 × 118	60 × 77	100.3	82.8	76.2	68	Modeled	90
TSSOP										
14	PW	MO-153	71 × 71	48 × 53	169.8	146.7	136	121.7	Modeled	35
16	PW	MO-153	104 × 104	56 × 76	148.9	127.9	117.6	103.9	Modeled	35
20	PW	MO-153	102 × 106	53 × 69	128	110.6	101.9	90.8	Modeled	34
24	PW	MO-153	94 × 140	74 × 91	119.9	98.8	90.6	80	Modeled	33
48	DGG	MO-153	4.6 × 3.2 mm	120 × 120	89.1	78.5	75.1	69.4	Measured	25.2
56	DGG	MO-153	3.94 × 5.08 mm	132 × 176	81.2	72.8	65.8	57.9	Modeled	13
64	DGG	MO-153	5.7 × 3.6 mm	120 × 120	72.9	63.3	61.8	57.1	Measured	21.3
TVSOP										
14	DGV	MO-194	75 × 75	62 × 62	181.5	165.8	159.5	150.4	Measured	66.7
16	DGV	MO-194	75 × 75	65 × 65	179.6	153.2	141.7	126.3	Modeled	
20	DGV	MO-194	104 × 104	94 × 94	146.1	122.3	111.6	97.4	Modeled	
24	DGV	MO-194	104 × 104	94 × 94	138.6	116.2	106.2	93.2	Modeled	
48	DGV	MO-194	100 × 240	62 × 186	92.9	80.9	77.1	71	Measured	27.2
56	DGV	MO-194	100 × 274	90 × 262	85.9	64.6	57.1	48.4	Modeled	
80	DBB	MO-194	100 × 224	93 × 203	105.6	78.4	71.8	63.7	Modeled	
PDIP (assumes zero trace length)										
8	P	MS-001			104					41
14/16	N	MS-001			78					32
20	N	MS-001			67					33
24	NT	MS-001			67					25
		BGA								
256	GFN	MO-151			42				ANAM data	6.2
388	GFW	MO-151			18.9				Model data	

Power Calculation

Reduction of power consumption makes a device more robust and reliable. When calculating the total power consumption of a circuit, both the static and the dynamic currents must be taken into account. Both bipolar and BiCMOS devices have varying static-current levels, depending on the state of the output (I_{CCL}, I_{CCH}, or I_{CCZ}), while a CMOS device has a single value for I_{CC}. These values can be found in the individual data sheets. TTL-compatible CMOS and BiCMOS inputs, when driven at TTL levels, also consume additional current because they may not be driven all the way to V_{CC} or GND; therefore, the input transistors are not switched completely off. This value, known as ΔI_{CC}, also is provided in the data sheet.

Due to the high operating frequencies, there is a strict limit on power consumption in computer systems. Therefore, allowable power consumption for each device on a board must be minimized. Power calculations are made to determine power-supply sizing, current requirements, cooling/heatsink requirements, and criteria for device selection. Power calculation also can determine the maximum reliable operating frequency.

There are two components that establish the amount of power consumption in a CMOS circuit:

- Static power consumption
- Dynamic power consumption

Dynamic power consumption results from charging and discharging external load and internal parasitic capacitances. The parameter for CMOS device parasitic capacitance is C_{pd}, which is listed in the data sheet and is obtained using equations 2 and 3:

$$C_{pd} = \frac{I_{CC}}{V_{CC} \times f_I} - C_{L(eff)} \quad \textbf{(2)}$$

$$C_{L(eff)} = C_L \times N_{SW} \times \frac{f_O}{f_I} \quad \textbf{(3)}$$

To explain the C_{pd} and the method of calculating dynamic power, see Table 3, which indicates the C_{pd} test conditions for AHC devices. The symbols used in Table 3 are:

V = V_{CC} (5 V)
G = ground (0 V)
1 = high logic level = V_{CC} (5 V)
0 = low logic level = ground (0 V)
X = don't care: 1 or 0, but not switching
C = 50% duty cycle input pulse (1 MHz) (see Figure 1)
D = 50% duty cycle input (1/2 frequency) out-of-phase input pulse (see Figure 1)
S = standard ac output load (50 pF to GND)

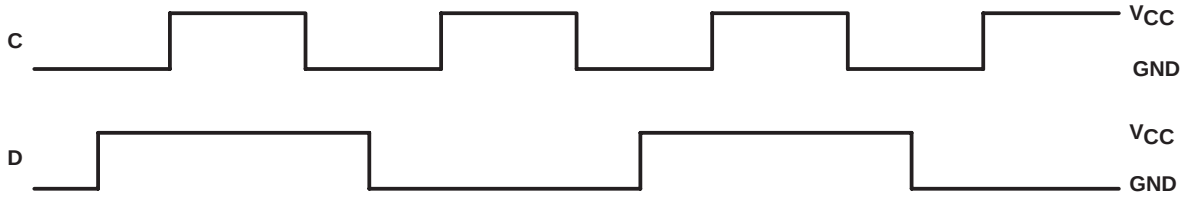

Figure 1. Input Waveform

Table 3 shows the switching of each pin for AHC devices. Once the C_{pd} is determined from the table, the P_D is easy to calculate using equations explained in the following sections.

Although a C_{pd} value is not provided for ABT and LVT, the I_{CC} versus frequency curves display essentially the same information (see Figures 2 and 3). The slope of the curve provides a value in the form of mA/(MHz × bit), which when multiplied by the number of outputs switching and the desired frequency, provides the dynamic power dissipated by the device without the load current. Equations 4 through 14 can be used to calculate total power for CMOS or BiCMOS devices.

Table 3. C_{pd} Test Conditions With One- or Multiple-Bit Switching

TYPE	PIN NO.																			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
AHC00	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC02	S	C	0	S	X	X	G	X	X	S	X	X	S	V						
AHC04	C	S	X	S	X	S	G	S	X	S	X	S	X	V						
AHC08	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC10	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC11	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC14	C	S	X	S	X	S	G	S	X	S	X	S	X	V						
AHC32	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC74	1	D	C	1	S	S	G	S	S	X	X	X	1	V						
AHC86	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC138	C	0	0	0	0	1	S	G	S	S	S	S	S	S	S	V				
AHC139	0	C	0	S	S	S	S	G	S	S	S	S	X	X	X	V				
AHC240	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC244	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC245	1	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC373†	0	S	D	D	S	S	D	D	S	G	C	S	D	D	S	S	D	D	S	V
AHC374‡	0	S	D	D	S	S	D	D	S	G	C	S	D	D	S	S	D	D	S	V
AHC540	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC541	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC573†	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V
AHC574‡	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V

† All bits switching, but with no active clock signal
‡ All bits switching

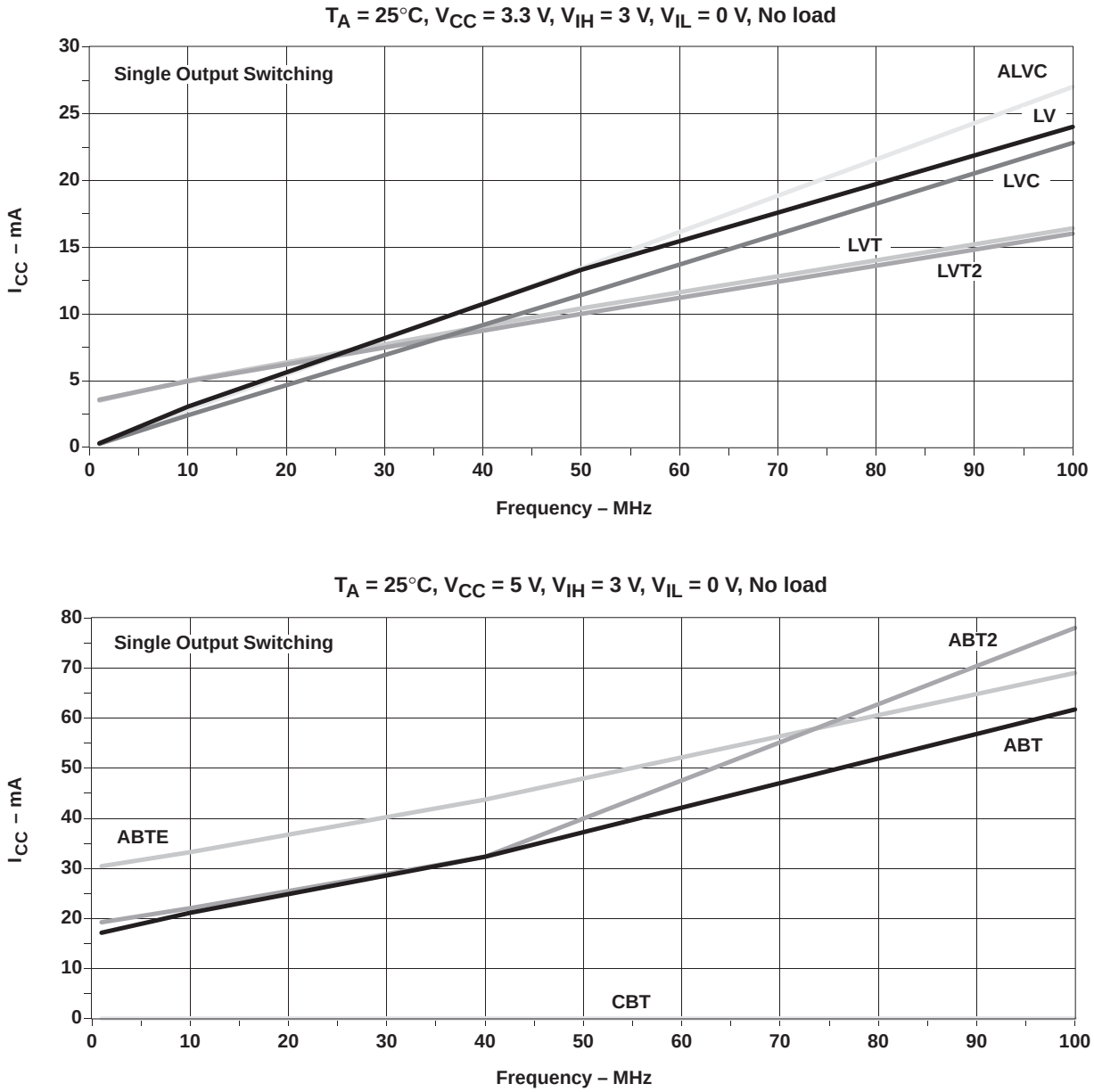

Figure 2. Power Consumption With a Single Output Switching

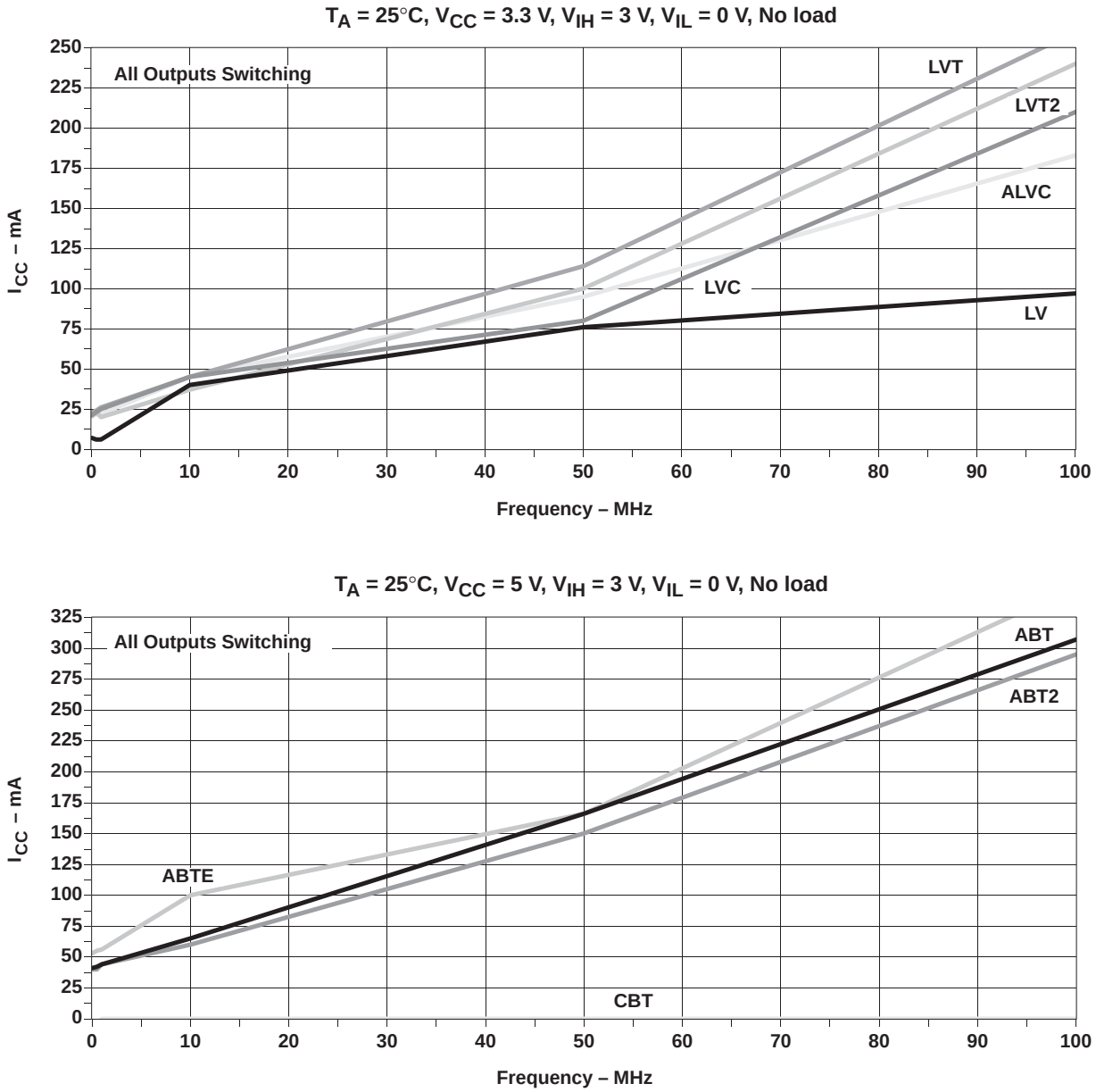

Figure 3. Power Consumption With All Outputs Switching

CMOS

CMOS-Level Inputs

Static power consumption can be calculated using equation 4.

$$P_S = V_{CC} \times I_{CC} \quad \textbf{(4)}$$

The dynamic power consumption of a CMOS device is calculated by adding the transient power consumption and capacitive-load power consumption.

Transient Power Consumption

The transient power is due to the current that flows only when the transistors of the devices are switching from one logic state to another. This power is a result of the current required to charge the internal nodes (*switching current*) plus the current that flows from V_{CC} to GND when the p-channel and n-channel transistors turn on briefly at the same time during the logic transition (*through current*). The frequency at which the device is switching, plus the rise and fall time of the input signal, as well as the internal nodes of the device, have a direct effect on the duration of the current spike. For fast input transition rates, the through current of the gate is negligible in comparison with the switching current. For this reason, the dynamic supply current is governed by the internal capacitance of the device and the charge and discharge current of the load capacitance.The transient power consumption can be calculated using equation 5.

$$P_T = C_{pd} \times {V_{CC}}^2 \times f_I \times N_{SW} \quad \textbf{(5)}$$

In case of single-bit switching, N_{SW} in equation 5 becomes 1.

Capacitive-Load Power Consumption

Additional power is consumed in charging of external load capacitance and is dependent on switching frequency. Equation 6 can be used to calculate this power while all outputs have the same load and are switching at the same output frequency.

$$P_L = C_L \times {V_{CC}}^2 \times f_O \times N_{SW} \text{ } (C_L \text{ is the load per output}) \quad \textbf{(6)}$$

In case of different loads and different output frequencies at all outputs, equation 7 is used to calculate capacitive-load power consumption.

$$P_L = \Sigma(C_{Ln} \times f_{On}) \times {V_{CC}}^2 \quad \textbf{(7)}$$

Therefore, dynamic power consumption (P_D) is the sum of these two power consumptions, and is expressed in equation 8 (single-bit-switching case) and 9 (multiple-bit switching with variable load and variable output frequencies):

$$P_D = \left(C_{pd} \times f_I \times {V_{CC}}^2\right) + \left(C_L \times f_O \times {V_{CC}}^2\right) \quad \textbf{(8)}$$

$$P_D = \left[\left(C_{pd} \times f_I \times N_{SW}\right) + \Sigma\left(C_{Ln} \times f_{On}\right)\right]{V_{CC}}^2 \quad \textbf{(9)}$$

Total power consumption with a CMOS-level input is the sum of static and dynamic power consumption.

TTL-Level Inputs

Similarly, with TTL-level inputs, both static and dynamic power consumption can be calculated using equations 10, 11, and 12.

$$P_S = V_{CC}[I_{CC} + (N_{TTL} \times \Delta I_{CC} \times DC_d)] \quad \textbf{(10)}$$

$$P_D = \left(C_{pd} \times f_I \times {V_{CC}}^2\right) + \left(C_L \times f_O \times {V_{CC}}^2\right) \text{ (single-bit switching)} \quad \textbf{(11)}$$

$$P_D = \left[\left(C_{pd} \times f_I \times N_{SW}\right) + \Sigma(C_{Ln} \times f_{On})\right]{V_{CC}}^2 \quad \textbf{(12)}$$

(multiple-bit switching with variable load and frequency)

BiCMOS

Static Power

$$P_S = V_{CC}\left\{DC_{en}\left[\left(N_H \times \frac{I_{CCH}}{N_T}\right) + \left(N_L \times \frac{I_{CCL}}{N_T}\right)\right] + (1 - DC_{en})I_{CCZ} + (N_{TTL} \times \Delta I_{CC} \times DC_d)\right\} \quad \textbf{(13)}$$

Where:

ΔI_{CC} = 0 for bipolar devices

NOTE:
For a continuous waveform at 50% duty cycle, DC_{en} = 1.

Equation 13 becomes:

$$P_S = V_{CC}\left[\left(N_H \times \frac{I_{CCH}}{N_T}\right) + \left(N_L \times \frac{I_{CCL}}{N_T}\right)\right] \quad (14)$$

NOTE:

If half of the time the waveform is high and half of the time the waveform is low and the waveform is switching continuously, $\Rightarrow (N_H = N_L = 1/2\ N_T)$, P_S becomes:

$$P_S = \left(\frac{V_{CC}}{2}\right)(I_{CCH} + I_{CCL}) \quad (15)$$

Dynamic Power

$$P_D = (DC_{em} \times N_{SW} \times V_{CC} \times f \times I_{CCD})\ \text{Condition is}\ 50\ \text{pF} \parallel 500\ \Omega \quad (16)$$

I_{CCD} is calculated with 50 pF || 500 Ω, and given number of outputs switching.

NOTE:

For a continuous waveform at 50% duty cycle, $DC_{en} = 1$.

Dynamic power with external capacitance:

$$P_D = DC_{en} \times N_{SW} \times V_{CC} \times f \times (V_{OH} - V_{OL}) \times (C_L - 50\ \text{pF}) + DC_{en} \times N_{SW} \times V_{CC} \times f \times I_{CCD} \quad (17)$$

I_{CCD} is calculated with 50 pF || 500 Ω, and given number of output switching.

Power is also consumed by the upper output driver due to the output resistor (500 Ω in most load circuits for outputs in the data sheet). This power is very small but must be included in the dynamic power consumption calculation. Equation 18 is used to calculate this power consumption.

$$P_{\_Res} = (V_{CC} - V_{OH}) \times \frac{V_{OH}}{R} \quad (18)$$

NOTE:

Assume that the output waveform is always at logic high and is not frequency dependent.

Therefore, total dynamic power consumption is:

$$P_{D\_TOT} = P_D + P_{\_Res} \quad (19)$$

Finally, total power consumption can be calculated as:

$$P_{\_Total} = P_{D\_TOT} + P_S \quad (20)$$

Where:

V_{CC} = supply voltage (V)
I_{CC} = power-supply current (A) (from the data sheet)
I_{CCL} = power-supply current when outputs are in low state (A) (from the data sheet)
I_{CCH} = power-supply current when outputs are in high state (A) (from the data sheet)
I_{CCZ} = power-supply current when outputs are in high-impedance state (A) (from the data sheet)
ΔI_{CC} = power-supply current when one input is at a TTL level (A) (from the data sheet)
DC_{en} = % duty cycle enabled (50% = 0.5)

DC_d = % duty cycle of the data (50% = 0.5)
N_H = number of outputs in high state
N_L = number of outputs in low state
N_{sw} = total number of outputs switching
N_T = total number of outputs

N_{TTL} = number of inputs driven at TTL levels

f_I = input frequency (Hz)
f_O = output frequency (Hz)
f = operating frequency (Hz)
V_{OH} = output voltage in high state (V)
V_{OL} = output voltage in low state (V)
C_L = external-load capacitance (F)
I_{CCD} = slope of the I_{CC} versus frequency curve (A/Hz × bit)

$C_{L(eff)}$ = effective-load capacitance (F)
f_O/f_I = ratio of output and input frequency (Hz)
P_T = transient power consumption
P_D = dynamic power consumption
P_S = static power consumption
$P_{\_Res}$ = power consumption due to output resistance
P_{D_TOT} = total dynamic power consumption
$P_{\_Total}$ = total power consumption

C_{PD} = dynamic power dissipation capacitance (F)
P_L = capacitive-load power consumption
Σ = sum of n different frequencies and loads at n different outputs
f_{On} = all different output frequencies at each output numbered 1 through n (Hz)
C_{Ln} = all different load capacitances at each output numbered 1 through n

For GTL and BTL/FB devices, the power consumption/calculation is similar to a BiCMOS device with the addition of the output power consumption through the pullup resistor, since GTL is open drain and BTL/FB is open collector.

The total power calculated using these equations should be less than the package power dissipation mentioned in the data sheets. Otherwise, the device might not function properly.

Benefits of Minimizing Power Consumption

Power consumption can be minimized in a number of ways. DC power consumption can be reduced to leakage by using only CMOS logic, as opposed to bipolar and BiCMOS logic. The leakage, in turn, is proportional to the area of diffusion, so the use of minimum-size devices is an advantage. Dynamic power consumption can be limited by reducing supply voltage, switched capacitance, and the frequency at which the logic is clocked. Supply voltage tends to be a system design consideration, and low-power systems use 1.5-V to 3.3-V supplies.

Power consumption is a function of the load capacitance, the frequency of operation, and the supply voltage. A reduction of any one of these is beneficial. A reduction in power consumption provides several other benefits. Less heat is generated, which reduces problems associated with high temperature, such as the need for heatsinks. This provides the consumer with a product that costs less. Furthermore, the reliability of the system is increased due to lower-temperature stress gradients on the device, and the integrity of the signal is improved due to the reduction of ground bounce and signal noise. An additional benefit of the reduced power consumption is the extended life of the battery in battery-powered systems.

Reliability Implications

The integrated-circuit component power dissipation during operation elevates the device junction temperature. The thermal impedance (θ_{JA} or k-factor) of a device package is defined as the increase in the junction temperature, above ambient temperature, due to the device power dissipation. Thermal impedance is measured in degrees Celsius per watt. Thermal characteristics of a device package are commonly described using two indices, Q_{JA} (junction to ambient) and Q_{JC} (junction to case). Controlling the junction temperature within a desired range is critical for proper device functionality and long-term reliability.

Table 4, based on long-term sustained temperatures, shows the relationship between junction temperature and predicted failure rate.

Table 4. Junction Temperature Versus 100,000-Hour Predicted Failure Rate

JUNCTION TEMPERATURE (°C)	FAILURE RATE (%)
100	0.02
110	1
120	11
130	46
140	80
150	96

Higher component temperatures increase the possibility of component wearout due to such failure mechanisms as electromigration and ball-bond intermetallic failures.

Thermal Definitions

Heat — A form of energy associated with the motion of atoms or molecules in solids, and capable of being transmitted through solid and fluid media by conduction, through fluid media by convection, and through empty space by radiation

Conduction Heating — The most commonly recognized form of heat transfer. Metal materials are good conductors of heat and can be quantified by a proportionality constant (k), also known as thermal conductivity. The higher the thermal-conductivity number, the more quickly heat transfer, by means of conduction, occurs. Leadframes are the primary media for conduction heating in plastic-encapsulated devices; however, mold compound materials play a major role in this type of heat transference.

Convection Heating — The heat transfer by fluid motion between regions of unequal density that result from nonuniform heating. This type of heat transfer is most commonly seen when air is forced across a heated surface, resulting in the cooling of the heat source. Heat is transferred to the air by means of convection heating. The rate of heat transfer depends on the surface area of the heat source and the velocity and physical properties of the airflow. When a device package is generating heat through normal operation, the device can be cooled by applying a constant airflow across the surface of the package.

Radiation — Radiant heat transfer occurs between two objects separated within a vacuum.

Ambient Temperature — The temperature of the surrounding air, usually used as a reference point to calculate the junction or case temperature. This temperature is measured at some specific distance from the device.

Case Temperature — The temperature on the package surface measured at the center of the top of the package

Junction Temperature — The temperature of the die inside the device package

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