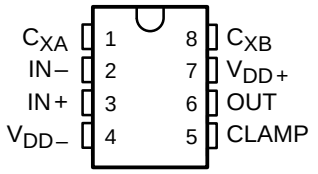
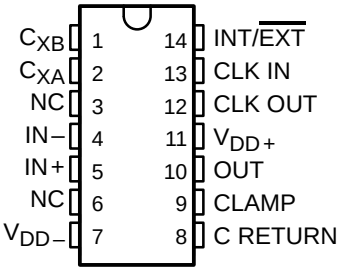
available features

- **Input Noise Voltage**
  - **0.5 μV p-p Typ, f = 0 to 1 Hz**
  - **1.5 μV p-p Typ, f = 0 to 10 Hz**
  - **47 nV/√Hz Typ, f = 10 Hz**
  - **13 nV/√Hz Typ, f = 1 kHz**
- **High Chopping Frequency . . . 10 kHz Typ**
- **No Clock Noise Below 10 kHz**
- **No Intermodulation Error Below 5 kHz**
- **Low Input Offset Voltage . . . 10 μV Max**
- **Excellent Offset Voltage Stability With Temperature . . . 0.05 μV/°C Max**
- **A_{VD} . . . 135 dB Min**
- **CMRR . . . 110 dB Min**
- **k_{SVR} . . . 120 dB Min**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**
- **No Noise Degradation With External Capacitors Connected to V_{DD-}**

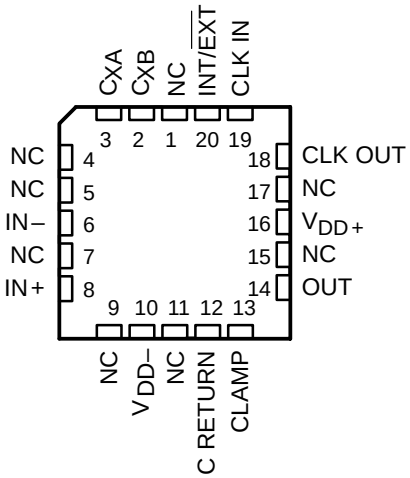
JG PACKAGE
(TOP VIEW)



J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLC2654M and TLC2654AM are low-noise chopper-stabilized operational amplifiers using the Advanced LinCMOS™ process. Combining this process with chopper stabilization circuitry makes possible excellent dc precision. In addition, circuit techniques are added that give the TLC2654M and TLC2654AM noise performance unsurpassed by similar devices.

Chopper-stabilization techniques provide for extremely high dc precision by continuously nulling input offset voltage even during variations in temperature, time, common-mode voltage, and power supply voltage. The high chopping frequency of the TLC2654M and TLC2654AM provides excellent noise performance in a frequency spectrum from near dc to 10 kHZ. In addition, intermodulation or aliasing error is eliminated from frequencies up to 5 kHz.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE		
		8-PIN	14-PIN	20-PIN
		CERAMIC DIP (JG)	CERAMIC DIP (J)	CHIP CARRIER (FK)
–55°C to 125°C	10 μV	TLC2654AMJG	TLC2654AMJ	TLC2654AMFK
	20 μV	TLC2654MJG	TLC2654MJ	TLC2654MFK

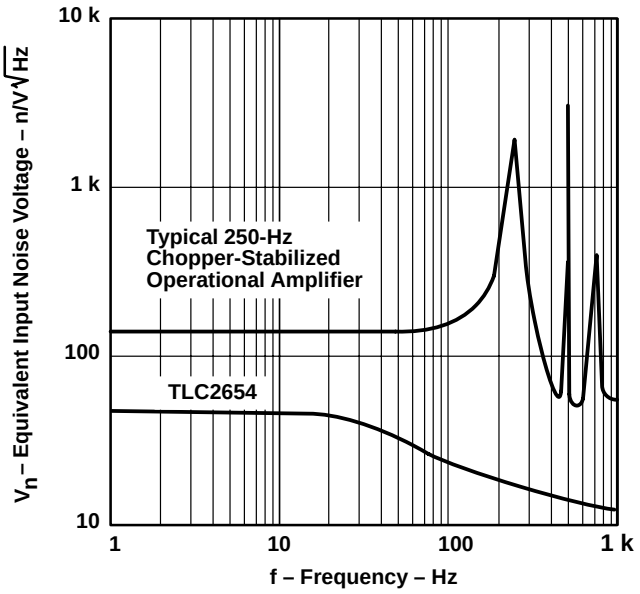
Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

This high dc precision and low noise, coupled with the extremely high input impedance of the CMOS input stage, makes the TLC2654M and TLC2654AM an ideal choice for a broad range of applications such as low-level, low-frequency thermocouple amplifiers and strain gauges, as well as wide-bandwidth and subsonic circuits. (For applications requiring even greater dc precision, use the TLC2652M or TLC2652AM device, which has a chopping frequency of 450 Hz.)

The TLC2654M and TLC2654AM input common-mode input voltage range includes the negative rail, thereby providing superior performance in either single-supply or split-supply applications, even at power supply voltage levels as low as ±2.3 V.

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY



Two external capacitors are required to operate the device; however, the on-chip chopper control circuitry is transparent to the user. On devices in the 14-pin and 20-pin packages, the control circuitry is accessible, allowing the user the option of controlling the clock frequency with an external frequency source. In addition, the clock threshold of the TLC2654M and TLC2654AM requires no level shifting when used in the single-supply configuration with a normal CMOS or TTL clock input.

Innovative circuit techniques used on the TLC2654M and TLC2654AM allow exceptionally fast overload recovery time. An output clamp pin is available to reduce the recovery time further.

The device inputs and output are designed to withstand –100-mA surge currents without sustaining latch-up. In addition, the TLC2654M and TLC2654AM incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

The TLC2654M and TLC2654AM are characterized for operation over the full military temperature range for –55°C to 125°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD+} (see Note 1) . . . . . 8 V
Supply voltage V_{DD-} (see Note 1) . . . . . −8 V
Differential input voltage (see Note 2) . . . . . ±16 V
Input voltage range, V_I (any input, see Note 1) . . . . . ±8 V
Voltage range on CLK IN and INT/$\overline{EXT}$ pins . . . . . V_{DD-} to V_{DD-} + 5.2 V
Input current, I_I (each input) . . . . . ±5 mA
Output current, I_O . . . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . unlimited
Current into CLK IN and INT/$\overline{EXT}$ pins . . . . . ±5 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . −55 °C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: J or JG package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 125°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	275 mW
J	1375 mW	11.0 mW/°C	275 mW
JG	1050 mW	8.4 mW/°C	210 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{DD\pm}$	±2.3	±8	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} −2.3	V
Clock input voltage	V_{DD-}	V_{DD-} +5	V
Operating free-air temperature, T_A	−55	125	°C

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2654M			TLC2654AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage (see Note 4)	V_{IC} = 0, R_S = 50 Ω	25°C		5	20		4	10	μV
			Full range			50			40	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.004	0.3*		0.004	0.3*	μV/°C
	Input offset voltage long-term drift (see Note 5)		25°C		0.003	0.06*		0.003	0.02*	μV/mo
I_{IO}	Input offset current		25°C		30			30		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		50			50		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ, See Note 6	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ, See Note 6	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 10 kΩ	25°C	120	155		135	155		dB
			Full range	120			120			
f_{ch}	Internal chopping frequency		25°C		10			10		kHz
	Clamp on-state current	V_O = ±5 V	25°C	25			25			μA
			Full range	25			25			
	Clamp off-state current	R_L = 100 kΩ	25°C			100			100	pA
			Full range			500			500	
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	105	125		110	125		dB
			Full range	105			110			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.3 V to ±8 V, V_O = 0, R_S = 50 Ω	25°C	110	125		120	125		dB
			Full range	105			115			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.5	2.1		1.5	2.1	mA
			Full range			2.2			2.2	

* This parameter is not production tested.
† Full range is −55° to 125°C.

NOTES: 4. This parameter is not production tested. Thermocouple effects preclude measurement of the actual V_{IO} of these devices in high-speed automated testing. V_{IO} is measured to a limit determined by the test equipment capability at the temperature extremes. The test ensures that the stabilization circuitry is performing properly.
5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
6. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR+	Positive slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.5	2		V/μs
			Full range	1.1			
SR–	Negative slew rate at unity gain		25°C	2.3	3.7		V/μs
			Full range	1.3			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		47		nV/√Hz
		f = 1 kHz	25°C		13		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.5		μV
		f = 0 to 10 Hz	25°C		1.5		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°		

† Full range is –55°C to 125°C.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage Normalized input offset voltage	Distribution vs Chopping frequency	1 2
I_{IO}	Input offset current	vs Chopping frequency vs Temperature	3 4
I_{IB}	Input bias current	vs Common-mode voltage vs Chopping frequency vs Temperature	5 6 7
	Clamp current	vs Output voltage	8
V_{OM}	Maximum peak output voltage swing	vs Output current vs Temperature	9 10
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	vs Frequency	11
CMRR	Common-mode rejection ratio	vs Frequency	12
A_{VD}	Differential voltage amplification	vs Frequency vs Temperature	13 14
f_{ch}	Chopping frequency	vs Supply voltage vs Temperature	15 16
I_{DD}	Supply current	vs Supply voltage vs Temperature	17 18
I_{OS}	Short-circuit output current	vs Supply voltage vs Temperature	19 20
SR	Slew rate	vs Supply voltage vs Temperature	21 22
	Pulse response	Small signal Large signal	23 24
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	vs Chopping frequency	25, 26
V_n	Equivalent input noise voltage	vs Frequency	27
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	28
	Gain-bandwidth product	vs Supply voltage vs Temperature	29 30
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance	31 32
	Phase shift	vs Frequency	13

TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLC2654M
INPUT OFFSET VOLTAGE**

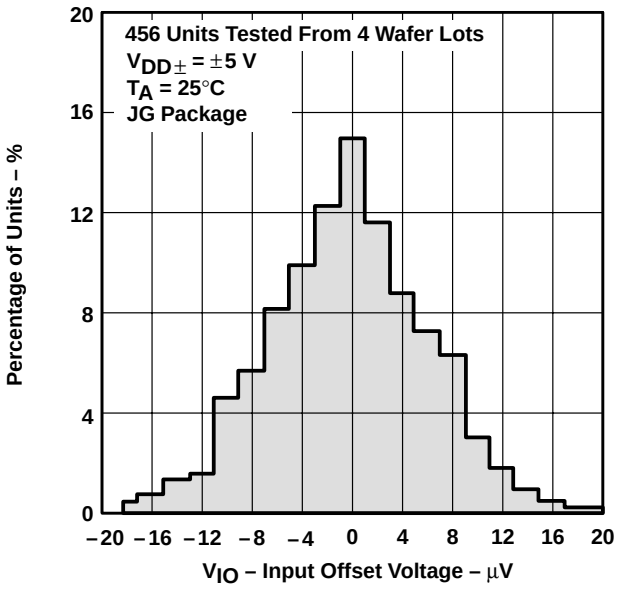


Figure 1

**NORMALIZED INPUT OFFSET VOLTAGE
vs
CHOPPING FREQUENCY**

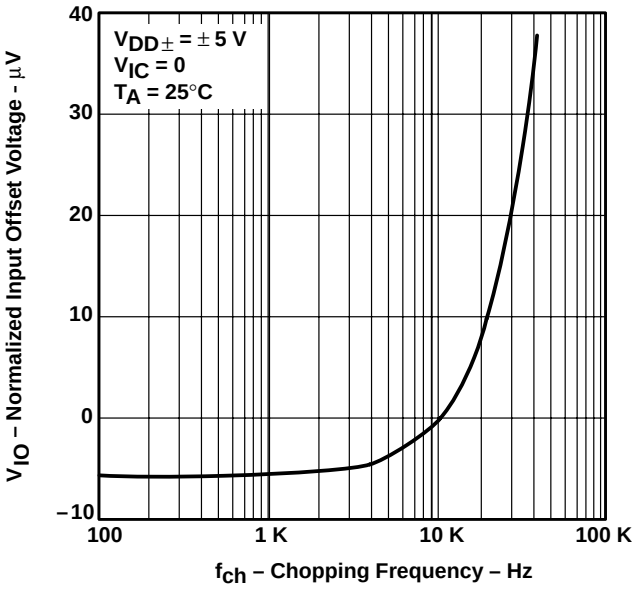


Figure 2

**INPUT OFFSET CURRENT
vs
CHOPPING FREQUENCY**

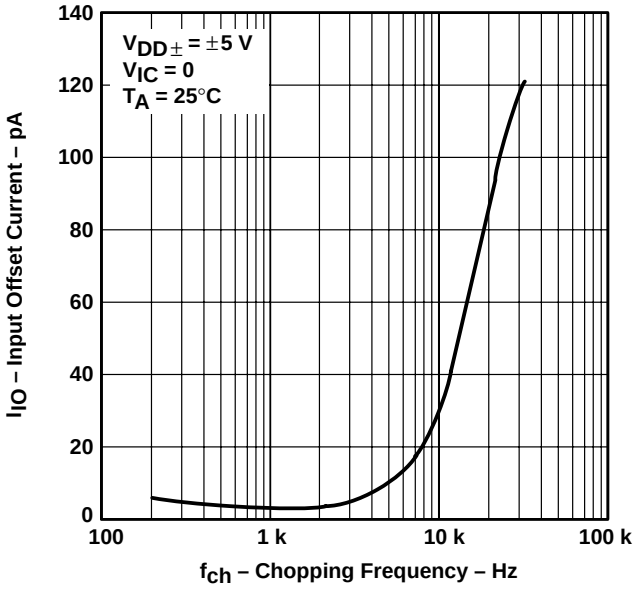


Figure 3

**INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE**

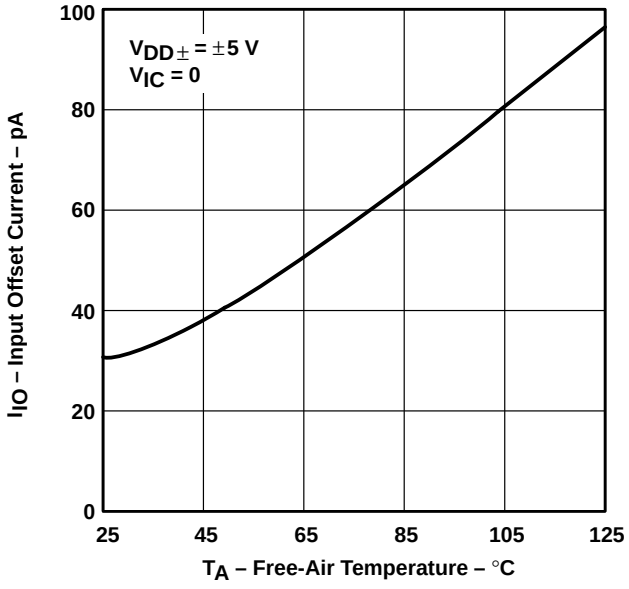


Figure 4

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

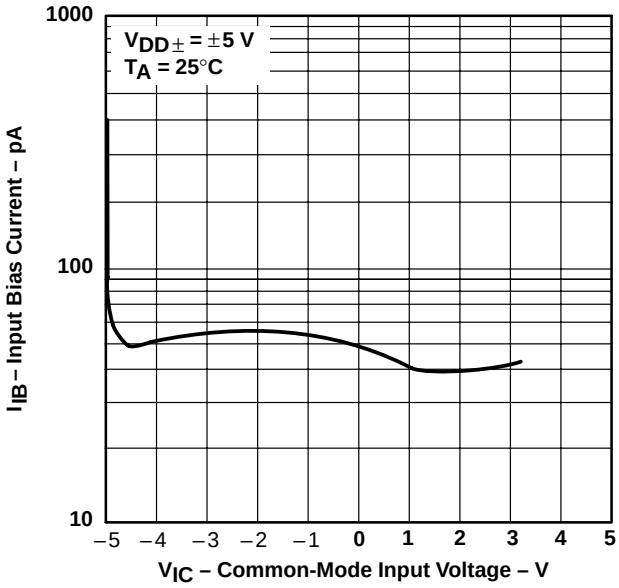


Figure 5

INPUT BIAS CURRENT vs CHOPPING FREQUENCY

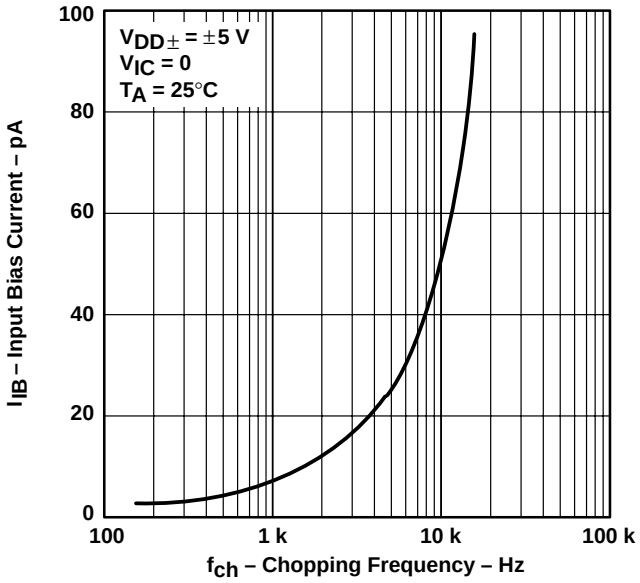


Figure 6

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

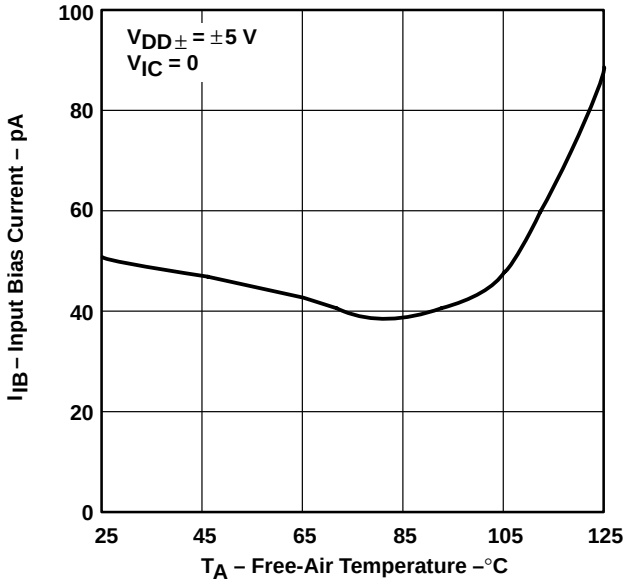


Figure 7

CLAMP CURRENT vs OUTPUT VOLTAGE

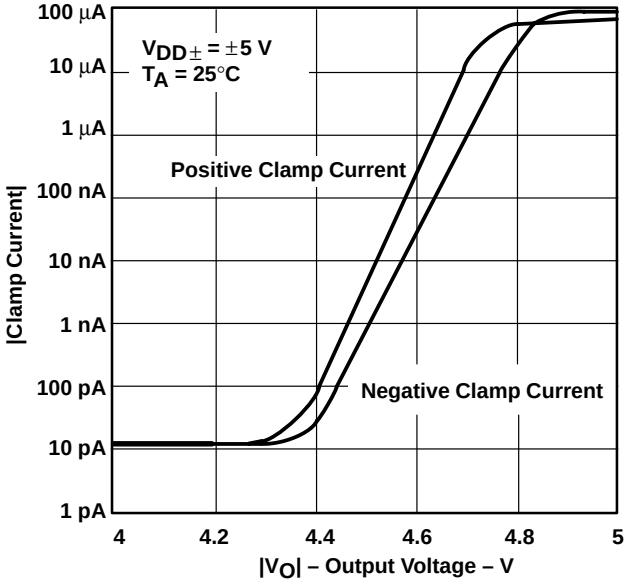


Figure 8

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

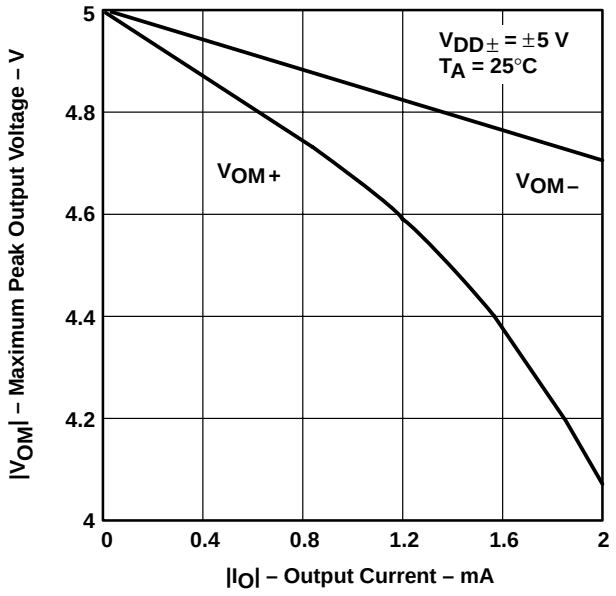


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

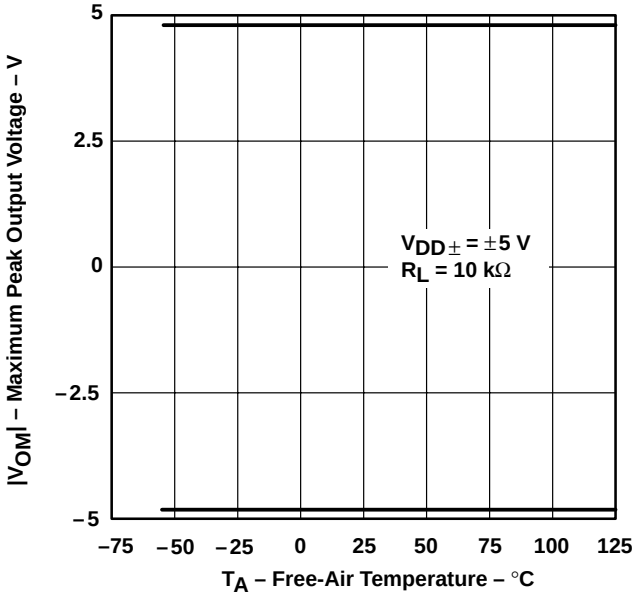


Figure 10

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

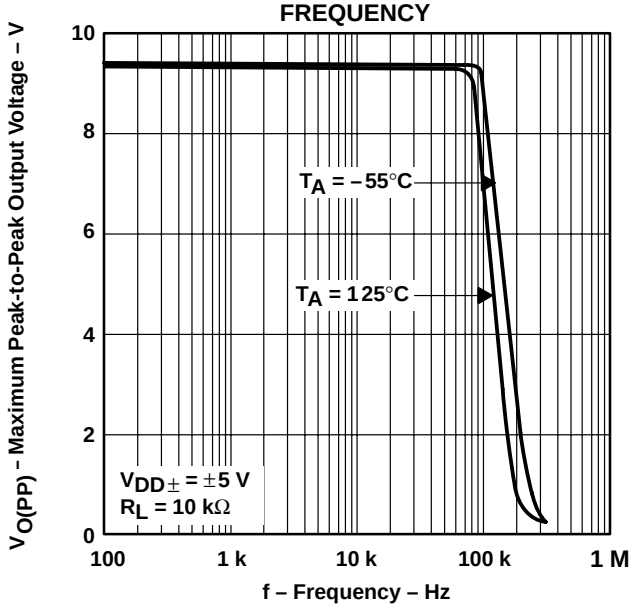


Figure 11

COMMOM-MODE REJECTION RATIO vs FREQUENCY

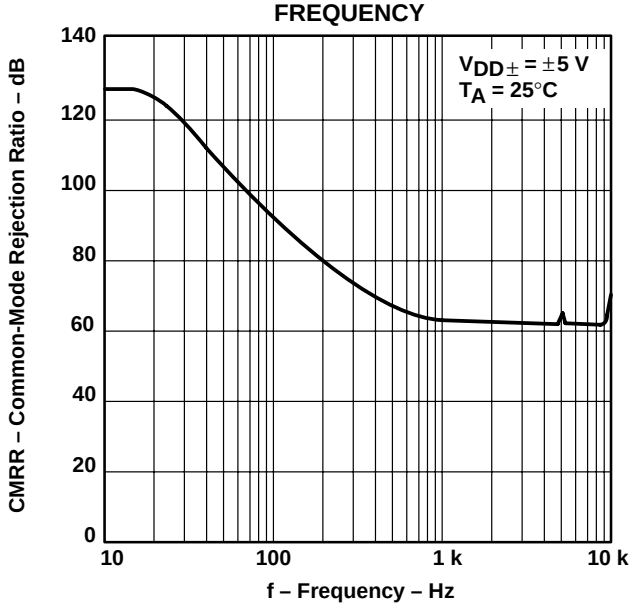


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

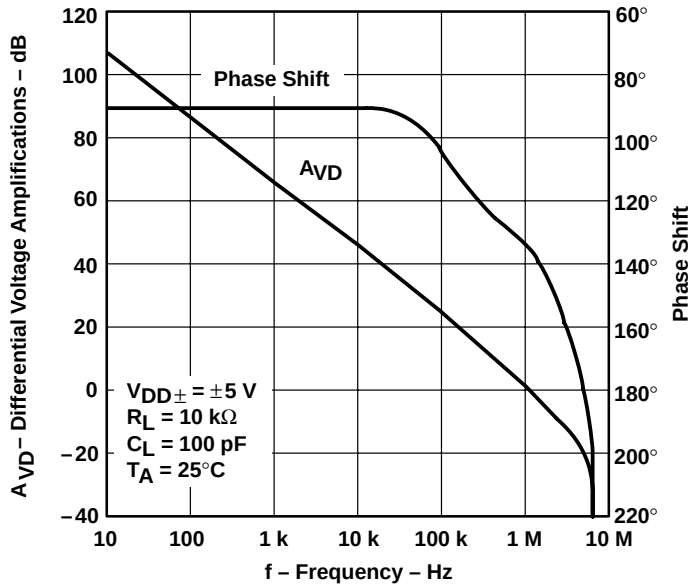


Figure 13

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

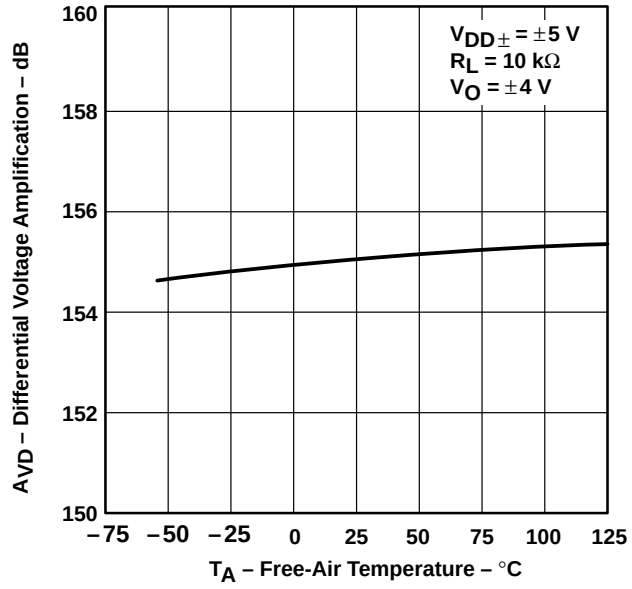


Figure 14

CHOPPING FREQUENCY vs SUPPLY VOLTAGE

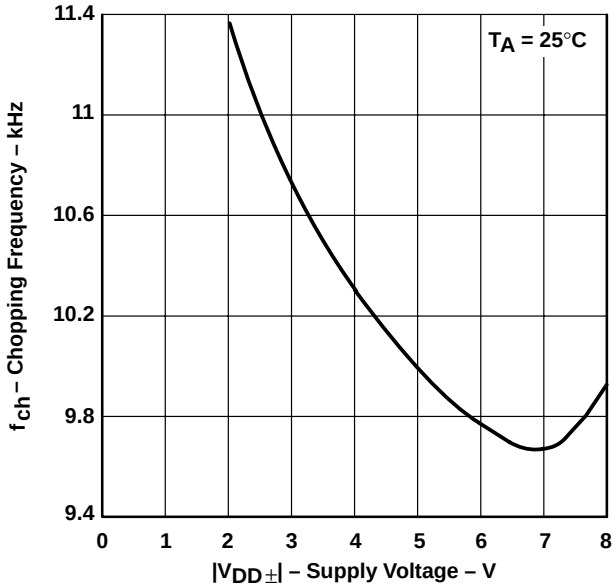


Figure 15

CHOPPING FREQUENCY vs FREE-AIR TEMPERATURE

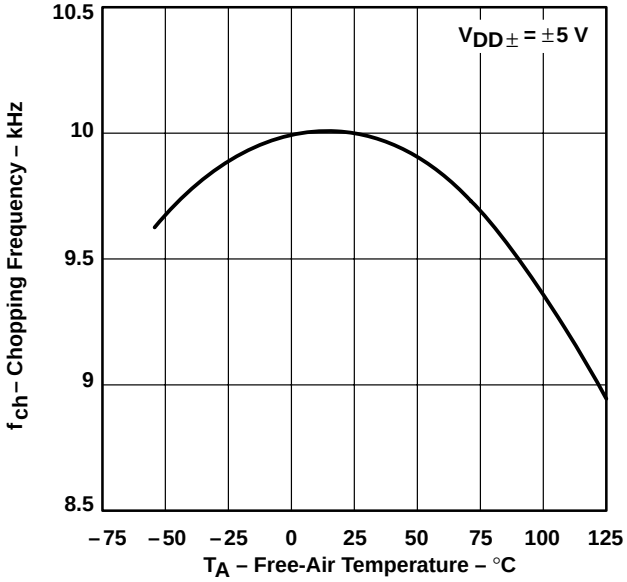


Figure 16

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

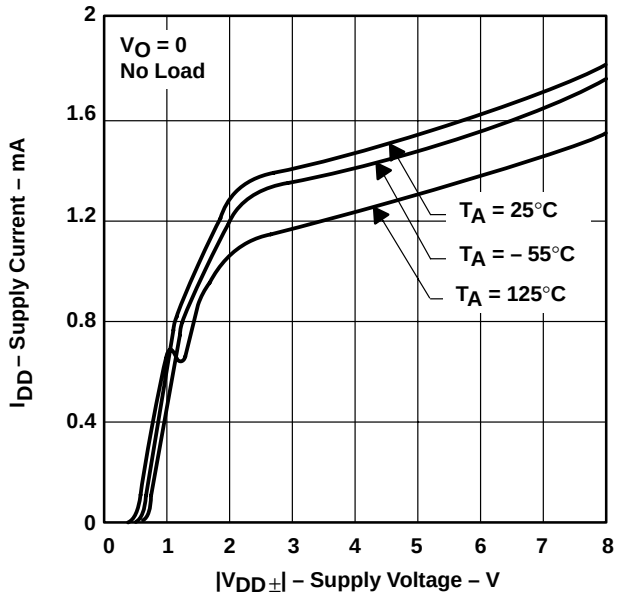


Figure 17

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

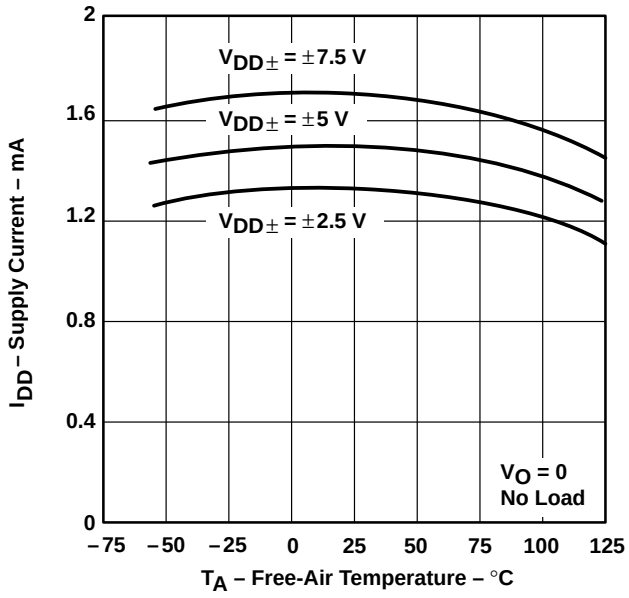


Figure 18

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

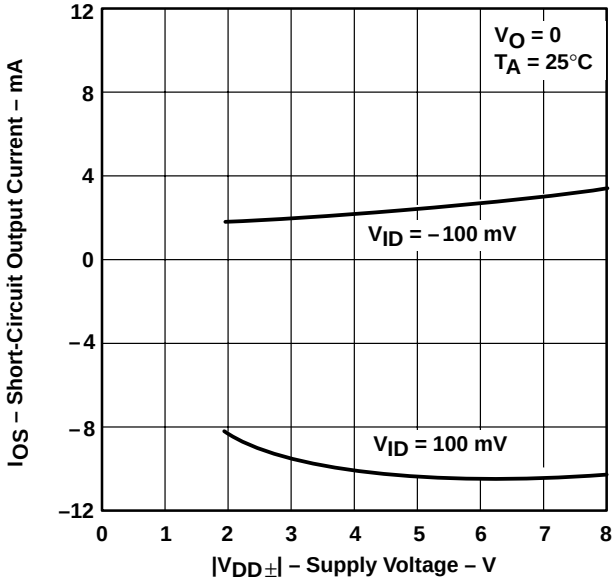


Figure 19

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

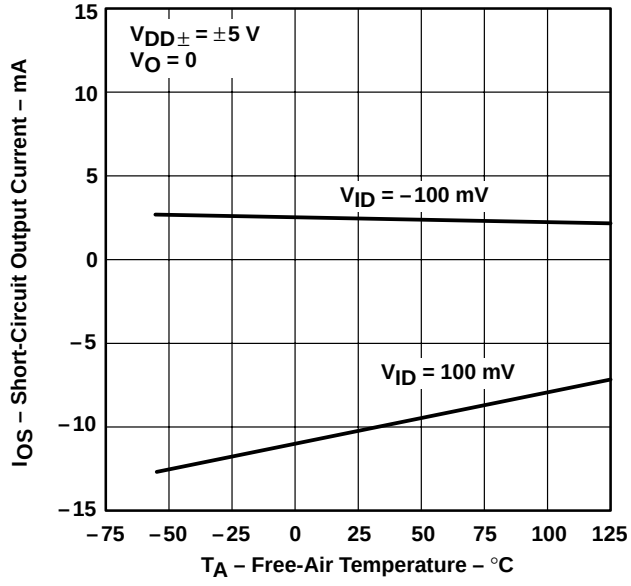


Figure 20

TYPICAL CHARACTERISTICS

SLEW RATE vs SUPPLY VOLTAGE

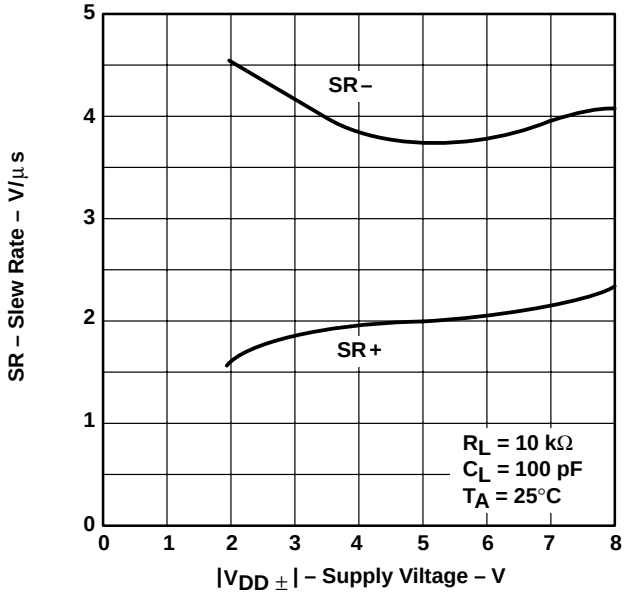


Figure 21

SLEW RATE vs FREE-AIR TEMPERATURE

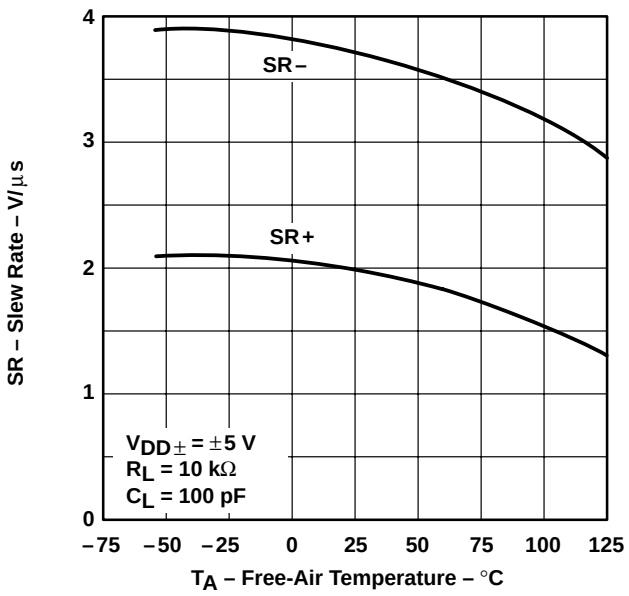


Figure 22

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

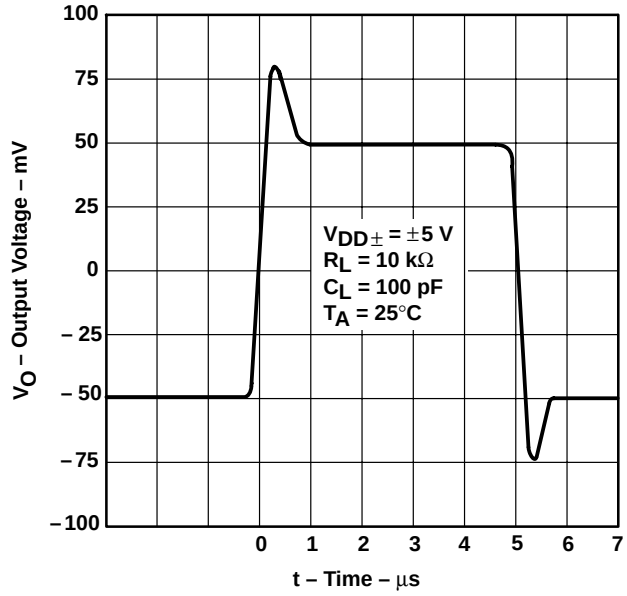


Figure 23

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

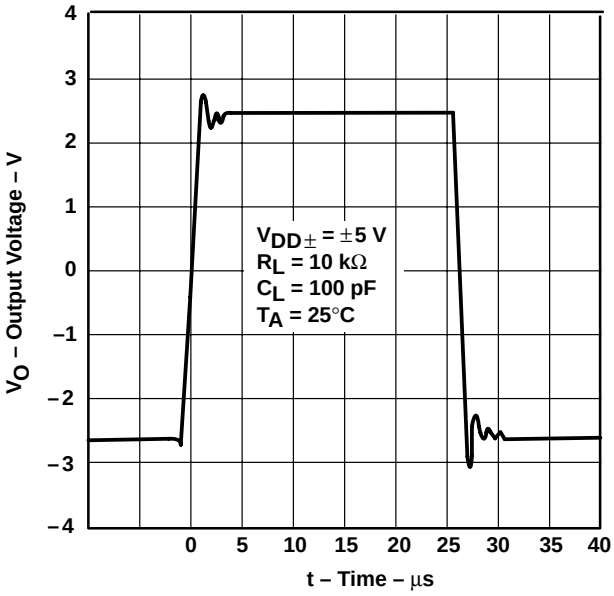


Figure 24

TYPICAL CHARACTERISTICS

PEAK-TO-PEAK INPUT NOISE VOLTAGE vs CHOPPING FREQUENCY

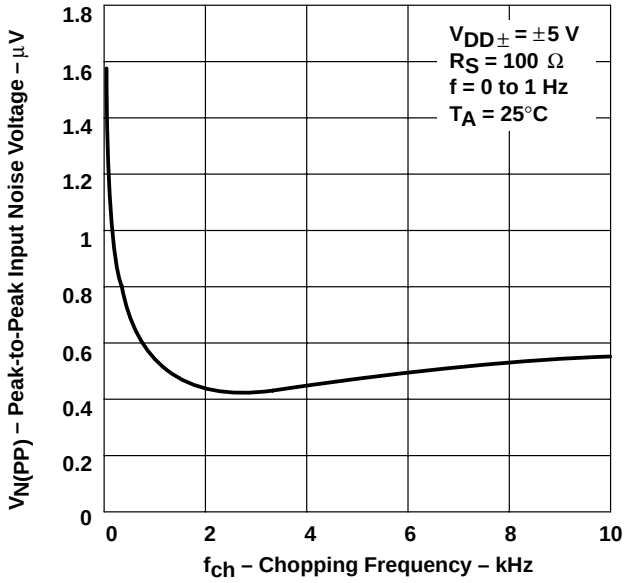


Figure 25

PEAK-TO-PEAK INPUT NOISE VOLTAGE vs CHOPPING FREQUENCY

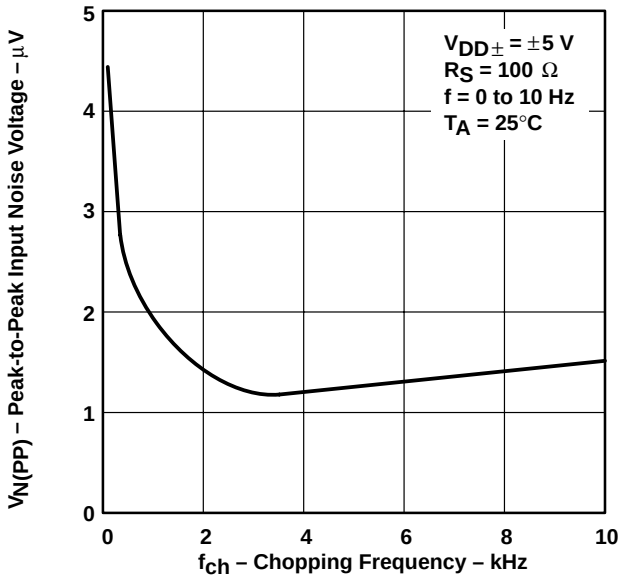


Figure 26

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

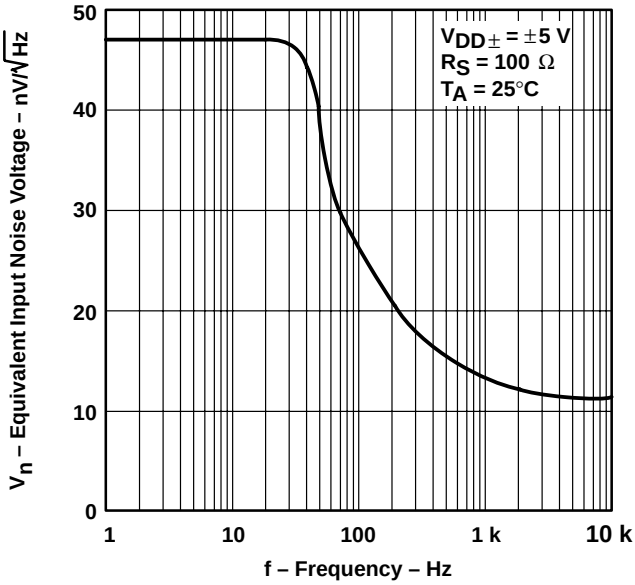


Figure 27

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

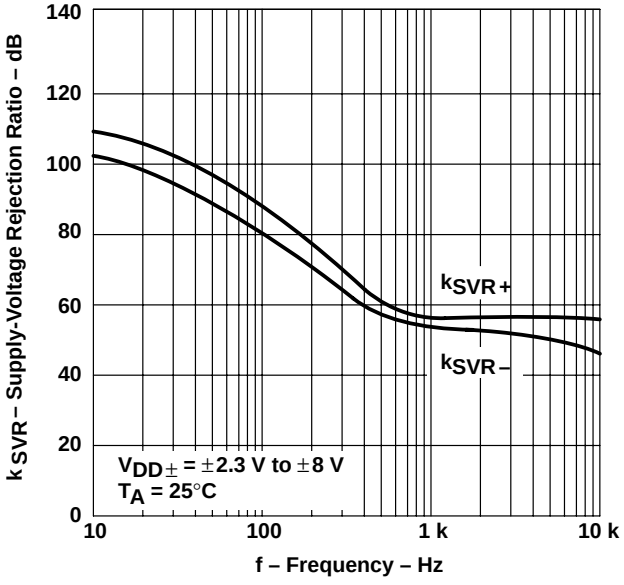


Figure 28

TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

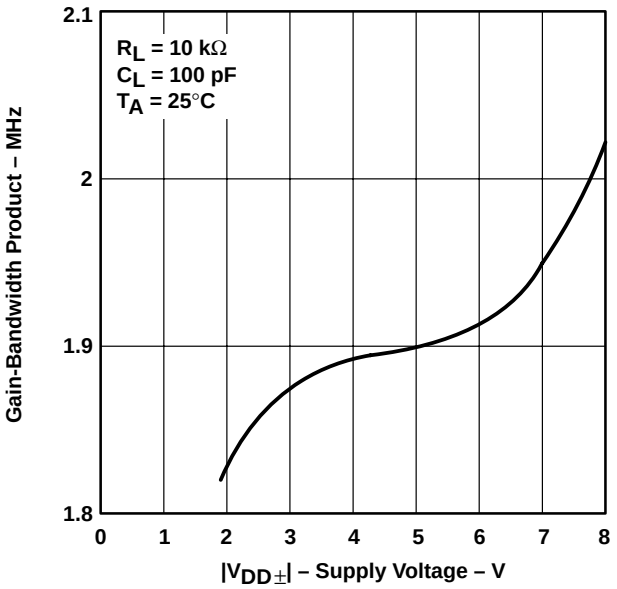


Figure 29

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

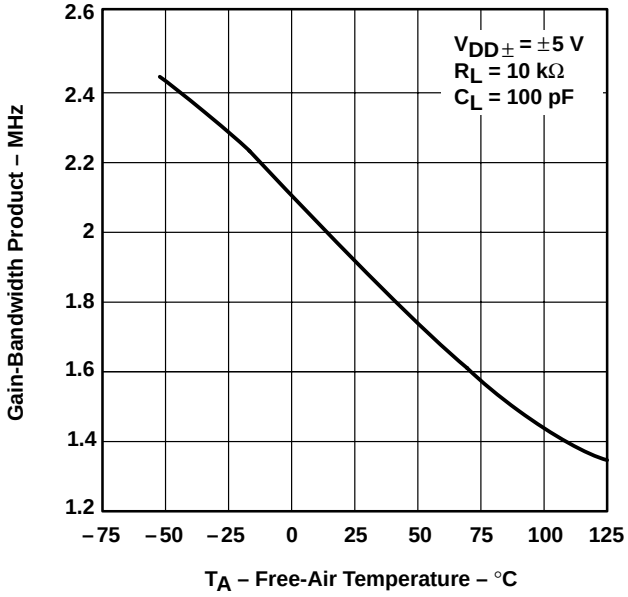


Figure 30

PHASE MARGIN vs SUPPLY VOLTAGE

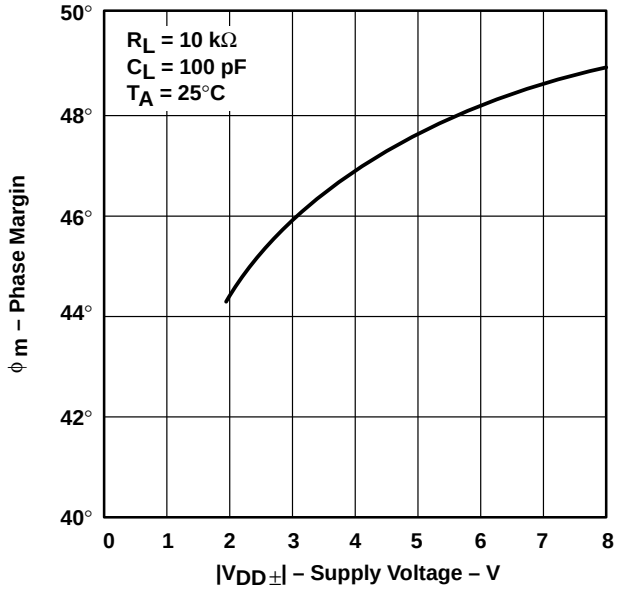


Figure 31

PHASE MARGIN vs LOAD CAPACITANCE

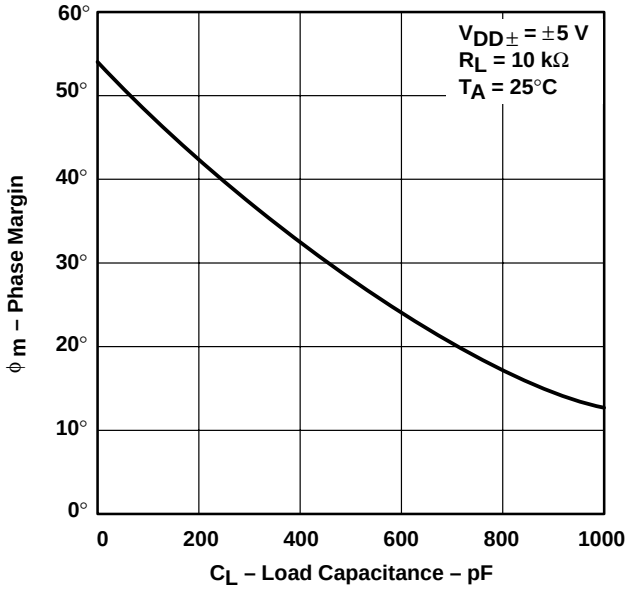


Figure 32

APPLICATION INFORMATION

capacitor selection and placement

Leakage and dielectric absorption are the two important factors to consider when selecting external capacitors C_{XA} and C_{XB}. Both factors an cause system degradation negating the performance advantages realized by using the TLC2654M.

Degradation from capacitor leakage becomes more apparent with the increasing temperatures. Low-leakage capacitors and standoffs are recommended for operation at T_A = 125°C. In addition, guard bands around the capacitor connections on both sides of the printed circuit board are recommended to alleviate problems caused by surface leakage on circuit boards.

Capacitors with high-dielectric absorption tend to take several seconds to settle upon application of power, which directly affects input offset voltage. In applications needing fast settling of input voltage, it is recommended that high-quality film capacitors, such as mylar, polystyrene, or polyproylene, be used. In other applications, however, a ceramic or other low-grade capacitor may suffice.

Unlike many choppers available today, the TLC2654M is designed to function with values of C_{XA} and C_{XB} in the range of 0.1 µF to 1 µF without degradation to input offset voltage or input noise voltage. These capacitors should be located as close as possible to the C_{XA} and C_{XB} pins and return to either the V_{DD-} pin or the C RETURN pin. Note that on many choppers, connecting these capacitors to the V_{DD-} pin causes degradation in noise performance, a problem that is eliminated on the TLC2654M.

internal/external clock

The TLC2654M has an internal clock that sets the chopping frequency to a nominal value of 10 kHz. On 8-pin packages, the chopping frequency can only be controlled by the internal clock; however, on all 14-pin packages and 20-pin FK package, the device chopping frequency may be set by the internal clock or controlled externally by use of the INT/$\overline{\text{EXT}}$ and CLK IN pins. To use the internal 10-kHz clock, no connection is necessary. If external clocking is desired, connect the INT/$\overline{\text{EXT}}$ pin to V_{DD-} and the external clock to CLK IN. The external clock trip point is 2.5 V above the negative rail; however, the CLK IN pin may be driven from the negative rail to 5 V above the negative rail. This allows the TLC2654M to be driven directly by 5-V TTL and CMOS logic when operating in the single-supply configuration. If this 5-V level is exceeded, damage could occur to the device unless the current into the CLK IN pin is limited to ±5 mA. A divide-by-two frequency divider interfaces with the CLK IN pin and sets the chopping frequency. The chopping frequency appears on the CLK OUT pin.

overload recovery/output clamp

When large differential input voltage conditions are applied to the TLC2654M, the nulling loop attempts to prevent the output from saturating by driving C_{XA} and C_{XB} to internally-clamped voltage levels. Once the overdrive condition is removed, a period of time is required to allow the built-up charge to dissipate. This time period is defined as overload recovery time (see Figure 33). Typical overload recovery time is significantly faster than competitive products; however, if required, this time can be reduced further by use of internal clamp circuitry accessible through the CLAMP pin.

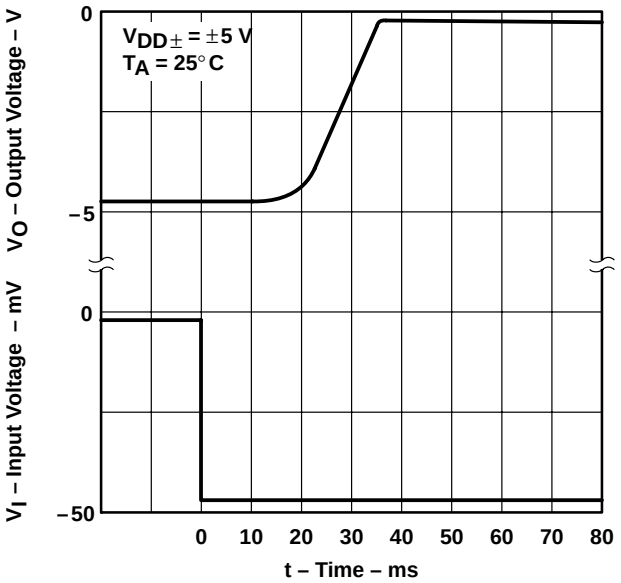


Figure 33. Overload Recovery

APPLICATION INFORMATION

overload recovery/output clamp (continued)

The clamp is simply a switch that is automatically activated when the output is approximately 1 V from either supply rail. When connected to the inverting input (in parallel with the closed-loop feedback resistor), the closed-loop gain is reduced and the TLC2654M output is prevented from going into saturation. Since the output must source or sink current through the switch (see Figure 8), the maximum output voltage swing is slightly reduced.

thermoelectric effects

To take advantage of the extremely low offset voltage temperature coefficient of the TLC2654M, care must be taken to compensate for the thermoelectric effects present when two dissimilar metals are brought into contact with each other (such as device leads being soldered to a printed circuit board). It is not uncommon for dissimilar metal junctions to produce thermoelectric voltages in the range of several microvolts per degree Celsius (orders of magnitude greater than the 0.01-μV/°C typical of the TLC2654M).

To help minimize thermoelectric effects, careful attention should be paid to component selection and circuit board layout. Avoid the use of nonsoldered connections (such as sockets, relays, switches, etc.) in the input signal path. Cancel thermoelectric effects by duplicating the number of components and junctions in each device input. The use of low-thermoelectric-coefficient components, such as wire-wound resistors, is also beneficial.

latch-up avoidance

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC2654 inputs and output are designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques to reduce the chance of latch-up should be used whenever possible. Internal protection diodes should not be forward biased in normal operation. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be stunted by using decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the supply rails and is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor. The chance of latch-up occurring increases with increasing temperature and supply voltage.

electrostatic discharge protection

The TLC2654M incorporates internal ESD-protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices, as exposure to ESD may result in degradation of the device parametric performance.

theory of operation

Chopper-stabilized operational amplifiers offer the best dc performance of any monolithic operational amplifier. This superior performance is the result of using two operational amplifiers – a main amplifier and a nulling amplifier – plus oscillator-controlled logic and two external capacitors to create a system that behaves as a single amplifier. With this approach, the TLC2654M achieves submicrovolt input offset voltage, submicrovolt noise voltage, and offset voltage variations with temperature in the nV/°C range.

APPLICATION INFORMATION

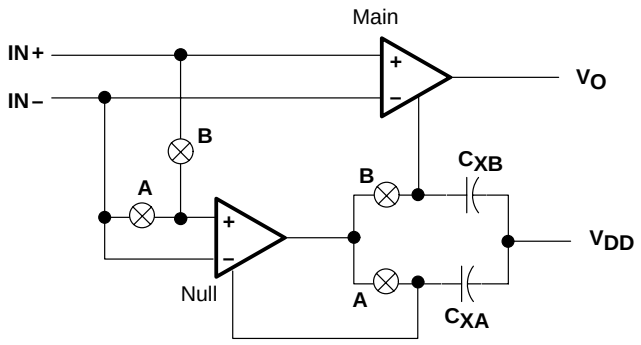


Figure 34. TLC2654 Simplified Block Diagram

theory of operation (continued)

The TLC2654 on-chip control logic produces two dominant clock phases – a nulling phase and an amplifying phase. The term chopper-stabilized derives from the process of switching between these two clock phases. Figure 34 shows a simplified block diagram of the TLC2654M. Switches A and B are make-before-break types. During the nulling phase, switch A is closed, shorting the nulling amplifier inputs together and allowing the nulling amplifier to reduce its own input offset voltage by feeding its output signal back to an inverting input node.

Simultaneously, external capacitor C_{XA} stores the nulling potential to allow the offset voltage of the amplifier to remain nulled during the amplifying phase.

During the amplifying phase, switch B is closed, connecting the output of the nulling amplifier to a noninverting input of the main amplifier. In this configuration, the input offset voltage of the main amplifier is nulled. Also, external capacitor C_{XB} stores the nulling potential to allow the offset voltage of the main amplifier to remain nulled during the next nulling phase.

This continuous chopping process allows offset voltage nulling during variations in time and temperature over the common-mode input voltage range and power supply range. In addition, because the low-frequency signal path is through both the null and main amplifiers, extremely high gain is achieved.

The low-frequency noise of a chopper amplifier depends on the magnitude of the component noise prior to chopping and the capability of the circuit to reduce this noise while chopping. The use of the Advanced LinCMOS process, with its low-noise analog MOS transistors and patent-pending input stage design, significantly reduces the input noise voltage.

The primary source of nonideal operation in chopper-stabilized amplifiers is error charge from the switches. As charge imbalance accumulates on critical nodes, input offset voltage can increase, especially with increasing chopping frequency. This problem has been significantly reduced in the TLC2654M by use of a patent-pending compensation circuit and Advanced LinCMOS process.

The TLC2654M incorporates a feed-forward design that ensures continuous frequency response. Essentially, the gain magnitude of the nulling amplifier and compensation network crosses unity at the break frequency of the main amplifier. As a result, the high-frequency response of the system is the same as the frequency response of the main amplifier. This approach also ensures that the slewing characteristics remain the same during both the nulling and amplifying phases.

theory of operation (continued)

The primary limitation on ac performance is the chopping frequency. As the input signal frequency approaches the chopper's clock frequency, intermodulation (or aliasing) errors result from the mixing of these frequencies.

To avoid these error signals, the input frequency must be less than half the clock frequency. Most choppers available today limit the internal chopping frequency to less than 500 Hz in order to eliminate errors due to the charge imbalancing phenomenon mentioned previously. However, to avoid intermodulation errors on a 500-Hz chopper, the input signal frequency must be limited to less than 250 Hz. The TLC2654M removes this restriction on ac performance by using a 10-kHz internal clock frequency. This high chopping frequency allows amplification of input signals up to 5 kHz without errors due to intermodulation and greatly reduces low-frequency noise.

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