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Interfacing the TLV1572 Analog-to-Digital Converter to the TMS320C203 DSP

Application Report

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Interfacing the TLV1572 Analog to Digital Converter to the TMS320C203 DSP

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ABSTRACT

The interface from the analog domain to the digital domain can be a mystifying design problem. The hardware design and software must operate together to produce a complete, usable design. This application report offers a specific solution to the problem of interfacing between the Texas Instruments (TI™)TLV1572 10-bit serial-output analog-to-digital converter (ADC) and the TMS320C203 digital signal processor (DSP).

This report also serves as reference information for further development of hardware and software. The contents include a hardware schematic and associated program software, block and timing diagrams, a list of the DSP serial port signals and registers, and a program flow chart.

1 Product Support

1.1 Related Documentation

The following list specifies product names, part numbers, and literature numbers of corresponding TI documentation.

- TMS320C2xx User's Guide, Literature number SPRU127B
- TLV1572 2.7 V to 5.5 V, 10-Bit, 1.25 MSPS Serial ADC with Auto-Power-down Data Sheet, Literature number SLAS171

1.2 World Wide Web

Our World Wide Web site at www.ti.com contains the most up to date product information, revisions, and additions. Users registering with TI&ME can build custom information pages and receive new product updates automatically via email.

1.3 Contact Information

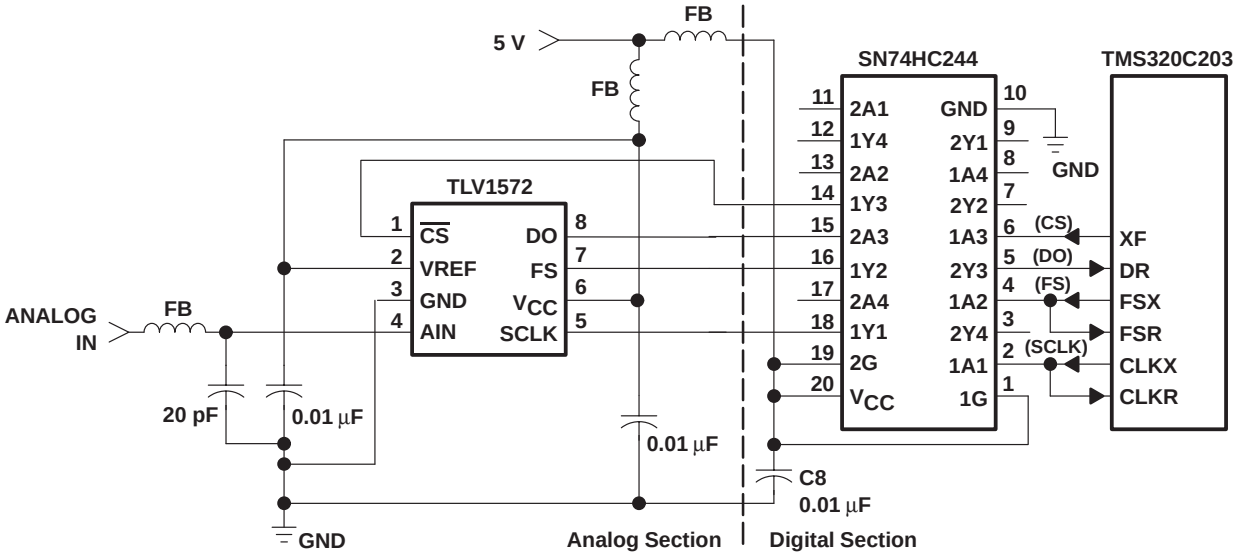
Americas Product Information Center	(972) 644–5580
US TMS320 hotline	(281) 274–2320
US TMS320 Fax	(281) 274–2324
US TMS320 BBS	(281) 274–2323
US TMS320 email	dsph@ti.com

2 Introduction

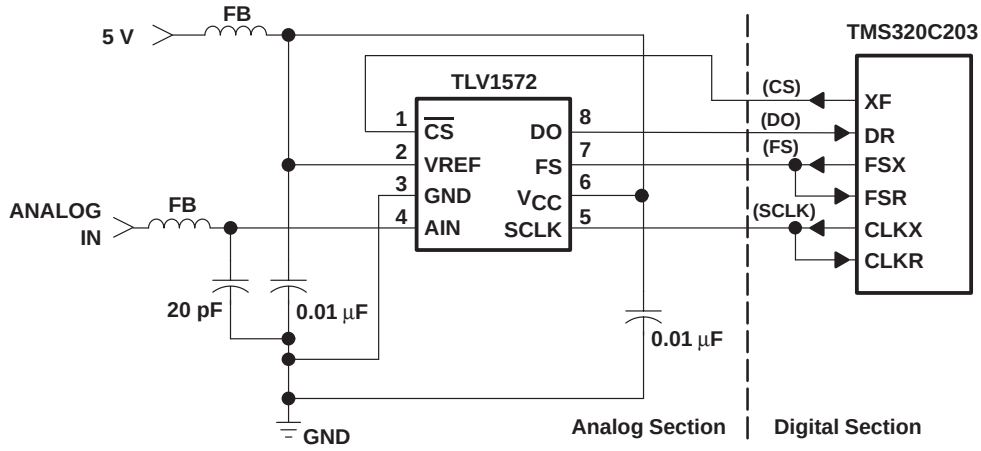
The hardware and software needed to implement the bridge between the system analog signals and the digital signal processing are described as follows.

- First, the basic operation of the TLV1572 is discussed.
- Second, the serial interface is described between the ADC and the DSP.
- Third, the software is discussed. The software application uses DSP internal interrupt processing and stores 256 conversion-result data-points for the analog input channel. The DSP serial port operates in Burst Mode.

Figure 1 shows the hardware schematic for connections with cabling (a) longer than 6 inches and (b) equal to or shorter than 6 inches. The leads should be kept as short as possible and the SCLK should have ground conductors on each side within the cable to minimize crosstalk.



(a) Hardware Connection with Cabling Longer than 6 Inches to the DSP



(b) Hardware Connection with Cabling Equal to or Shorter than 6 Inches to the DSP

NOTES: 1. FB is a ferrite bead, Fair-Rite™ #2744044447 or equivalent.
2. Bypass capacitors for terminals VREF and V_{CC} should be as close to the device pins as possible.

Figure 1. TLV1572 to DSP Serial Port Hardware Connection

Fair-Rite™ is a registered trademark of Fair–Rite Products Corporation.

3 TLV1572 Overview

The TLV1572 is a 10–bit successive approximation analog–to digital converter (ADC), as shown in Figure 2. The TLV1572 has one analog input (AIN), chip-select ($\overline{CS}$), serial clock (SCLK), and serial data output (DO).

An additional input, called frame sync (FS), initiates data transfer when using a DSP and connects to the DSP serial port FSX pin.

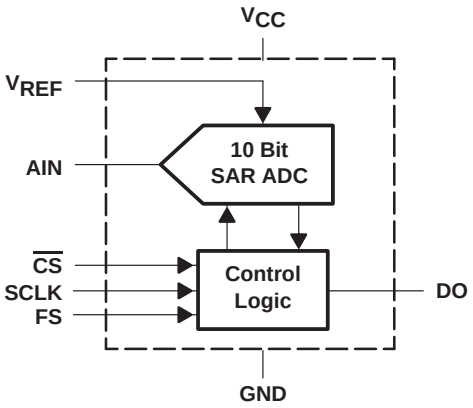


Figure 2. TLV1572 Functional Block Diagram

3.1 Operational Overview

3.2 Signal Sequence

As shown in the timing sequence in Figure 3, a high level on the $\overline{CS}$ pin initiates a power-down for the TLV1572 and SCLK takes DO to a high impedance state. When taken low, $\overline{CS}$ enables the device inputs, but no data is transferred until the falling edge of FSX is received from the DSP to FS.

After the falling edge of the DSP FSX, the TLV1572 starts shifting the data out on the DO line: first 6-null bits, then the 10-bit A/D conversion data.

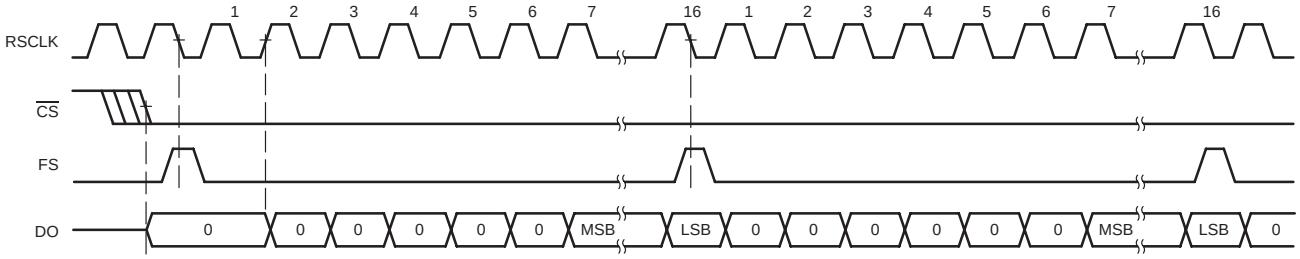


Figure 3. DSP Application Timing

3.3 Reference Voltage Inputs

The voltage applied from the VREF pin to ground defines the analog input range for the TLV1572. The voltage at VREF establishes the full scale limit where the analog input produces all 1s on the digital output. The GND pin at zero volts establishes the zero scale where the analog input produces all 0s on the digital output.

Input analog voltages exceeding the VREF will still produce all 1s and analog voltages below ground will still produce all 0s; however, the absolute maximum voltage applied to the VREF pin and the analog input should not exceed Vcc + 0.3 V or be lower than –0.3 V below circuit ground.

4 The ADC/DSP System

The software configures the DSP serial port to the 16-bit master mode so that the DSP generates the frame sync signal at FSX and the data clock at CLKX serial port terminals. From the hardware schematic, the connections between the DSP and the ADC are as follows:

Table 1. DSP/ADC Interconnection

FROM DSP	TO DSP	TO ADC	FROM ADC
FSX	FSR	FS	
CLKX	CLKR	SCLK	
	DR		DO
XF		$\overline{CS}$	

The following statements describe the generation and application of the configuration and control signals (see Figure 1 and Figure 2):

- The DSP CLKX output provides an 18.75 MHz data clock that is a divide by 2 of the DSP master clock.
- The DSP XF provides a high-to-low transition to start the TLV1572.
- The falling edge of the frame sync signal (FSX) of the DSP serial port initiates the data transfer between the DSP and the ADC.
- The TLV1572 DO serial output provides the digital conversion results to the DSP DR terminal.

Since this DSP/ADC interface is synchronous, the FSX signal is sent to the FSR terminal and the CLKX is sent to the CLKR terminal.

4.1 DSP Serial Port

The DSP serial port provides direct communication with serial I/O devices and consists of five registers and the following six basic signals:

CLKX Serial transmit clock. Clocks the transmitted data from the DX† terminal.

CLKR Serial receive clock. Clocks data into the DSP DR terminal provided from the TLV1572 DO terminal.

DX† Data transmit. From this terminal the DSP transmits 16 bit data to the input terminal of the ADC or other peripheral devices.

DR Data receive. The DSP receives 16 bit data from the DO terminal of the TLV1572 into this terminal.

FSX Frame sync transmit. Frames the transmit data. The DSP begins to transmit data from DX on the falling edge of FSX and continues to transmit data for the next 16 clock cycles from the CLKX terminal. The FSX signal is applied to the TLV1572 FS terminal.

FSR Frame sync receive. Frames the receive data. The DSP begins to receive data on the falling edge of FSR and continues to recognize valid data for the following 16 clocks from CLKR.

† DX is not used in this application since the TLV1572 requires no internal programming.

For information on the five registers, see the section, *DSP Serial Port Operation, in Chapter 9 of the TI TMS320C2xx User's Guide*.

Table 2 lists the serial port pins and registers.

Table 2. DSP Serial Port Signals and Registers

PINS	DESCRIPTION	REGISTER	DESCRIPTION
CLKX	Transmit clock signal	SSPCR	Synchronous serial port control register
CLKR	Receiver clock signal	SDTR	Synchronous data transmit and receive register
DX†	Transmitted serial data signal	XSR	Transmit shift register
DR	Received serial data signal	RSR	Receiver shift register
FSX	Transmit frame synchronization signal		
DSR	Receive frame synchronization signal		

† DX is not used in the TLV1572 application

For this application the DSP serial port is programmed as the master, so the CLKX output is fed to the CLKR terminal and the FSX output is fed to the FSR terminal.

4.2 DSP Internal Serial Port Operation:

Three signals are necessary to connect the transmit pins of the transmitting device with the receive pins of the receiving device for data transmission:

- DX† the transmitted serial data signal, sends the actual data.
- FSX initiates the transfer (at the beginning of the 16 bit packet).
- CLKX clocks the bit transfer.

† DX is not used in the TLV1572 application

The corresponding pins on the receive device are DR, FSR, and CLKR, respectively.

As shown in Figure 4, the transmit data is written to the SDTR transmit and received data is read from the SDTR receive. A transmit command is executed by writing data to the SDTR transmit FIFO buffer, which copies the data to the XSR when the XSR is empty.

The XSR manages the shifting of the data to the DX† pin, thus allowing another write to SDTR transmit as soon as the SDTR-to-XSR copy is completed. On completion of the SDTR-to-XSR copy, a 0–to-1 transition occurs on the XRDY bit in the SSPCR and generates a XINT.

The process is similar for receiving. On completion of the RSR-to-SDTR copy, a 0-to-1 transition occurs on the RRDY bit in the SSPCR and generates a RINT.

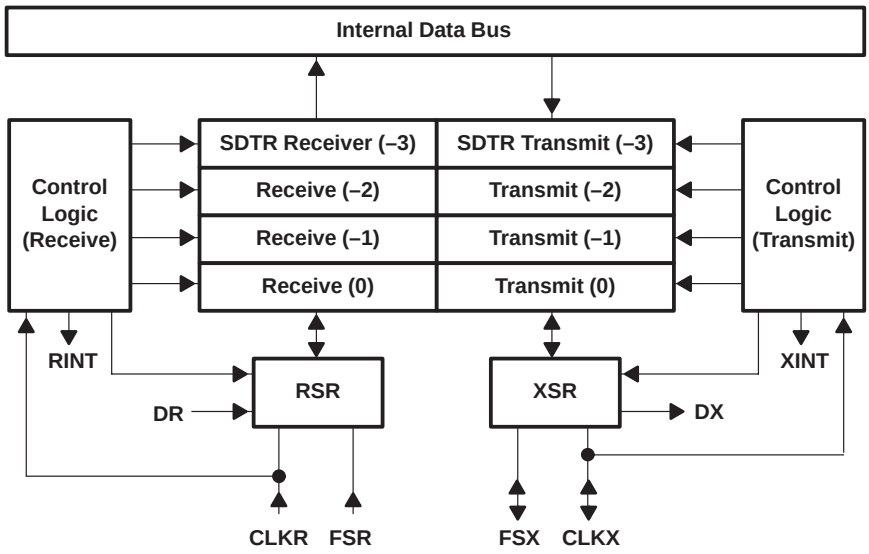


Figure 4. Internal DSP Serial Port Block Diagram

5 Software Overview

This interface program uses DSP internal interrupt processing using the RINT signal and stores 256 conversion result data-points for the analog input channel.

This program uses one of the DSP interrupts (RINT) to read and to store 256 data samples. Figure 5 shows the program flowchart.

The Crystal is 75 MHz, the CPU CLK for the C203 DSP is 37.5 MHz, SCLK for the TLV1572 is driven by CLKX, which is 18.75 MHz.

The program starts with a common initialization procedure for the DSP followed by the initialization of the serial port.

The following steps initialize the DSP:

1. Disable the global interrupts.
2. Set the data page pointer to 0h.
3. Set Starting Address.
4. Set number of samples.
5. Unmask (enable) RINT bit in IMR (Interrupt Mask Register).
6. Enable global interrupts.

The next two steps initialize the serial port.

Step 1: Set the Synchronous serial port control register to 0C00Eh (SSPCR=0C00Eh).

The individual bits within the SSPCR now contain the following functions:

⇒ The Frame Sync Mode bit is set to 1 (FSM=1) to allow Burst Mode operation.

⇒ The Clock Mode bit is set to 1 (MCM=1) to set the transmit clock CLKX to 1/2 of the DSP master clock of 37.5 MHz (CLKX frequency = 18.75 MHz)

⇒ The Transmit Mode bit is set to 1 (TXM=1) to generate the frame sync internally as required for the data transfer initiation. FSX is now programmed as an output.

⇒ The FREE and SOFT bits are set to 1. The clock continues to run at breakpoint.

Step 2: Set the Synchronous serial port control register to 0C03Eh (SSPCR=0C03Eh)

⇒ Writing 1s to the Transmitter Reset field (XRST) and to the Receiver Reset field (RRST) activates the serial port transmitter and receiver.

The program executes the following steps:

1. Initializes the C203 DSP
2. Initializes the serial port
3. On data transfer from RSR to SDTR, a RINT occurs that causes the DSP to send a Frame Sync to TLV1572, loading the content of SDTR (receive) into the memory.

4. After obtaining all data (ACC = 0), the DSP exits the loop subroutine.
5. The data is now available for use in customer defined functions (algorithms).

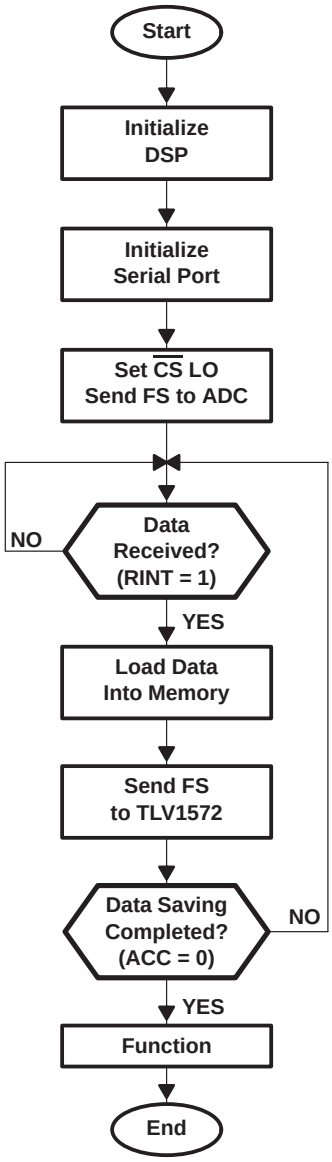


Figure 5. TLV1572 to TMS320C203 DSP Interface Program Flow Chart

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Appendix A Program Listing

```
; ************************************************************
; *       (C) COPYRIGHT TEXAS INSTRUMENTS, INC. 1997         *
; ************************************************************
; *                                                          *
; * File: 1572.ASM  Main routine                             *
; *                                                          *
; ************************************************************
       .title  ”TLV1572 ADC Interface routine”
; ************************************************************
; This routine allows the ’C2O3EVM to interface with an ADC on the
; Serial port of the DSP.
.mmregs
SDTR      .set   0fff0h
SSPCR     .set   0fff1h
temp0     .set   060h
temp1     .set   061h
       .ps    0
       B      start     ;0     RESET
       CLRC   INTM      ;2     HOLD/INT1
       RET
       CLRC   INTM      ;4     INT2/INT3
       RET
       CLRC   INTM      ;6     TINT
       RET
       B      rec_int   ;8     RINT go to “rec_int”

       .ps    1000h     ; Starting Program Address = 1000h
       .entry
start:
;**    DSP INITIALIZATION
       SETC   INTM            ;Disable global interrupts
       LDP    #0              ;Set data page pointer
       LAR    AR6, #1B00h     ;Starting address of sampling memory
       LACC   #100h           ;Taking 100h  ADC data
       MAR    *, AR6          ;Selecting AR6
       SPLK   #0008h, IMR     ;Unmasked RINT
       CLRC   INTM            ;nable global interrupts
;**    SERIAL PORT INITIALIZATION
       SPLK   #0c00eh, temp0   ;FREE=SOFT=TXM=MCM=FSM=1
       OUT    temp0, SSPCR
       SPLK   #0c03eh, temp0
```

```
       OUT    temp0, SSPCR     ;Activate Transmitter and Receiver

       SPLK   #0h, temp0       ;temp0 = 0
       CLRC   XF               ;Set XF and TLV1572's CS lo
       OUT    temp0,SDTR       ;Send FS to TLV1572
loop:
       IDLE                    ;Wait for RINT
       BCND   loop, GT         ;If ACC > 0, go to loop
       SPLK   #0000h, IMR      ;Mask RINT
;**
;**     FUNCTION(S)
;**
end_loop:
       NOP
       NOP
       B      end_loop
rec_int:
;**    RSR to SDTR complete, RINT active
       IN     *+, SDTR         ;Save SDTR to memory, (AR6) + 1
       OUT    temp0, SDTR      ;Send FS to TLV1572
       SUB    #1h              ;(ACC) – 1
       CLRC   INTM             ;Enable Interrupts
       RET
; END OF RECEIVING
       .end
```