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Switched-Capacitor ADC Analog Input Calculations Application Report

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Switched-Capacitor ADC Analog Input Calculations

ABSTRACT

This application report describes calculations to analyze the analog input circuit to a switched-capacitor analog-to-digital converter. The calculations determine the maximum value of the external driving source resistance to provide a desired ADC conversion accuracy.

1 Introduction

Many successive-approximation analog-to-digital converters (ADC) use the switched capacitor array architecture. To a first-order approximation ADC, the analog input of these converters can be represented electrically by a series resistor followed by a capacitor to ground as shown in Figure 1.

During the analog input sampling time, the capacitor is connected to the analog-driving source through an internal series resistor (series resistance of the internal switch). The following analysis relates this input circuit to the maximum value of the external driving source resistance to provide a desired ADC conversion accuracy.

Although using most op amps with a series resistor-capacitor load would produce a second order system, it is assumed that the resistance values within and external to the device are sufficient to prevent any overshoot. These results are generally valid for the TLC54x, TLC154x, and TLC254x ADC families.

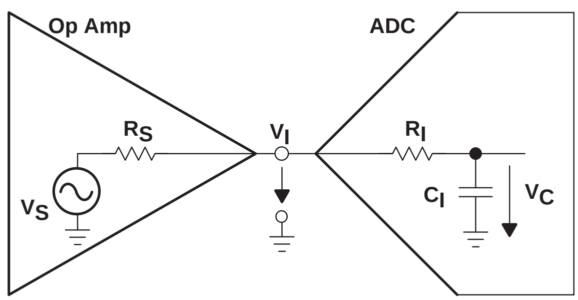

Figure 1. Equivalent Input Circuit Including the Driving Source

2 Maximum Driving Source Resistance

The input impedance to a switched capacitor input ADC is exponential in characteristic and cannot be treated as a constant impedance during the sampling interval. The maximum driving source resistance then also varies with the speed of the I/O clock.

The general equation for the maximum value of the source resistance is:

$$Rs = \frac{Ts \times TC}{tc \times Ci} - ri$$

Where

Ts = converter specific sampling time,
tc = charge time to achieve the required accuracy, and
TC = time constant of the entire RC network

The examples in this report show how to obtain the maximum value of analog source resistance for a desired ADC accuracy.

2.1 Analog Input Circuit Analysis

For the following analysis, assume that the capacitor voltage, Vc, needs to approach the source voltage, Vs, to within 1/16 of an LSB or by 6.25%, as shown in Figure 2. The accuracy represents less than 0.1 LSB error and allows for the consideration of additional, inherent errors, such as DNL and INL, while keeping the total conversion error within ±1/2 LSB.

Using the equivalent circuit in Figure 1, the time required to charge the analog input capacitance from 0 volts to the input analog voltage, Vs, to within 1/16 of an LSB can be derived as follows:

$$Vc = Vs\left(1 - e^{\frac{-tc}{Rt \times Ci}}\right) \qquad (1)$$

with *Vc* = voltage across *Ci and*

$$Rt = Rs + ri \qquad (2)$$

Where

Rs = source resistance and
ri = ADC input series resistance

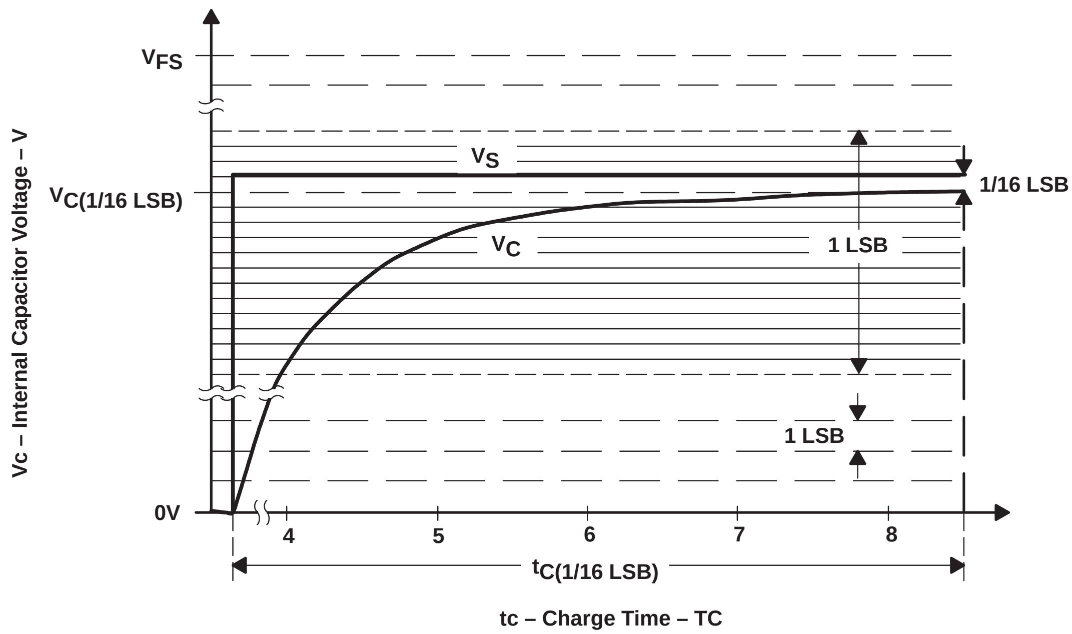

Figure 2. Internal Capacitor Voltage, Vc, as a Function of the Charge Time, tc

The final capacitor voltage to achieve 1/16 LSB is given by:

$$Vc_{1/16} = Vs - \frac{Vs}{2^{N+4}} = Vs\left(1 - \frac{1}{2^{N+4}}\right) \tag{3}$$

where *N* is the resolution of the converter and *4* is the equivalent number of additional resolution bits to resolve one LSB into 16 levels to achieve the accuracy of 1/16 of an LSB.

Now equating equation (1) to equation (3):

$$Vs\left(1 - \frac{1}{2^{N+4}}\right) = Vs\left(1 - e^{\frac{-tc}{Rt \times Ci}}\right) \tag{4}$$

and solving for the charge time, *tc*, leads to:

$$tc_{1/16LSB} = Rt \times Ci \times ln2^{N+4} \tag{5}$$

where *ln* is the natural logarithm

2.2 Evaluating the Number of Time Constants Using Equation (5)

Consider an 8-bit (N = 8) resolution converter with the total series resistance from equation (2). Equation (5) gives the time, in number of time constants, required to charge the equivalent ADC input capacitance to within 1/16 LSB, such that

$$\begin{aligned} tc_{1/16LSB} &= Rt \times Ci \times ln2^{8+4} \\ &= Rt \times Ci \times 8.32 \\ &= 8.32\ time\ constants \\ &= 8.32\ TC \end{aligned} \tag{6}$$

Where

$$TC = Rt \times Ci \tag{7}$$

Therefore, to charge the input to within 1/16 LSB at 8-bit resolution requires 8.32 time constants. Table 1 shows results of similar calculations for 10, 12, 14, 16, and higher bit conversions.

Table 1. Charge Time, tc, Required for 1/16 LSB Accuracy

RESOLUTION	CHARGE TIME, tc
8 bit	8.32 Time Constants
10 bit	9.70 Time Constants
12 bit	11.10 Time Constants
14 bot	12.48 Time Constants
16 bit	13.87 Time Constants

3 General Equation for a Given ADC Sampling Time (Ts)

The required input time constant must be small enough to be within the given ADC analog input sampling time (Ts) for the desired accuracy. In the case given in Section 4, 1/16 LSB was chosen to give an error of not more than 6.25%. The internal sampling time for the ADC must be equal to or greater than the required number of time constants, so the minimum sampling time for any desired accuracy is given by the general equation:

$$Ts(min) = Number\ of\ TC\ required\ for\ the\ desired\ accuracy \tag{8}$$

3.1 TLC549 8-Bit Example

Assume the TLC549 8-bit converter is operating at a 2-MHz I/O clock frequency. Referring to the timing diagram of Figure 2 (from the data sheet), the device has a 4-I/O-clock-period sample time called Sample Cycle B. On the eighth falling edge the analog input is held and a conversion cycle begins. Therefore, the total time the TLC549 allows for analog input sampling for a selected accuracy is:

$$Ts = Number\ of\ I/O\ clocks\ for\ sampling \times \frac{1}{I/O\ clock\ frequecny}$$
$$Ts = 4 \times \frac{1}{2\ MHz} = 4 \times 500\ ns = 2\ \mu s \tag{9}$$

Equating this analog sampling time in equation (9) to the total number of time constants required for the analog input capacitance to charge to within 1/16 LSB gives:

$$tc_{1/16LSB} = Ts = 2\ \mu s = 8.32\ (Rs + Ri) \times Ci$$

With Ci = 100 pF and ri = 1 kΩ and solving for Rs, then,

$$Rs = \frac{2\ \mu s}{8.32 \times 100\ pF} – ri$$
$$Rs = 2.4\ k\Omega – 1\ k\Omega = 1.4\ k\Omega$$

So the analog source resistance can be no larger than 1.40 kΩ for 1/16 LSB accuracy.

3.2 TLC2543 12-Bit Example

Now assume that the TLC2543 12-bit converter is running with a 4-MHz I/O clock rate and 12 I/O clock mode. From Figure 3 (from the data sheet) the sampling time for the analog input is called Sample Cycle B and is 8 I/O clocks long. On the falling edge of the 12th falling edge of the I/O clock sequence, the input is held and conversion begins. Therefore, the total time for analog input sampling is:

$$Ts = Number\ of\ I/O\ clocks \times \frac{1}{4\ MHz} = 8 \times 250\ ns = 2\ \mu s$$

Inserting this analog sampling time into equation (7) and equating to total number of time constants required for the TLC2543 converter to settle within 1/16 LSB gives:

$$tc_{1/16LSB} = 2\ \mu s = 1.11 \times (Rs + Ri) \times Ci$$

With Ci = 100 pF and Ri = 1 kΩ and solving for Rs, then

$$Rs = \frac{2\ \mu s}{1.11 \times 100\ pF} - ri$$

$$Rs = 1.8\ k\Omega - 1\ k\Omega = 800\ \Omega$$

So the input analog source resistance can be no larger than 800 ohms for 1/16 LSB accuracy for the TLC2543 analog input operating in the 12 I/O clock mode.

4 Summary

The calculations in this application report show that the maximum driving source resistance for a specific ADC varies with the sampling time and circuit parameters to the required accuracy according to:

$$Rs = \frac{Ts}{Ci \times Ln\ 2^{N+m}} - ri$$

With:

Rs = Driving source resistance
Ts = ADC specific sampling time
Ci = ADC equivalent input capacitance
ri = ADC equivlaent input resistance
N = ADC resolution in bits
m = equivalent number of additional resolution bits to achieve the accuracy of $\frac{1}{2^m}$ of an LSB