Interfacing the A/D Converters TLC5540/10 to the DSKplus DSP Starter Kit TMS320C54x

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1. Introduction

This Application Note describes the construction of a test circuit using the A/D converters TLC5540 and TLC5510, and alternative ways of interfacing these converters to the DSKplus DSP starter kit TMS320C54x. Details are given of the test circuit of the TLC5540/10 and of the interface, and the programming of the digital signal processor TMS320C54x is also described.

2. TLC5540/10 Test Circuit

The TLC5540/10 test circuit is intended for the development of laboratory prototypes with the 8-bit high-speed A/D converters TLC5540 and TLC5510 from Texas Instruments.

The maximum conversion rate of the TLC5540 is at least 40 MSPS (Mega Samples Per Second), and the typical analog input bandwidth is more than 75 MHz. The layout therefore plays a decisive role in determining performance, and construction in the laboratory using a breadboard is no longer a suitable approach. In addition, the use of surface-mounted components is necessary, if a proper evaluation of performance is to be made.

2.1 Supply Voltages

The TLC5540/10 test circuit must be provided with three separate supply voltages if the optimum performance is to be achieved. Details of these various supply voltages are given in Table 1 .

Voltage	Jumper	Application
+5 V	J2	Analog supply voltage, and positive supply of the input amplifier
-5 V	J3	Negative supply voltage of the input amplifier
+5 V	J8	Digital supply voltage

Table 1: Supply Voltages

There exists a common grounding area (0 V) for the analog +5-V and -5-V supply voltages. The grounding area for the digital supply voltage is isolated from the grounding area of the analog supply voltage, in order to prevent one influencing the other.

The two grounding areas can simply be connected together by making a connection from E21 to E22, or from E13 to E14. In this way, it is possible to create and evaluate various alternative grounding options.

The available connections can be seen in the circuit of the TLC5540/10 test circuit diagram, as shown in Figure 1.

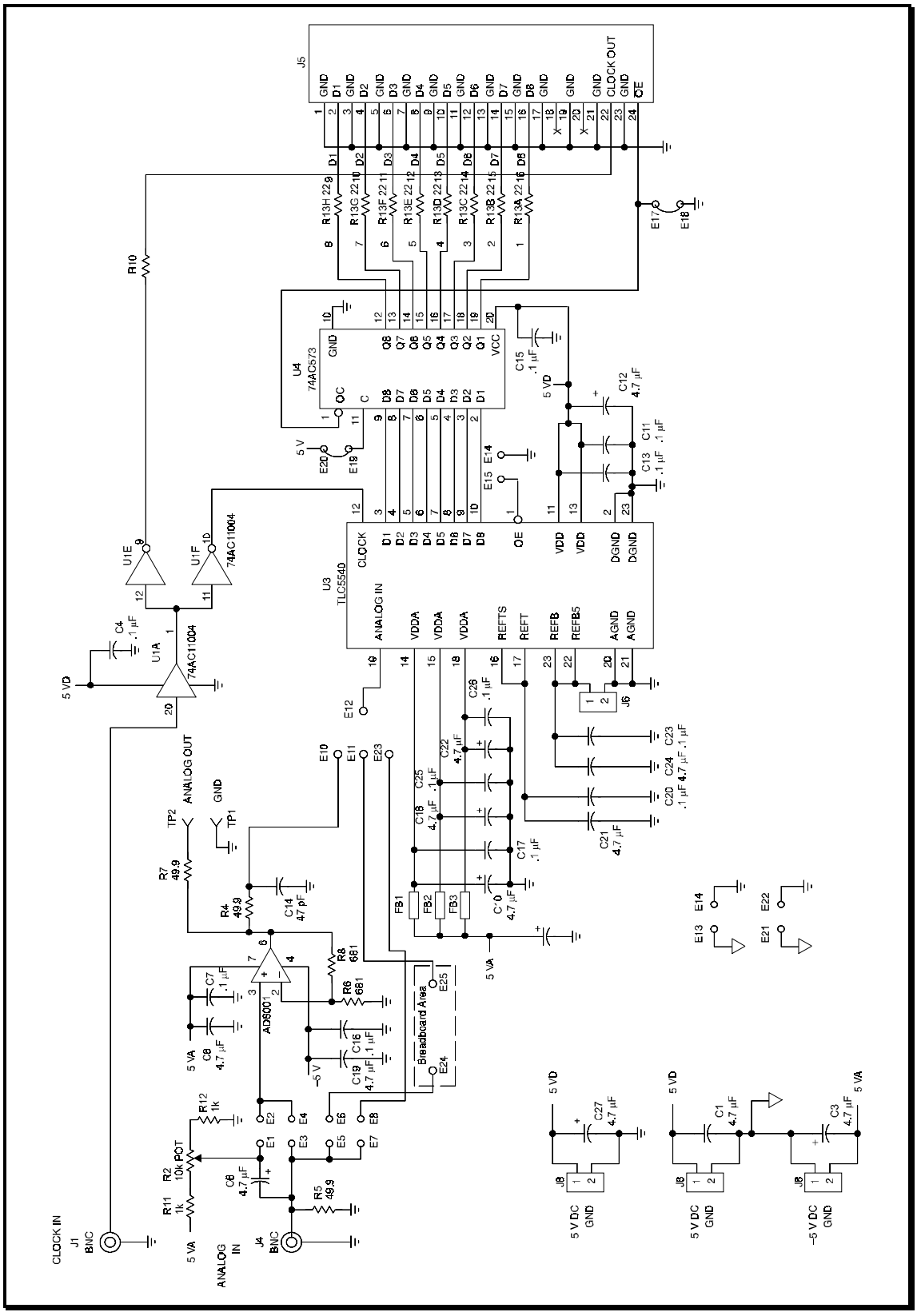

Figure 1: Circuit Diagram of the TLC5540/10 Test Circuit

2.2 Analog Input

The analog input signal is taken via the BNC connector J4. This signal is taken to the input of the TLC5540/10 via one of four alternative routes:

- directly;
- via the amplifier input (with DC coupling);
- via the amplifier input (with AC coupling); or
- with the input defined by the user.

2.2.1 Direct Input

The input signal can be taken directly to the TLC5540/10, by making use of the solder bridges from E7 to E8 and from E23 to E12. The reference voltage for the TLC5540/10 is generated in this circuit by means of the internal reference resistors. If the jumper J6 is inserted, the reference voltage will be 2.28 V with respect to 0 V; otherwise, it will be 2.6 V with respect to 0.6 V.

2.2.2 Amplifier Input (DC Coupling)

The operational amplifier AD8001 is situated in the input stage. It can be operated up to a frequency of 400 MHz with an amplification of +2, and is able to drive a low resistance load.

The amplification factor is set to a factor of +2 by means of the resistors R_6 and R_8. By removing R_6, the amplification will be set to a factor of +1. The AD8001 is a current feed-back (transimpedance) amplifier. With trans-impedance amplification, the operation is different from that of an operational amplifier with voltage feedback. The non-inverting input is at a high resistance; in the ideal case, the inverting input has an input resistance of 0 Ω. As a result of this, the resistor R_8 must be retained in the circuit and its value must be changed to 953 Ω.

An antialiasing low-pass filter has been implemented at the output of the operational amplifier by means of R_4 and C_{14}. Frequencies above 20 MHz (F_s/2) are filtered out in this way. The capacitance of the condenser C_{14} can be varied in order to achieve other filter characteristics.

The capacitive loading at the output of the operational amplifier is reduced by means of the resistor R_4 in series with the output. The resistor R_7 prevents capacitive loading at the test point TP2 by the probe of the oscilloscope becoming excessive, and thus any tendency for the operational amplifier to oscillate.

The output of the operational amplifier is connected to the analog input of the TLC5540/10 by a solder bridge from E10 to E12. The amplifier input can be DC or AC coupled to the input signal. Table 2 shows the connections needed for these options.

Coupling	Connection
DC	E3 to E4
AC	E1 to E2

Table 2: Coupling of the input signal

2.2.3 Amplifier Input (AC Coupling)

If AC coupling is desired, an offset voltage can be provided by means of the potentiometer R_2. The offset voltage can be adjusted from almost 0 V up to +5 V (analog). With an amplification factor of + 2, the positive dynamic drive limit of the operational amplifier will already be reached with an offset voltage of 2.5 V.

The cutoff frequency of the low-pass filter is determined by the 4.7-µF capacitor (C_6) and resistance value set by means of the potentiometer.

2.2.4 Input Range of the TLC5540/10

The permissible input voltage range of the TLC5540/10 depends on the jumper J6. Table 3 shows options for setting this.

Jumper J6	Input Voltage Range
Not inserted	0.6 V to 2.6 V
Inserted	0 V to 2.28 V

Table 3: Input Voltage Range of the A/D Converter

Other settings are also possible; the data sheet of the TLC5540/10 gives more information about this.

2.2.5 Test Points

The analog output voltage of the operational amplifier can be measured at the test points TP1 and TP2. The allocation of these test points can be seen in Table 4 below.

TP1	Analog Ground
TP2	Output of the operational amplifier

Table 4: Test points

2.2.6 Input Defined by the User

An optional circuit extension allows additional tests to be made. The analog input signal is taken to the circuit extension via a solder bridge from E5 to E6. The connection of the circuit extension to the input of the A/D converter is made with an additional solder bridge from E23 to E12.

2.3 Digital Data Output

The digital data of the A/D converter is buffered by an octal latch SN74AC573. A series resistor of 22 Ω per output is provided to reduce line reflections. The individual data outputs are taken to the connecting strip J5. The outputs of the SN74AC573 are switched into a high resistance state via the $\overline{OE}$ input. This allows a bus interface to an external circuit. The jumper between E17 and E18 must be removed, and the outputs of the SN74AC573 controlled by means of Pin 24 on the connecting strip ($\overline{OE}$). The outputs are then only active when the data of the A/D converter should be read.

2.4 Clock Circuit

The maximum clock frequency of the A/D converter TLC5540 (TLC5510) is 40 MHz (20 MHz). The clock signal is fed in via the BNC input J1. It is buffered by two inverters of the 74AC11004, and is applied to the clock input of the A/D converter and to Pin 22 of the connecting strip J5.

3. Timing Behavior of TLC5540/10

The analog input data of the TLC5540 and TLC5510 is sampled at the falling edge of the clock signal. The conversion time of the analog input signal amounts to 2.5 clock cycles. Figure 2 shows the timing behavior of the TLC5540/TLC5510.

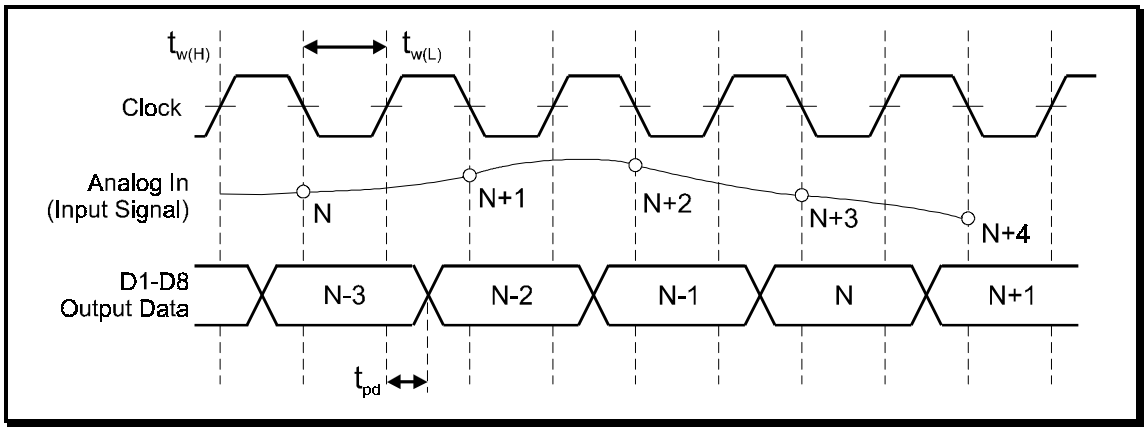

Figure 2: Timing Behavior of the TLC5540/TLC5510

The digital data is valid after a delay time t_{pd} = 15 ns for the TLC5540, or t_{dd} = 30 ns for the TLC5510. Several important parameters of the TLC5510 are summarized in Table 5, these applying under the following operating conditions: V_{DD} = 5 V, V_{RT} = 2.5 V, V_{RB} = 0.5 V, f_S = 20 MSPS, T_A = 25°C.

Parameter		MIN	NOM	MAX	UNIT
Pulse duration, clock high, $t_{W(H)}$		25			ns
Pulse duration, clock low, $t_{W(L)}$		25			ns
Parameter	**Test Conditions**				
f_{conv} Maximum conversion rate	$V_{I(ANLG)}$ = 0.5 V - 2.5 V	20			MSPS
BW Analog input bandwidth	At -1 dB		14		MHz
t_{dd} Delay time, digital output	$C_L \leq$ 10 pF		18	30	ns

Table 5: Parameters of the TLC5510

Several important parameters of the TLC5540 have been brought together in Table 6, and these apply under the following operating conditions: V_{DD} = 5 V, V_{RT} = 2.6 V, V_{RB} = 0.6 v, f_S = 40 MSPS, T_A = 25°C.

Parameter			MIN	NOM	MAX	UNIT
Pulse duration, clock high, $t_{W(H)}$			12.5			ns
Pulse duration, clock low, $t_{W(L)}$			12.5			ns
Parameter		**Test Conditions**				
f_S	Maximum conversion rate	TA = MIN to MAX	40			MSPS
f_S	Minimum conversion rate	TA = MIN to MAX		5		MSPS
BW	Analog input bandwidth	At -3 dB, $V_{I(ANLG)}$ = 2 V_{pp}		75		
t_{pd}	Delay time, digital output	$C_L \leq 10$ pF		9	15	

Table 6 Parameters of the TLC5540

4. Interface of DSK+ to TLC5540/10

The interface between the TMS320C54x DSK+ and the A/D converters TLC5540/10 will now be described. This Application Note shows two alternative solutions. In the first solution, the clock frequency CLKOUT of the DSK+ is used as the clock input for the A/D converter. This arrangement is shown in Figure 3. The second solution uses the programmable counter of the TMS320C54x as a source for the clock frequency.

4.1 Circuit Option 1

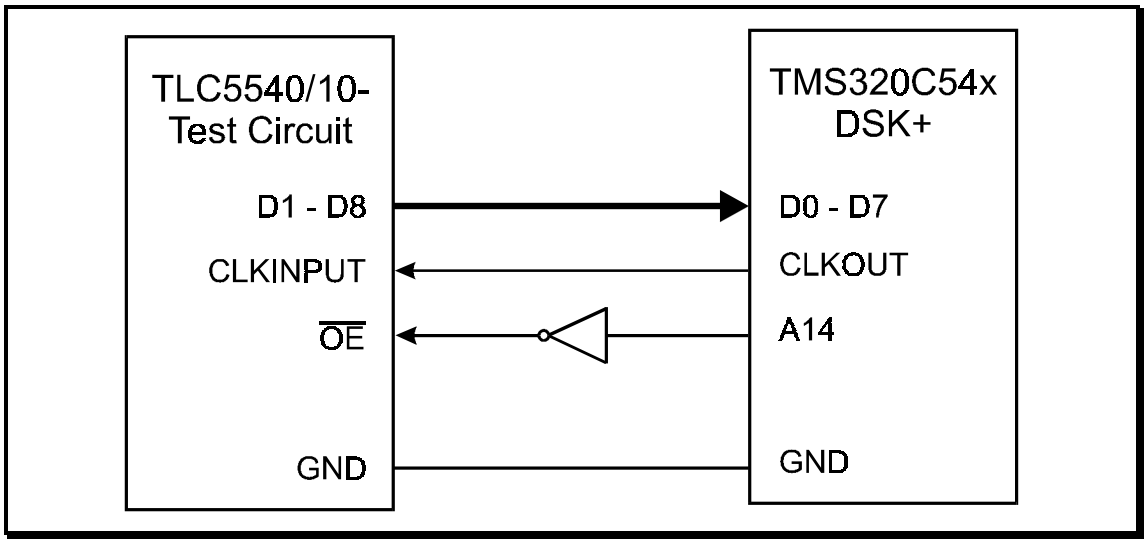

Figure 3: Interfacing the DSK+ to the TLC5540/10

The data bus D1 - D8 of the A/D converters TLC5540/10 is connected by means of the data bus driver SN74AC573 to the data bus D0 - D7 of the TLC320C54x DSK+. The SN74AC573 of the TLC5540/10 test circuit must only be in an active state when data should be read from the DSK+; otherwise a bus conflict between the two systems will arise. For this reason, the $\overline{OE}$ input of the data bus driver is used for control. A High level signal will be generated with the address line A14 (Address 4000_{16}) at every access of the DSK+, and this will be passed on inverted to the $\overline{OE}$ input and thus switch the data bus driver SN74AC573 into an active state. Should the address line A14 be used only for the TLC5540/10 test circuit, then no additional address decoder is necessary. The jumper J6 of the test circuit must be removed, so that the $\overline{OE}$ input is not continuously pulled to a Low level.

The data bus driver SN74AC573 need not be used if the DSP is connected directly to the A/D converter. In this case, the $\overline{OE}$ input of the TLC5540/10 will be used for control.

The necessary clock frequency for the A/D converter is generated by the DSK+. The CLKOUT signal is connected directly to the clock input of the test circuit. Because of the clock frequency of 40 MHz, this option can however only be used with the TLC5540.

The clock signal is buffered by means of the octal inverter 74AC11004, and taken both to the A/D converter and to the connecting strip J5 (Pin 22).

In order to equalize the potential of the two systems, their grounds must be connected together.

4.2 Programming Example 1

This program has been compiled with the algebraic assembler DSKplus (Version 1.00) from Texas Instruments.

```
*********************************************************
* (C) TEXAS INSTRUMENTS DEUTSCHLAND GMBH, 1997          *
* File: TLC5540.ASM                                     *
*********************************************************
          .mmregs
          .setsect ".text", 0x1800,0

          .text
START:    AR1 = #4000h   ;Addressing the A/D converter
          AR2 = #2400h   ;Pointer to memory for
                          converted values
          AR4 = #50h     ;Counter for number of samples
S_LOOP:   A = *AR1       ;A/D value to accumulator
          *AR2+ = A      ;Store the A/D value in memory
W_LOOP:   if (*AR4- != 0) goto S_LOOP ;have all values ?
END       goto END
```

In this example, the conversion is performed with oversampling. The clock cycle time of the TMS320C54x is 25 ns, and it is therefore not possible to read in each conversion value. In the programming example, 80 conversion values are read and stored in the internal DARAM from Address 2400_{16}.

These values can be displayed directly with the graphical display of the DSK+ “Code Explorer”.

4.3 Circuit Option 2

In the second solution, the clock frequency of the A/D converter is programmable. This is necessary for the TLC5510, which has a maximum clock frequency of 20 MHz, but it can also be used for the TLC5540. The interface is shown in Figure 4 .

The programmable counter of the TMS320C54x is used for clock generation. The clock frequency can be programmed as follows:

$$TOUT = \frac{1}{25ns \times (TDDR_{reg} + 1) \times (PRD_{reg} + 1)}$$

The setting of the desired clock frequency is performed by means of the programming of the registers $TDDR_{reg}$ and PRD_{reg} in the function ‘timerinit’.

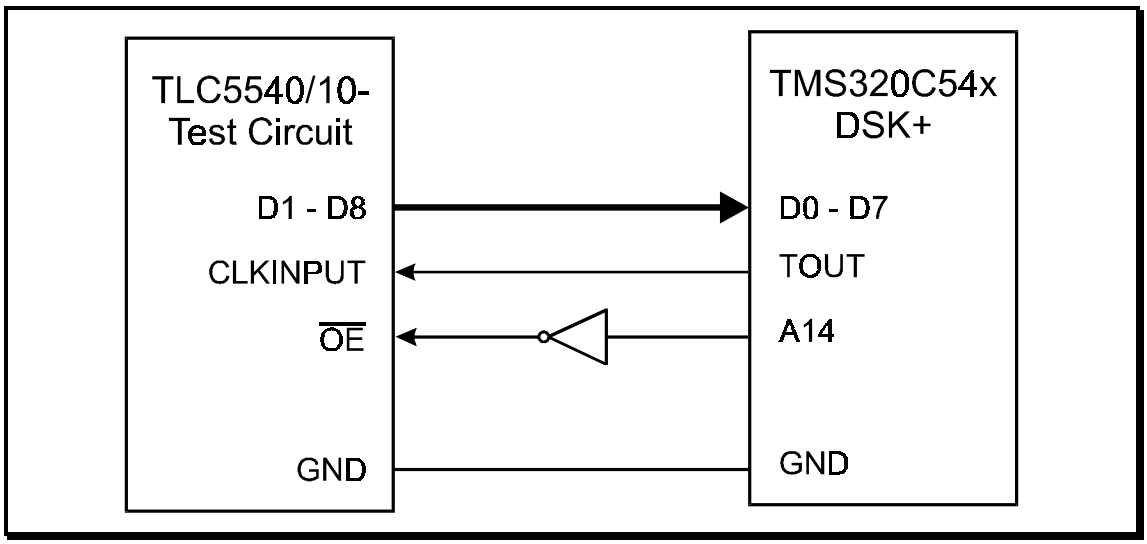

Figure 4: Interface of the DSK+ to the TLC5540/10

The maximum sampling frequency of the TLC5510 is 20 MHz. In the programming example shown, a sampling frequency of 20 MHz has been chosen, by setting the register PRD_{reg} to 1 and the register $TDDR_{reg}$ to 0. With a sampling frequency of 20 MHz oversampling occurs, as in the previous example, since with a clock cycle time of 25 ns it is not possible to read in every conversion value.

4.4 Programming Example 2

```
*********************************************************
* (C) TEXAS INSTRUMENTS DEUTSCHLAND GMBH, 1997          *
* File: TLC5540.ASM                                     *
* Interface 'C54x DSKplus to the TLC5540/10             *
*********************************************************

          .width   80
          .length  55
          .title "TLC5540EVM Interface"
          .mmregs
          .setsect ".text",   0x1800,0

          .text

START:     sp = #0ffah
           call timerinit
           AR1 = #4000h   ;Addressing the A/D converter
GO:        AR2 = #2400h   ;Pointer to memory for
                           converted values
           AR4 = #50h     ;Counter for number of samples
S_LOOP:    AR3 = #0h      ;Counter for W_LOOP
           A = *AR1       ;A/D value to accumulator
           *AR2+ = A      ;Store the A/D value in memory
; hereafter, the DSP can calculate functions, such as
; filters, etc.
W_LOOP:    if (*AR3- != 0) goto W_LOOP ;Wait for next
                                        value
           if (*AR4- != 0) goto S_LOOP ;have all values ?
END        goto END

.copy "path\timer.asm"

*********************************************************
*       (C) COPYRIGHT TEXAS INSTRUMENTS, INC. 1996      *
*********************************************************
*                                                       *
```

```
* File: TIMER.ASM  Timer initialization code for the   *
* 'C54x DSKplus                                        *
*                                                      *
********************************************************
         .width   80
         .length  55
         .title "Timer Initialization Routine"
********************************************************
PRDreg     .set  1h
TDDRreg    .set  0h

          .eval  TDDRreg | 20h, TDDRval
timerinit:
          prd = #PRDreg                ;set Timer
                                        Period Register
          tcr = #TDDRval               ;set Timer
                                        Control Register
                                        and start timer
          return
```

Compared with the first Programming Example, in this Example a Wait Loop (W_LOOP) has been included. The wait loop is used in order to match the time of a read cycle to that of the programmed sampling frequency. For this to happen, the MMR (Memory Mapped Register) AR3 is loaded with an appropriate value. This matching is however necessary only if the sampling frequency is faster than the read time. In this way, the repeated reading out of the same conversion result can be avoided.

As already shown in the previous programming example, 80 conversion values are read and stored in the internal DARAM from address 2400_{16}. These values can be directly displayed with the graphical display of the DSK+ “Code Explorer”.

5. References

Texas Instruments, Data Book: Data Acquisition Circuits SLAD001
Texas Instruments, Data Sheet: TLC5540 SLAS105B
Texas Instruments, Data Sheet:TLC5510 SLAS095G
Texas Instruments, Data Sheet: 74AC11004 SCAS033B
Texas Instruments, Data Sheet: SN74HCT245 SCLS177B
Texas Instruments, Data Sheet: TMS320C54x SPRS039
Texas Instruments, TMS320C54x CPU and Peripherals SPRU131C
Texas Instruments, TMS320C54x Algebraic Instruction Set SPRU179
Texas Instruments TMS320C54x DSKplus User's Guide SPRU191