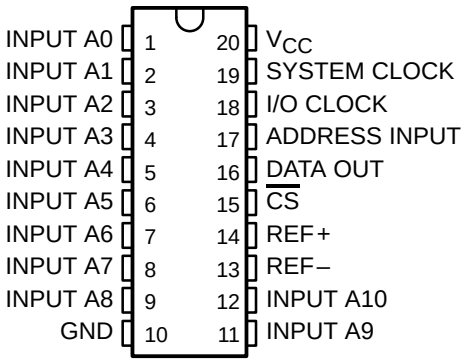
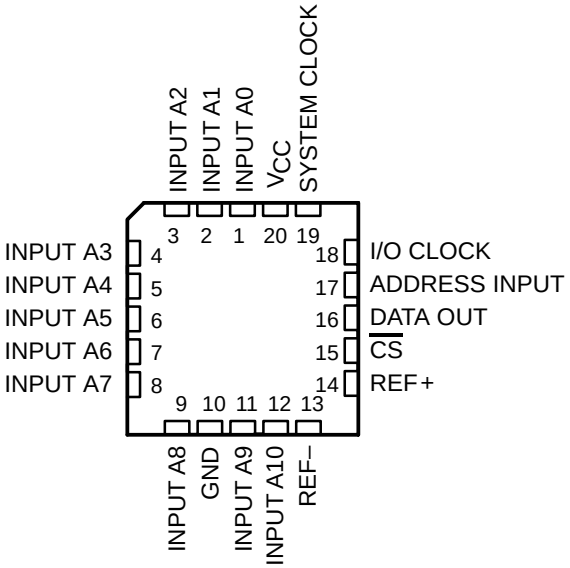
- **LinCMOS™ Technology**
- **8-Bit Resolution A/D Converter**
- **Microprocessor Peripheral or Stand-Alone Operation**
- **On-Chip 12-Channel Analog Multiplexer**
- **Built-in Self-Test Mode**
- **Software-Controllable Sample and Hold**
- **Total Unadjusted Error . . . ±0.5 LSB Max**
- **TLC541 is Direct Replacement for Motorola**
  - **MC145040 and National Semiconductor**
  - **ADC0811. TLC540 is Capable of Higher Speed**
- **Pinout and Control Signals Compatible with TLC1540 Family of 10-Bit A/D Converters**

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



TYPICAL PERFORMANCE	TLC540	TLC541
Channel Acquisition Sample Time	2 µs	3.6 µs
Conversion Time	9 µs	17 µs
Samples per Second	75 x 10^3	40 x 10^3
Power Dissipation	6 mW	6 mW

description

The TLC540 and TLC541 are LinCMOS™ A/D peripherals built around an 8-bit switched-capacitor successive-approximation A/D converter. They are designed for serial interface to a microprocessor or peripheral via a 3-state output with up to four control inputs, including independent SYSTEM CLOCK, I/O CLOCK, Chip Select ($\overline{CS}$), and ADDRESS INPUT. A 4-MHz system clock for the TLC540 and a 2.1-MHz system clock for the TLC541 with a design that includes simultaneous read/write operation allow high-speed data transfers and sample rates of up to 75,180 samples per second for the TLC540 and 40,000 samples per second for the TLC541. In addition to the high-speed converter and versatile control logic, there is an on-chip 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal self-test voltage, and a sample-and-hold that can operate automatically or under microprocessor control. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The converters incorporated in the TLC540 and TLC541 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A switched-capacitor design allows low-error (±0.5 LSB) conversion in 9 µs for the TLC540 and 17 µs for the TLC541 over the full operating temperature range.

The I-suffix versions are characterized for operation from –40°C to 85°C. The M-suffix versions are characterized for operation from –55°C to 125°C.

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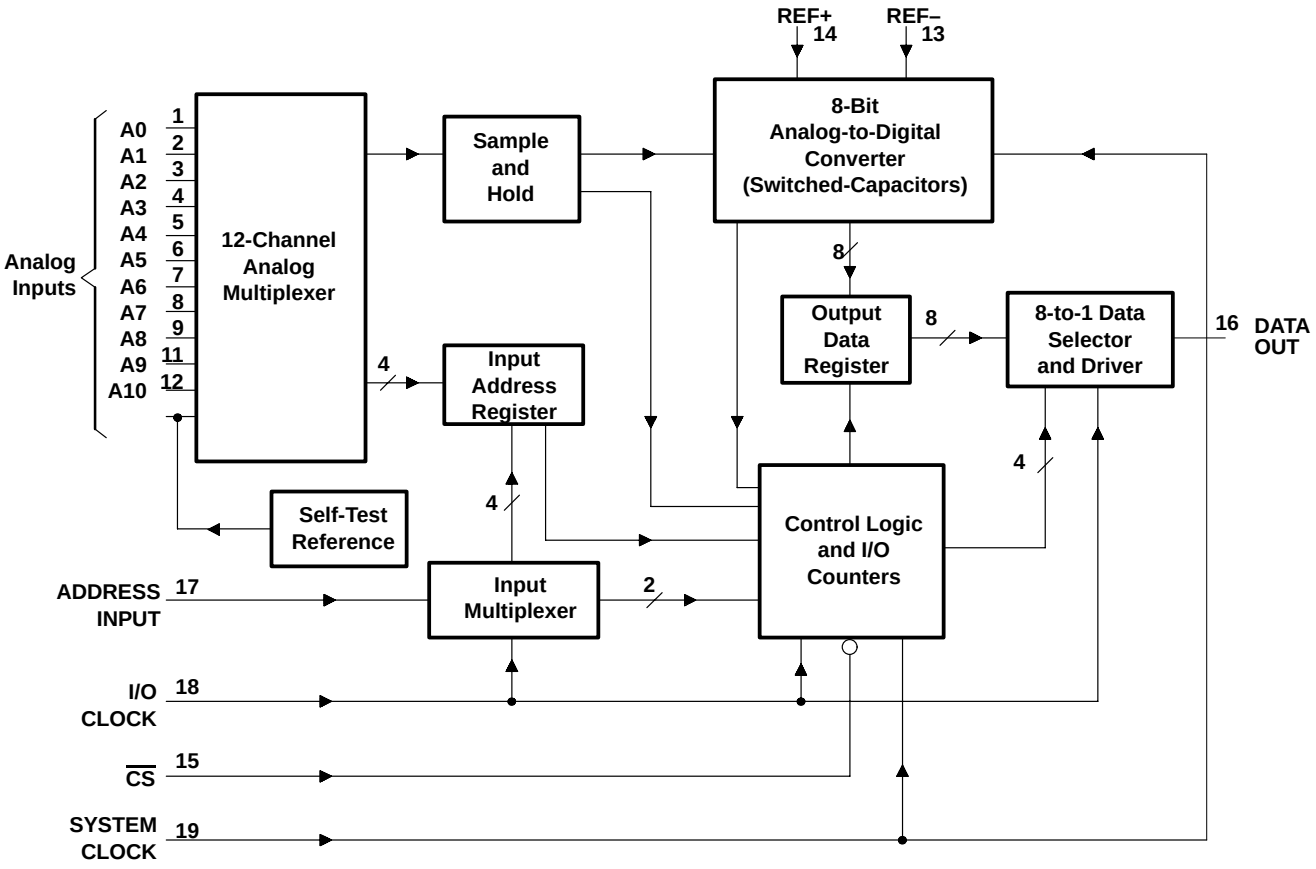
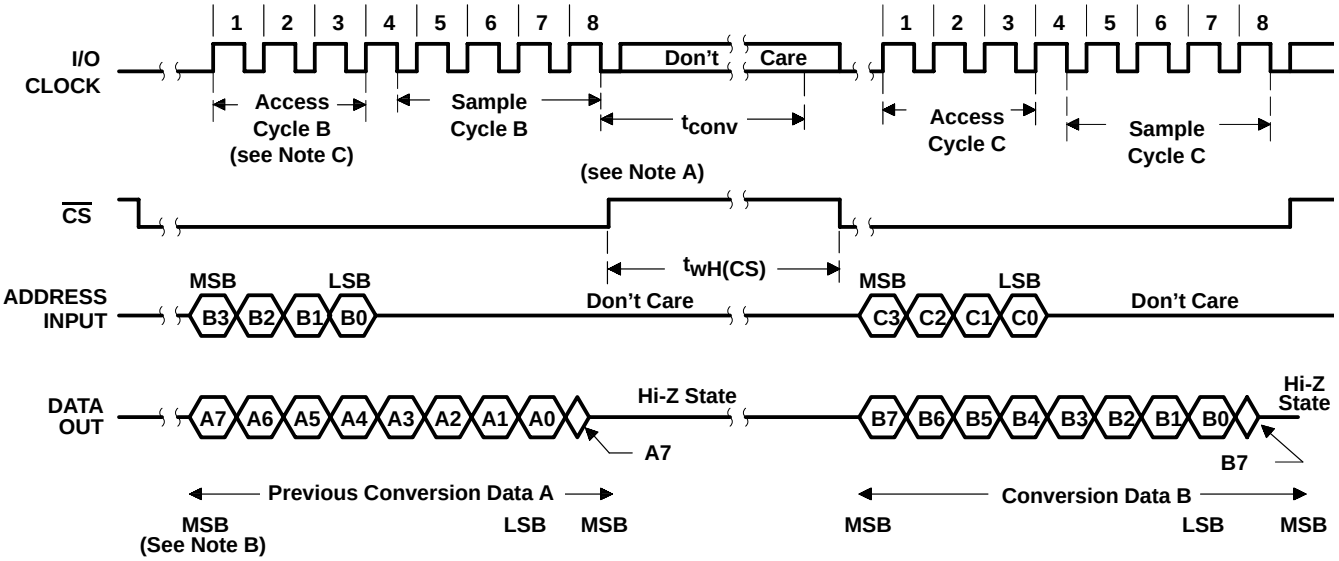
functional block diagram



operating sequence



NOTES: A. The conversion cycle, which requires 36 SYSTEM CLOCK periods, is initiated on the 8th falling edge of I/O CLOCK after $\overline{CS}$ goes low for the channel whose address exists in memory at that time. If $\overline{CS}$ is kept low during conversion, I/O CLOCK must remain low for at least 36 SYSTEM CLOCK cycles to allow conversion to be completed.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6–A0) will be clocked out on the first seven I/O CLOCK falling edges.

C. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for three SYSTEM CLOCK cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

absolute maximum ratings over operating free–air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	6.5 V
Input voltage range (any input)	–0.3 V to V_{CC} +0.3 V
Output voltage range	–0.3 V to V_{CC} +0.3 V
Peak input current range (any input)	±10 mA
Peak total input current (all inputs	±30 mA
Operating free-air temperature range: TLC540I, TLC541I	–40°C to 85°C
TLC540M, TLC541M	–55°C to 125°C
Storage temperature range	–65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package	260°C

NOTE 1: All voltage values are with respect to digital ground with REF– and GND wired together (unless otherwise noted).

recommended operating conditions

			TLC540			TLC541			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 2)			2.5	V_{CC}	$V_{CC}+0.1$	2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{REF-} (see Note 2)			−0.1	0	2.5	−0.1	0	2.5	V
Differential reference voltage, $V_{REF+} - V_{REF-}$ (see Note 2)			1	V_{CC}	$V_{CC}+0.2$	1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)			0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH}			2			2			V
Low-level control input voltage, V_{IL}					0.8			0.8	V
Setup time, address bits at data input before I/O CLOCK↑, $t_{su(A)}$			200			400			ns
Hold time, address bits after I/O CLOCK↑ $t_{h(A)}$			0			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit $t_{su(CS)}$ (see Note 3)			3			3			System clock cycles
$\overline{CS}$ high during conversion, $t_{wH(CS)}$			36			36			System clock cycles
Input/output clock frequency, $f_{clock(I/O)}$			0		2.048	0		1.1	MHz
System clock frequency, $f_{clock(SYS)}$			$f_{clock(I/O)}$		4	$f_{clock(I/O)}$		2.1	MHz
System clock high, $t_{wH(SYS)}$			110			210			MHz
System clock low, $t_{wL(SYS)}$			100			190			MHz
Input/output clock high, $t_{wH(I/O)}$			200			404			ns
Input/output clock low, $t_{wL(I/O)}$			200			404			ns
Clock transition time (see Note 4)	System	$f_{clock(SYS)} \le 1048$ kHz			30			30	ns
		$f_{clock(SYS)} > 1048$ kHz			20			20	
	I/O	$f_{clock(I/O)} \le 525$ kHz			100			100	
		$f_{clock(I/O)} > 525$ kHz			40			40	
Operating free-air temperature, T_A		TLC540I, TLC541I	−40		85	−40		85	°C
		TLC540M, TLC541M	−55		125	−40		125	

NOTES: 2. Analog input voltages greater than that applied to REF + convert as all “1”s (11111111), while input voltages less than that applied to REF– convert as all “0” s (00000000). For proper operation, REF + voltage must be at least 1 V higher than REF–voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

3. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for three SYSTEM CLOCK cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum chip select setup time has elapsed.
4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating temperature range, $V_{CC} = V_{REF+}$ = 4.75 V to 5.5 V (unless otherwise noted), $f_{clock(I/O)}$ = 2.048 MHz for TLC540 or $f_{clock(I/O)}$ = 1.1 MHz for TLC541

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage, DATA OUT		V_{CC} = 4.75 V I_{OH} = 360 µA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V I_{OL} = 1.6 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		$V_O = V_{CC}$, $\overline{CS}$ at V_{CC}			10	µA
			V_O = 0, $\overline{CS}$ at V_{CC}			–10	µA
I_{IH}	High-level input current		$V_I = V_{CC}$		0.005	2.5	µA
I_{IL}	Low-level input current		V_I = 0		–0.005	–2.5	µA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V		1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V		0.4	1	µA
			Selected channel at 0 V, Unselected channel at V_{CC}		–0.4	–1	µA
$I_{CC} + I_{ref}$	Supply and reference current		$V_{REF+} = V_{CC}$, $\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs			7	55	pF
		Control inputs			5	15	pF

† All typical values are at T_A = 25°C.

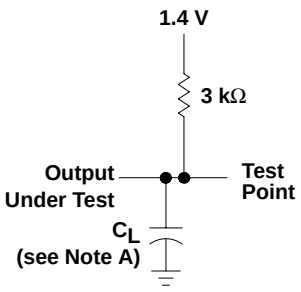
operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{REF+} - 4.75$ V to 5.5 V, $f_{clock(I/O)} = 2.048$ MHz for TLC540 or 1.1 MHz for TLC541, $f_{clock(SYS)} = 4$ MHz for TLC540 or 2.1 MHz for TLC541

PARAMETER		TEST CONDITIONS	TLC540			TLC541			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Linearity error	See Note 5			±0.5			±0.5	LSB
	Zero error	See Notes 2 and 6			±0.5			±0.5	LSB
	Full-scale error	See Notes 2 and 6			±0.5			±0.5	LSB
	Total unadjusted error	See Note 7			±0.5			±0.5	LSB
	Self-test output code	Input A11 address = 1011 (see Note 8)	01111101 (125)		10000011 (131)	01111101 (125)		10000011 (131)	
t_{conv}	Conversion time	See Operating Sequence			9			17	µs
	Total access and conversion time	See Operating Sequence			13.3			25	µs
t_a	Channel acquisition time (sample cycle)	See Operating Sequence			4			4	I/O clock cylces
t_v	Time output data remains valid after I/O CLOCK↓		10			10			ns
t_d	Delay time, I/O CLOCK↓ to data output valid	See Parameter Measurement Information			300			400	ns
t_{en}	Output enable time				150			150	ns
t_{dis}	Output disable time				150			150	ns
$t_{r(bus)}$	Data bus rise time				300			300	ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

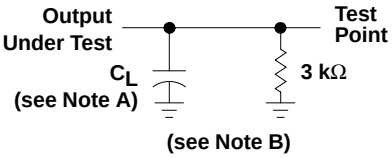
NOTES: 2. Analog input voltages greater than that applied to REF+ convert to all ”1”s (11111111) while input voltages less than that applied to REF– convert to all ”0” s (00000000). For proper operation, REF+ voltage must be at least 1 V higher than REF–voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
7. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic.

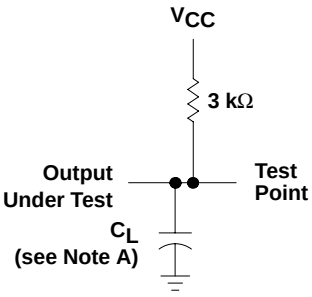
PARAMETER MEASUREMENT INFORMATION



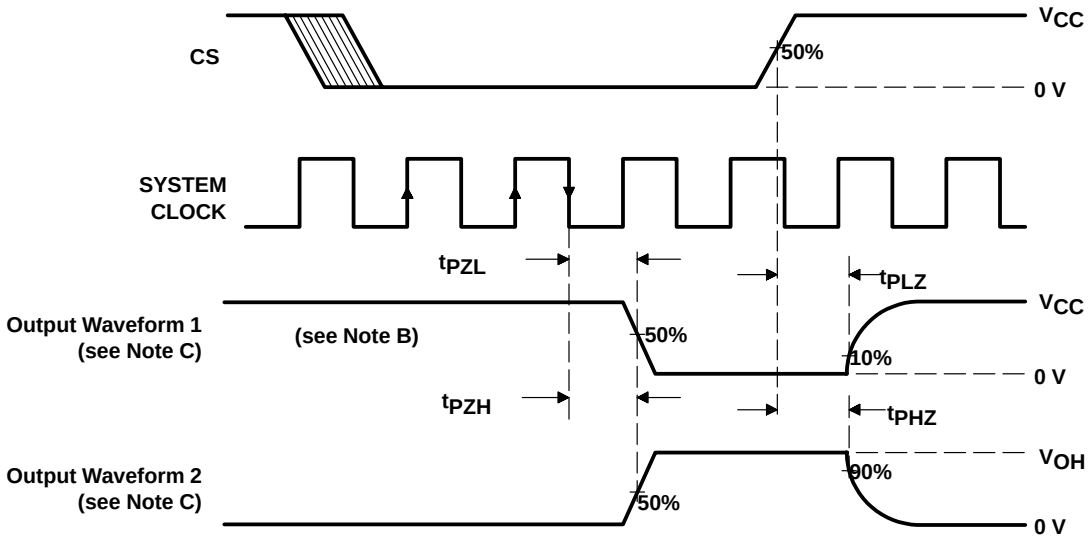
LOAD CIRCUIT FOR t_d, t_r, AND t_f



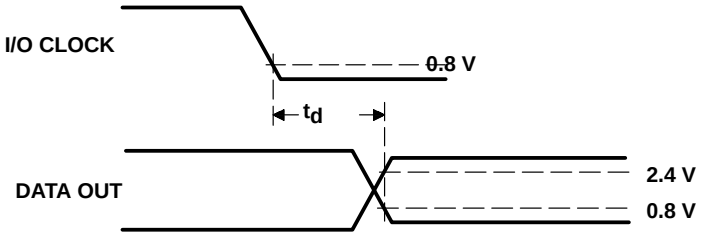
LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}



LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS FOR DELAY TIME

VOLTAGE WAVEFORMS FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC540 and 100 pF for TLC541.
B. $t_{en} = t_{PZH}$ or t_{PZL}, $t_{dis} = t_{PHZ}$ or t_{PLZ}.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

principles of operation

The TLC540 and TLC541 are each complete data acquisition systems on a single chip. They include such functions as analog multiplexer, sample and hold, 8-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs [two clocks, chip select ($\overline{CS}$), and address]. These control inputs and a TTL-compatible 3-state output are intended for serial communications with a microprocessor or microcomputer. With judicious interface timing, with TLC540 a conversion can be completed in 9 μs, while complete input-conversion-output cycles can be repeated every 13 μs. With TLC541 a conversion can be completed in 17 μs, while complete input-conversion-output cycles are repeated every 25 μs. Furthermore, this fast conversion can be executed on any of 11 inputs or its built-in “self-test” and in any order desired by the controlling processor.

The system and I/O Clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to SYSTEM CLOCK, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using I/O CLOCK. SYSTEM CLOCK will drive the “conversion crunching” circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, DATA OUT is in a 3-state condition and ADDRESS INPUT and I/O CLOCK are disabled. This feature allows each of these pins, with the exception of $\overline{CS}$, to share a control logic point with their counterpart pins on additional A/D devices when additional TLC540/541 devices are used. In this way, the above feature serves to minimize the required control logic pins when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for two rising edges and then a falling edge of SYSTEM CLOCK after a low $\overline{CS}$ transition, before the low transition is recognized. This technique is used to protect the device against noise when the device is used in a noisy environment. The MSB of the previous conversion result will automatically appear on DATA OUT.
2. A new positive-logic multiplexer address is shifted in on the first four rising edges of I/O CLOCK. The MSB of the address is shifted in first. The negative edges of these four I/O clock pulses shift out the second, third, fourth, and fifth most significant bits of the previous conversion result. The on-chip sample and hold begins sampling the newly addressed analog input after the fourth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Three clock cycles are then applied to I/O CLOCK and the sixth, seventh, and eighth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final eighth clock cycle is applied to I/O CLOCK. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 36 SYSTEM CLOCK cycles. After this final I/O Clock cycle, $\overline{CS}$ must go high or the I/O CLOCK must remain low for at least 36 System Clock cycles to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on I/O CLOCK. If glitches occur on I/O CLOCK, the I/O sequence between the microprocessor/controller and the device will lose synchronization. Also, if $\overline{CS}$ is taken high, it must remain high until the end of the conversion. Otherwise, a valid falling edge of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 system clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

principles of operation (continued)

It is possible to connect the System and I/O Clock pins together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

1. When $\overline{CS}$ is recognized by the device to be at a low level, the common clock signal is used as an I/O Clock. When $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used to drive the ”conversion crunching” circuitry.
2. The device will recognize a $\overline{CS}$ low transition only when the $\overline{CS}$ input changes and subsequently the System Clock pin receives two positive edges and then a negative edge. For this reason, after a $\overline{CS}$ negative edge, the first two clock cycles will not shift in the address because a low $\overline{CS}$ must be recognized before the I/O Clock can shift in an analog channel address. Also, upon shifting in the address, $\overline{CS}$ must be raised after the sixth I/O Clock pulse that has been recognized by the device, so that a $\overline{CS}$ low level will be recognized upon the lowering of the eighth I/O Clock signal that is recognized by the device. Otherwise, additional common clock cycles will be recognized as I/O Clock pulses and will shift in an erroneous address.

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device will accommodate these applications. Although the on-chip sample and hold begins sampling upon the negative edge of the fourth I/O Clock cycle, the hold function is not initiated until the negative edge of the eighth I/O Clock cycle. Thus, the control circuitry can leave the I/O Clock signal in its high state during the eighth I/O Clock cycle until the moment at which the analog signal must be converted. The TLC540/TLC541 will continue sampling the analog input until the eighth falling edge of the I/O Clock. The control circuitry or software will then immediately lower the I/O Clock signal and hold the analog signal at the desired point in time and start conversion.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.

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