TLC320AD55C
Data Manual

Sigma-Delta Analog Interface Circuit

SLAS085
July 1995

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Contents

Contents (Continued)

List of Illustrations

List of Tables

1 Introduction

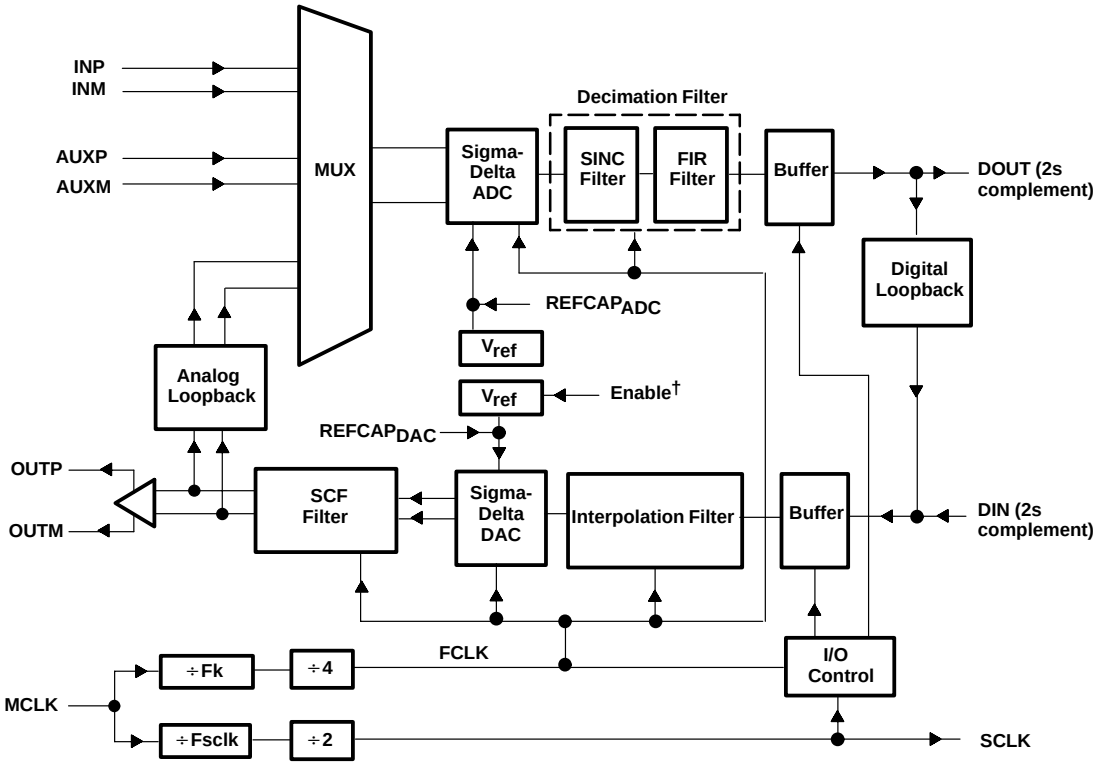
The TLC320AD55C provides high resolution low-speed signal conversion from digital-to-analog (D/A) and from analog-to-digital (A/D) using oversampling sigma-delta technology. This device consists of two, serial, synchronous conversion paths (one for each data direction) and includes an interpolation filter before the digital-to-analog converter (DAC) and a decimation filter after the analog-to-digital converter (ADC) (see Figure 1–1). Other overhead functions provide analog filtering and on-chip timing and control. The sigma-delta architecture produces high resolution, analog-to-digital and digital-to-analog conversion at low system speeds and low cost.

The options and the circuit configurations of this device can be programmed through the serial interface. The options include reset, power-down, communications protocol, serial clock rate, signal sampling rate, and test mode as outlined in Appendix A. The circuit configurations could include a selection of input ports to the ADC, analog loopback, digital loopback, decimator sinc filter output, decimator finite-duration impulse-response (FIR) filter output, interpolator sinc filter output, and interpolator FIR filter output. The TLC320AD55C is characterized for operation from 0°C to 70°C.

1.1 Features

- Single 5-V power supply
- Power dissipation (P_D) of 150 mW maximum in the operating mode
- Power-down mode to 1 mW
- General-purpose 16-bit signal processing
- 2s-complement format
- Serial port interface
- Minimum 80-dB harmonic distortion plus noise
- Differential architecture
- Internal reference voltage (V_{ref})
- Internal 64 $\times$ oversampling
- Analog output with programmable gain of 1, 1/2, 1/4, and 0 (squelch)
- Phone-mode output control
- Variable conversion rate selected as MCLK/(Fk $\times$ 256), Fk = 1,2,3,...,256
- System test mode:
  - Digital loopback test
  - Analog loopback test

1.2 Functional Block Diagram

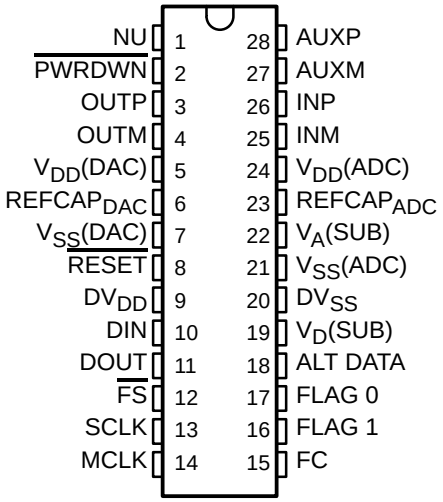


† See control 3 register in Appendix A.

Figure 1–1. Functional Block Diagram

1.3 Terminal Assignments

DW PACKAGE
(TOP VIEW)



NU – Make no external connection

Figure 1–2. Terminal Assignments

1.4 Ordering Information

T_A	PACKAGE
	SMALL OUTLINE (DW)
0°C to 70°C	TLC320AD55CDW

1.5 Terminal Functions

TERMINALS NAME	NO.	I/O	DESCRIPTION
AUXM	27	I	Inverting input to auxiliary analog input
AUXP	28	I	Noninverting input to auxiliary analog input
ALT DATA	18	I	Signals on ALT DATA are routed to DOUT during secondary communiction when phone mode is enabled.
DIN	10	I	Data input. DIN receives the DAC input data and command information from the DSP and is synchronized to SCLK.
DOUT	11	O	Data output. DOUT transmits the ADC output bits and is synchronized to SCLK. DOUT is at Hi-Z when $\overline{FS}$ is not activated.
DV_{DD}	9	I	Digital power supply
DV_{SS}	20	I	Digital ground
FC	15	I	Function control. FC is sampled and latched on the rising edge of $\overline{FS}$ for the primary serial communication. Refer to Section 3 Serial Communications for more details.
FLAG 0	17	O	During phone mode, FLAG 0 contains the value set in control 2 register.
FLAG 1	16	O	During phone mode, FLAG 1 contains the value set in control 2 register.
$\overline{FS}$	12	O	Frame sync. When $\overline{FS}$ goes low, the serial communication port is activated. In all serial transmission modes, $\overline{FS}$ is held low during bit transmission. Refer to Section 3 Serial Communications for a detailed description.
INM	25	I	Inverting input to analog input
INP	26	I	Noninverting input to analog input
MCLK	14	I	Master clock. MCLK derives the internal clocks of the sigma-delta analog interface circuit.
OUTM	4	O	Inverting output of the DAC analog power amplifier. Functionally identical with and complementary to OUTP. OUTM and OUTP can drive 600 Ω differentially. OUTM should not be used alone for single-ended operation.
OUTP	3	O	Noninverting output of the DAC analog power amplifier. OUTM and OUTP can drive 600 Ω differentially. OUTP should not be used alone for single-ended operation.
$\overline{PWRDWN}$	2	I	Power down. When $\overline{PWRDWN}$ is pulled low, the device goes into a power-down mode; the serial interface is disabled and most of the high-speed clocks are disabled. However, all of the registers' values are sustained and the device resumes full power operation without reinitialization when $\overline{PWRDWN}$ is pulled high again. $\overline{PWRDWN}$ resets the counters only and preserves the programmed register contents. Refer to Section 2.2.1.3 Software and Hardware Power-Down.
$REFCAP_{ADC}$	23	O	Analog-reference voltage connection for external capacitor for the ADC. The nominal voltage on $REFCAP_{ADC}$ is 3.4 V. A buffer must be used when this voltage is used externally. $REFCAP_{ADC}$ is not to be used as the mid-supply voltage reference for single-ended operation.
$REFCAP_{DAC}$	6	O	Analog-reference voltage connection for external capacitor for the DAC. The nominal voltage on $REFCAP_{DAC}$ is 3.4 V. A buffer must be used when this voltage is used externally.
$\overline{RESET}$	8	I	Reset. The reset function initializes all of the internal registers to their default values. The serial port can be configured to the default state accordingly. Refer to Appendix A Table A–2 Control 1 Register and Section 2.2.1 Reset and Power-Down for more detailed descriptions.
SCLK	13	O	Shift clock. SCLK is derived from MCLK and clocks serial data into DIN and out of DOUT.

NOTE 1: All digital inputs and outputs are TTL compatible unless otherwise noted.

1.5 Terminal Functions (Continued)

TERMINALS NAME	NO.	I/O	DESCRIPTION
V_A(SUB)	22	I	Analog substrate. V_A(SUB) must be grounded.
V_D(SUB)	19	I	Digital substrate. V_D(SUB) must be grounded.
V_{DD}(ADC)	24	I	Analog ADC path supply
V_{DD}(DAC)	5	I	Analog DAC path supply
V_{SS}(ADC)	21	I	Analog ADC path ground
V_{SS}(DAC)	7	I	Analog DAC path ground

NOTE 1: All digital inputs and outputs are TTL compatible unless otherwise noted.

1.6 Definitions and Terminology

Data Transfer Interval The time during which data is transferred from DOUT and to DIN. The interval is 16 shift clocks and this data transfer is initiated by the falling edge of the frame-sync signal.

Signal Data The input signal and all of the converted representations through the ADC channel and return through the DAC channel to the analog output. This is contrasted with the purely digital software control data.

Primary Communications The digital data transfer interval. Since the device is synchronous, the signal data words from the ADC channel and to the DAC channel occur simultaneously.

Secondary Communications The digital control and configuration data transfer interval into DIN and the register read data cycle from DOUT. The data transfer interval occurs when requested by hardware or software.

Frame Sync The falling edge of the signal that initiates the data transfer interval. The primary frame sync starts the primary communications, and the secondary frame sync starts the secondary communications.

Frame Sync and Sampling Period The time between falling edges of successive primary frame-sync signals.

f_s The sampling frequency that is the reciprocal of the sampling period.

Frame-Sync Interval The time period occupied by 16 shift clocks. It goes high on the sixteenth rising edge of SCLK after the falling edge of the frame sync.

ADC Channel All signal processing circuits between the analog input and the digital conversion results at DOUT.

DAC Channel All signal processing circuits between the digital data word applied to DIN and the differential output analog signal available at OUTP and OUTM.

Host Any processing system that interfaces to DIN, DOUT, SCLK, or $\overline{FS}$.

Dxx A bit position in the primary data word (xx is the bit number).

DSxx A bit position in the secondary data word (xx is the bit number).

d The alpha character d is used to represent valid programmed or default data in the control register format (see secondary serial communications) when discussing other data bit portions of the register.

X The alpha character X represents a don't-care bit position within the control register format.

FIR Finite-duration impulse response.

1.7 Register Functional Summary

There are six data and control registers that are used as follows:

Register 0 The No-op register. The 0 register allows secondary requests without altering any other register.

Register 1 The control 1 register. The data in this register controls:

- The software reset
- The software power-down
- Selection of the normal or auxiliary analog inputs
- The output amplifier gain (1, 1/2, 1/4, or squelch)
- Selection of the analog loopback
- Selection of the digital loopback
- 16-bit or 15-bit mode of operation

Register 2 The control 2 register. The data in this register:

- Contains the output flag indicating a decimator FIR filter overflow
- Contains Flag 0 and Flag 1 output values for use in the phone mode
- Selects the phone mode
- Selects or bypasses the decimation FIR filter
- Selects or bypasses the interpolater FIR filter

Register 3 The Fk divide register. This register controls the filter clock rate and the sample period.

Register 4 The Fsclk divide register. This register controls the shift (data) clock rate.

Register 5 The control 3 register. This register enables and disables the DAC reference.

2 Functional Description

2.1 Device Functions

The following sections describe the functions of the device.

2.1.1 Operating Frequencies

The sampling (conversion) frequency is derived from the master clock (MCLK) input by the following equation:

$$f_S = \text{Sampling (conversion) frequency} = \frac{\text{MCLK frequency}}{(\text{Fk register value}) \times 256}$$

The inverse is the time between the falling edges of two successive primary frame-synchronization signals and it is the conversion period.

The input and output data clock (SCLK) is given by:

$$\text{SCLK frequency} = \frac{\text{MCLK frequency}}{(\text{Fsclk register value}) \times 2}$$

2.1.2 ADC Signal Channel

To produce excellent common-mode rejection of unwanted signals, the analog signal is processed differentially until it is converted to digital data.

The ADC converts the signal into discrete output digital words in 2s-complement format, corresponding to the analog-signal value at the sampling time. These 16-bit digital words, representing sampled values of the analog input signal, are clocked out of the serial port, DOUT, during the frame-sync interval (one word for each primary communication interval). During secondary communications, the data previously programmed into the registers can be read out with the appropriate register address, and the read bit set to 1. When a register read is not requested, all 16 bits are 0 in the secondary word.

2.1.3 DAC Signal Channel

DIN receives the 16-bit serial data word (2s complement) from the host during the primary communications interval and latches the data on the seventeenth rising edge of SCLK. The data are converted to an analog voltage by the DAC and then passed through a (sin x)/x correction circuit and a smoothing filter. An output buffer with three software-programmable gains (0 dB, –6 dB, and –12 dB) drives the differential outputs OUTP and OUTM. A squelch mode can also be programmed for the output buffer. During secondary communications, the configuration program data are read into the device control registers.

2.1.4 Serial Interface

The digital serial interface consists of the shift clock, the frame synchronization signal, the ADC-channel data output, and the DAC-channel data input. During the primary 16-bit frame synchronization interval, SCLK transfers the ADC channel results from DOUT and transfers 16-bit DAC data into DIN.

During the secondary frame-synchronization interval, the SCLK transfers the register read data from DOUT when the read bit is set to a one. In addition, SCLK transfers control and device parameter information into DIN. The functional sequence is shown in Figure 3–1.

2.1.5 Register Programming

All register programming occurs during secondary communications, and data are latched and valid on the rising edge of the frame-sync signal. When the default value for a particular register is desired, that register does not need to be addressed during secondary communications. The no-op command addresses the no-op register (register 0), and register programming does not take place during this communication.

DOUT is released from the high-impedance state on the falling edge of the primary or secondary frame-sync interval. In addition, each register can be read back during DOUT secondary communications by setting the read bit D13 to 1 in the addressed register (refer to Appendix A). When the register is in the read mode, no data can be written to the register during this cycle. To return this register to the write mode requires a subsequent secondary communication.

2.1.6 Sigma-Delta ADC

The sigma-delta ADC is a fourth-order, sigma-delta modulator with 64-times oversampling. The ADC provides high-resolution, low-noise performance using oversampling techniques.

2.1.7 Decimation Filter

The decimation filter reduces the digital data rate to the sampling rate. This is accomplished by decimating with a ratio of 1:64. The output of this filter is a sixteen-bit, 2s-complement data word clocking at the sample rate.

NOTE

The sample rate is determined through a programmable relationship of MCLK/(Fk $\times$ 256), Fk = 1,2,3,...,256

2.1.8 Sigma-Delta DAC

The sigma-delta DAC is a fourth-order, sigma-delta modulator with 64-times oversampling. The DAC provides high-resolution, low-noise performance from a one-bit converter using oversampling techniques.

2.1.9 Interpolation Filter

The interpolation filter resamples the digital data at a rate of 64 times the incoming sample rate. The high-speed data output from this filter is then used in the sigma-delta DAC.

2.1.10 Switched-Capacitor Filter (SCF)

A switched-capacitor filter network is implemented on the analog output to provide low-pass operation with high rejection in the stop band.

2.1.11 Analog/Digital Loopback

The loopbacks provide a means of testing the ADC/DAC channels and can be used for in-circuit, system-level tests. The loopbacks feed the appropriate output to the corresponding input on the device.

The test capabilities include an analog loopback between the two analog paths and a digital loopback between the two digital paths. Each loopback is enabled by setting the D1 or D2 bit in control 1 register (see Appendix A).

2.1.12 DAC Voltage Reference Enable

The DAC voltage reference can be disabled through the control 3 register. This allows the use of an external voltage reference applied to the DAC channel modulator. By supplying an external reference, the user can scale the output voltage range of this channel. The internal reference value is 3.6 V which provides a 6-V, peak-to-peak, differential output. The ratio of an external reference to the internal reference determines the output voltage range of the DAC channel as shown in the following equation:

$$V_{O(PP)} = \frac{V(EXT\ REF)}{3.6} \times 6\ V$$

NOTE

The distortion and noise specifications listed in Section 4 Specifications apply only under the following condition:

$$\frac{V(EXT\ REF)}{3.6} \leq 1$$

2.1.13 FIR Overflow Flag

The decimator FIR filter provides an overflow flag to the control 2 register to indicate that the input to the filter has exceeded the range of the internal filter calculations. When this bit is set in the register, it remains set until the register is read by the user. Reading this value always resets the overflow flag.

2.2 Terminal Descriptions

The following sections describe the terminal functions.

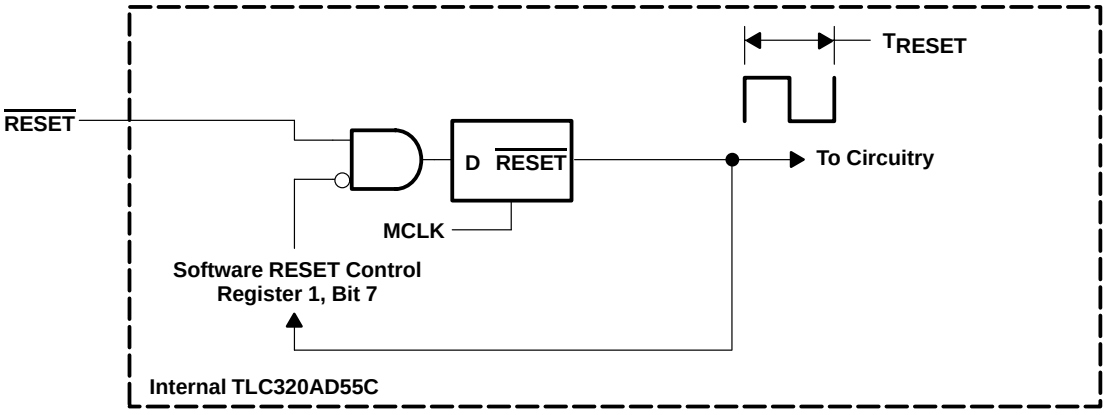
2.2.1 Reset and Power-Down

2.2.1.1 Reset

As shown in Figure 2–1, the TLC320AD55C resets both the internal counters and registers, including the programmed registers, in two ways:

- By appling a low-going reset pulse to the $\overline{\text{RESET}}$ terminal
- By writing to the programmable software reset bit (D07 in control 1 register)

$\overline{\text{PWRDWN}}$ resets the counters only and preserves the programmed register contents. The DAC resets to the 15-bit mode.



NOTE A: $\overline{\text{RESET}}$ to circuitry is at least 6 MCLK periods long and releases on the positive edge of MCLK.

Figure 2–1. Reset Function

2.2.1.2 Conditions of Reset

The two internal reset signals used for the reset and synchronization functions are:

- Counter reset – This signal resets all flip-flops and latches that are not externally programmed, with the exception of those generating the reset pulse itself. Additionally, this signal resets the software power-down bit.

  Counter reset = $\overline{\text{RESET}}$ terminal or reset bit or $\overline{\text{PWRDWN}}$ terminal

- Register reset – This signal resets all flip-flops and latches that are not reset by the counter reset, except those generating the reset pulse itself.

  Register reset = $\overline{\text{RESET}}$ terminal or reset bit

Both reset signals are at least six MCLK periods long (T_{RESET}) and release on the trailing edge of MCLK.

2.2.1.3 Software and Hardware Power-Down

Given the definitions above, the software-programmed power-down condition is cleared by programming the software bit (control 1 register bit 6) to a 0 or is cleared by cycling the power to the device, bringing $\overline{\text{PWRDWN}}$ low, or bringing $\overline{\text{RESET}}$ low (see Figure 2–2).

$\overline{\text{PWRDWN}}$ removes power to the entire chip. The software-programmable, power-down bit only removes power from the analog section of the chip, which allows a software power-up function. Cycling the power-down terminal from high to low and back to high resets all flip-flops and latches that are not externally programmed, thereby preserving the register contents with the exception that the software power-down bit is cleared.

When $\overline{\text{PWRDWN}}$ is not being used, it should be tied high [V_{DD}(ADC) is preferred].

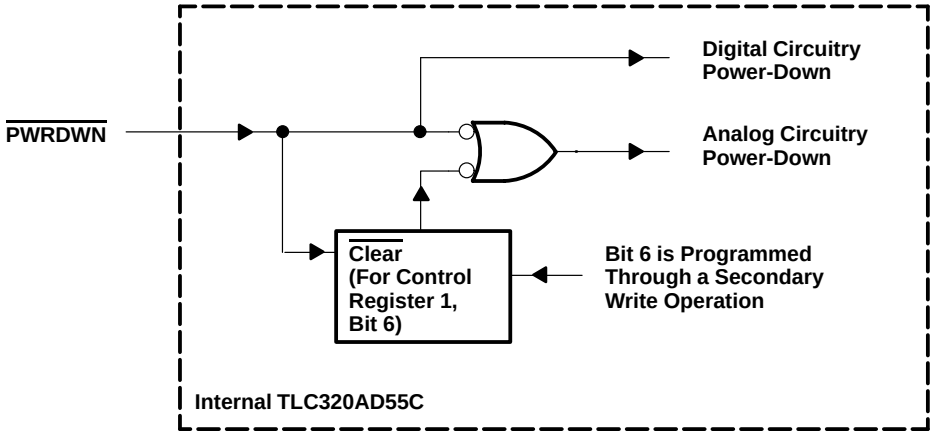


Figure 2–2. Internal Power-Down Logic

2.2.2 Master Clock Circuit

The clock circuit generates and distributes necessary clocks throughout the device. MCLK is the external master clock input. SCLK is derived from MCLK [SCLK = MCLK/(Fsclk × 2), Fsclk = 1,2,3,...,256] in order to provide clocking of the serial communications between the device and a digital signal processor (DSP). The sample rate of the data paths is set as MCLK/(Fk × 256). Fk and Fsclk are programmable register values used as divisors of MCLK. The default value for the Fk and Fsclk register is 8 (decimal).

2.2.3 Data Out (DOUT)

DOUT is taken from the high-impedance state by the falling edge of the frame-sync signal. The most significant data bit then appears on DOUT.

DOUT is placed in a high-impedance state on the sixteenth rising edge of SCLK (internal or external) after the falling edge of the frame-sync signal. In the primary communication, the data word is the ADC conversion result. In the secondary communication, the data is the register read results when requested by the read/write (R/$\overline{\text{W}}$) bit with the eight MSBs set to zero (see the serial communications section). When a register read is not requested, the secondary word is all zeroes.

2.2.4 Data In (DIN)

In the primary communication, the data word is the input digital signal to the DAC channel. In the secondary communication, the data is the control and configuration data to set up the device for a particular function (see Section 3 Serial Communications).

2.2.5 Hardware Program Terminal (FC)

This input provides for hardware programming requests for secondary communication. It works in conjunction with the control bit D00 of the secondary data word. The signal on FC is latched 1/2 shift clock after the rising edge of the next internally generated primary frame-sync interval. FC should be tied low when not being used (see Section 3.2 Secondary Serial Communication).

2.2.6 Frame-Sync

The frame-sync signal indicates that the device is ready to send and receive data. The data transfer from DOUT and into DIN begins on the falling edge of the frame-sync signal.

The frame sync is generated internally and goes low on the rising edge of SCLK and remains low during the 16-bit data transfer.

2.2.7 Multiplexed Analog Input

The two differential analog inputs (INP and INM or AUXP and AUXM) are multiplexed into the sigma-delta modulator. The performance of the AUX channel is similar to the normal input channel.

2.2.8 Analog Input

The signal applied to the terminals INM and INP should be differential to preserve the device specifications (see Figure 2–3). A single-ended input signal should always be converted to a differential input signal prior to being used by the TLC320AD55C. The signal source driving the analog inputs (INM, INP, AUXM, AUXP) should have a low source-impedance for lowest noise performance and accuracy.

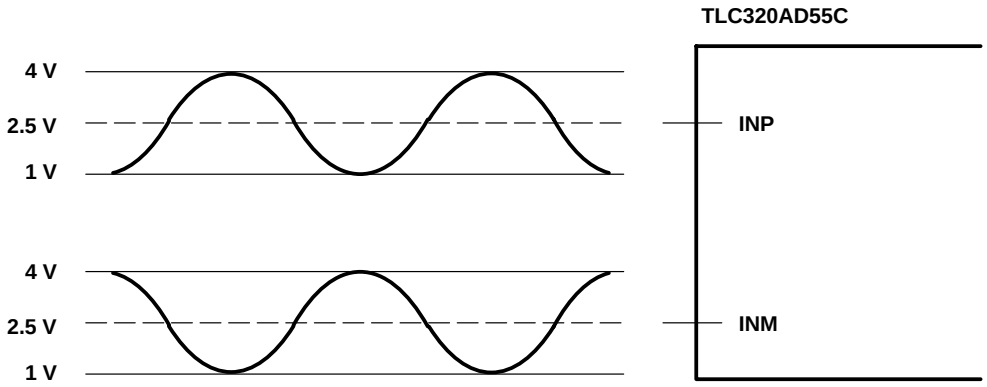


Figure 2–3. Differential Analog Input Configuration

3 Serial Communications

DOUT, DIN, SCLK, $\overline{FS}$, and FC are the serial communication signals. The digital output data from the ADC is taken from DOUT. The digital input data for the DAC is applied to DIN. The synchronizing clock for the serial communication data and the frame sync is taken from SCLK. The frame-synchronization pulse that encloses the ADC/DAC data transfer interval is taken from $\overline{FS}$. For signal (audio) data transmitted from the ADC or to the DAC, primary serial communication is used. To read or write words that control both the options and the circuit configurations of the device, secondary communication is used.

The purpose of the primary and secondary communications is to allow conversion data and control data to be transferred across the same serial port. A primary transfer is always dedicated to conversion data. A secondary transfer sets up and reads the register values described in Appendix A. A primary transfer occurs for every conversion period. A secondary transfer occurs only when requested. Two methods exist for requesting a secondary command. Terminal FC can request a secondary communication when it is asserted, or the LSB of the DAC data within a primary transfer can request a secondary communication. The selection of which method is enabled is provided in control 1 register (bit 0) as shown in Appendix A.

For all serial communications, the most significant bit is transferred first. For a 16-bit ADC word and a 16-bit DAC word, D15 is the most significant bit and D0 is the least significant bit. For a 15-bit DAC data word in the 16-bit primary communication, D15 is the most significant bit, D1 is the least significant bit, and D0 is used for the embedded function control. All digital data values are in 2s-complement format.

These logic signals are compatible with TTL-voltage levels and CMOS current levels.

3.1 Primary Serial Communication

Primary serial communication is used both to transmit and receive conversion signal data. The ADC word length is always 16 bits. The DAC word length depends on the status of D0 in the control 1 register. After power-up or reset, the device defaults to the 15-bit mode (not 16-bit mode). The DAC word length is 15 bits and the last bit of the primary 16-bit serial communication word is a function-control bit used to request secondary serial communications. In the 16-bit mode, all 16 bits of the primary communications word are used as data for the DAC and the hardware terminal FC must be used to request secondary communications.

Figure 3–1 shows the timing relationship for SCLK, $\overline{FS}$, DOUT and DIN in a primary communication. The timing sequence for this operation is as follows:

1. The TLC320AD55C takes $\overline{FS}$ low.
2. One 16-bit word is transmitted from the ADC (DOUT) and one 16-bit word is received for the DAC (DIN).
3. The TLC320AD55C takes $\overline{FS}$ high.

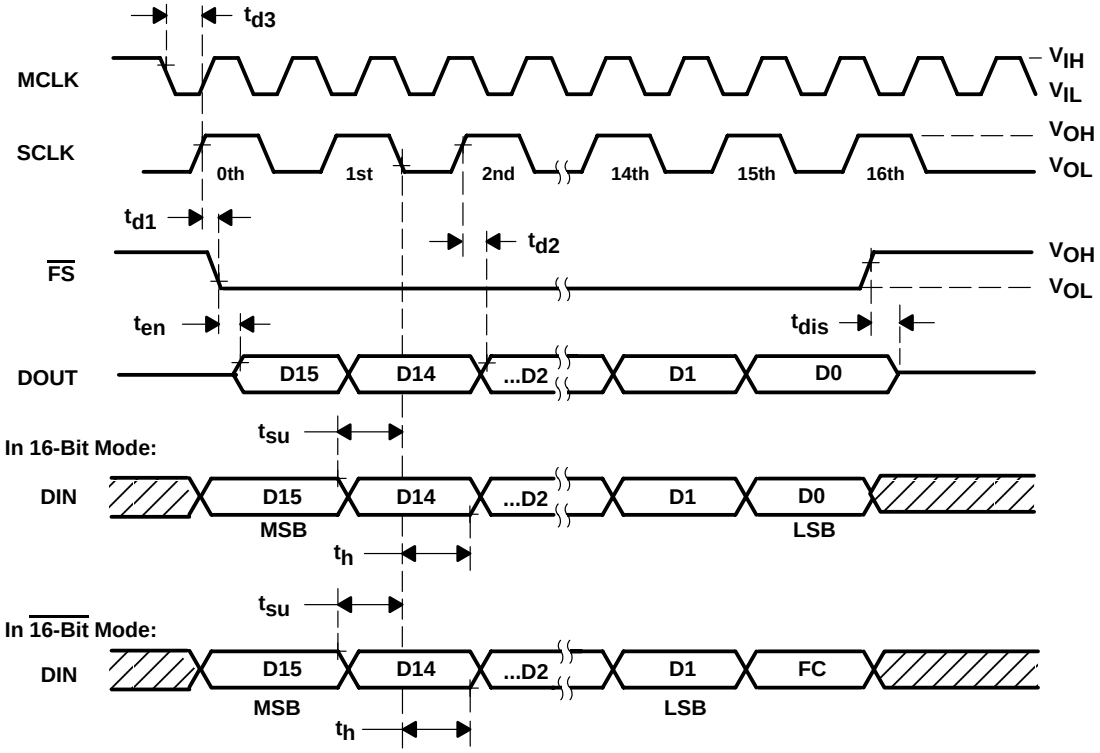


Figure 3–1. Primary Serial Communication Timing

When a secondary request is made through the LSB of the DAC data word ($\overline{16\text{-bit}}$ mode), the format shown in Figure 3–2 is used:

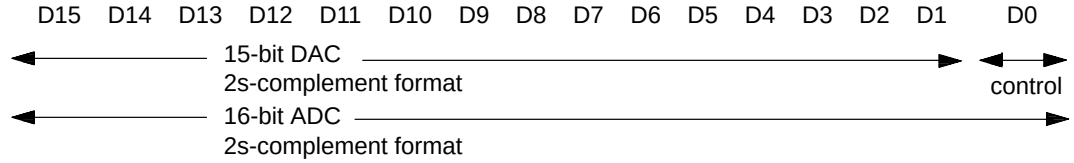


Figure 3–2. DAC and ADC Word Lengths

3.2 Secondary Serial Communication

Secondary serial communication reads or writes 16-bit words that program both the options and the circuit configurations of the device. All register programming occurs during secondary communications. Four primary and secondary communication cycles are required to program the four registers. When the default value for a particular register is desired, the user can omit addressing it during secondary communication. A no-op command addresses the no-op register (register 0), and no register programming takes place during this secondary communication.

There are two methods for initiating secondary communications (see Figure 3–3):
1) by asserting a high level on FC, or 2) by asserting the LSB of DIN 16-bit serial communication high while not in 16-bit mode (see control 1 register bit 0).

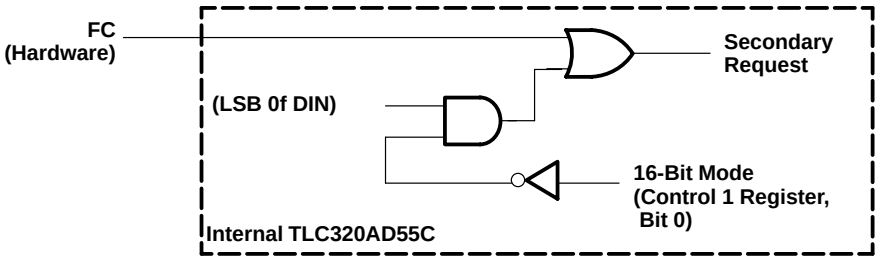


Figure 3–3. Hardware and Software Methods to Initate a Secondary Request

1. Figures 3–5 and 3–6 show the two different methods by which FC requests secondary communication words as well as the timing for $\overline{FS}$, DOUT, DIN, and SCLK. The examples span two primary communication frames. Figure 3–5 shows the use of hardware function control.

   During a secondary communication, a register can be written to or read from. When writing a value to a register, DIN contains the value to be written (see Figure 3–7). The data returned on DOUT is 00(hex). When performing a read function, DIN can still provide data to be written to an addressed register; however, DOUT contains the most recent value contained in the register addressed by DIN.

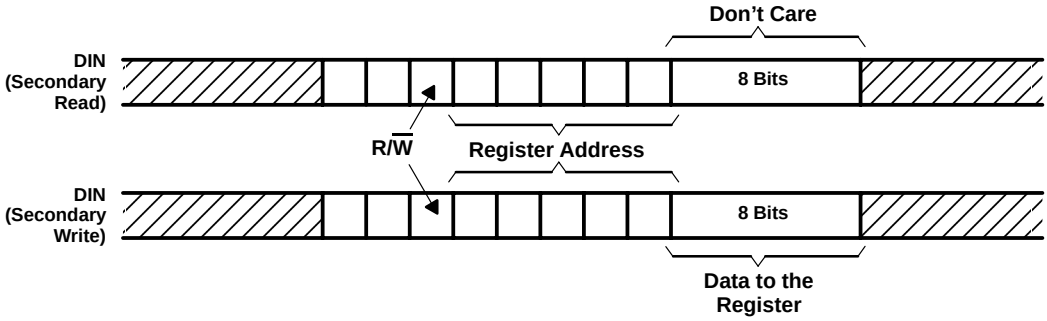


Figure 3–4. Secondary DIN Format

   In Figure 3–5, FC clocks in and latches on the rising edge of frame sync ($\overline{FS}$). This causes the start of the secondary update 32 FCLKs (see Fk divide register, Appendix A) after the start of the primary communication frame. Read and write examples are shown for DIN and DOUT.

2. Figure 3–6 shows the use of software function control.

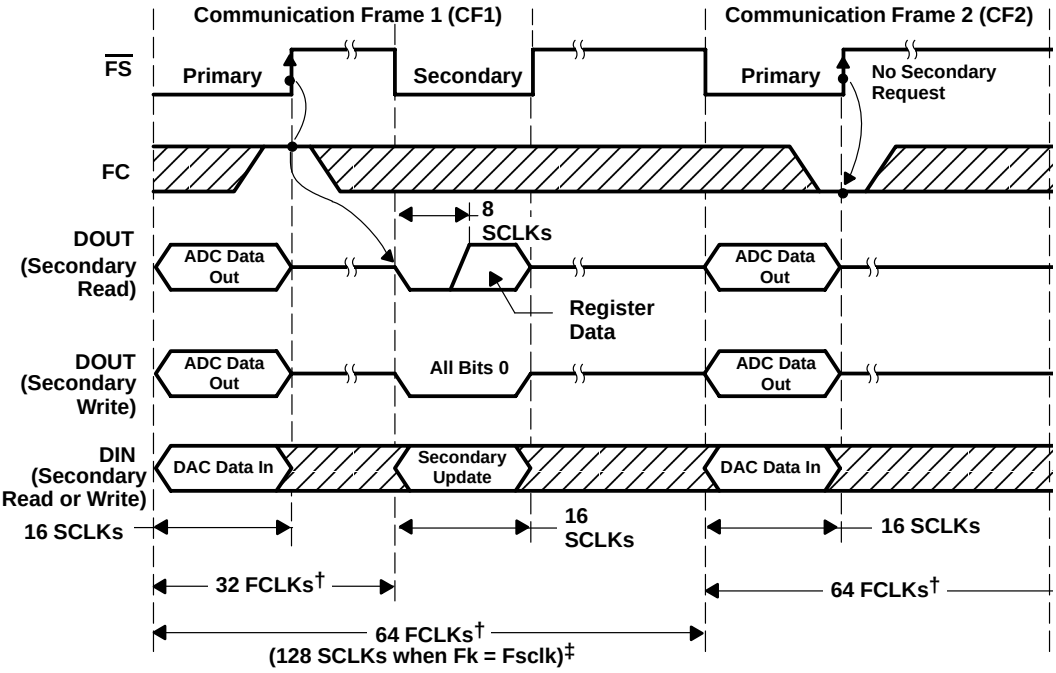
   The software request for function control is typically used when the required resolution of the DAC channel is less than 16 bits. Then the least significant bit (D0) can be used for the secondary requests as shown in Table 3–1.

Table 3–1. Least-Significant-Bit Control Function

CONTROL BIT D0	CONTROL BIT FUNCTION
0	No operation (no-op)
1	Secondary communication request

On the falling edge of the next $\overline{FS}$, D15 through D1 is input to DIN or D15 through D0 is output to DOUT.

When a secondary communication request is made, $\overline{FS}$ goes low for 32 FCLKs (see Fk divide register, Appendix A) after the beginning of the primary frame.

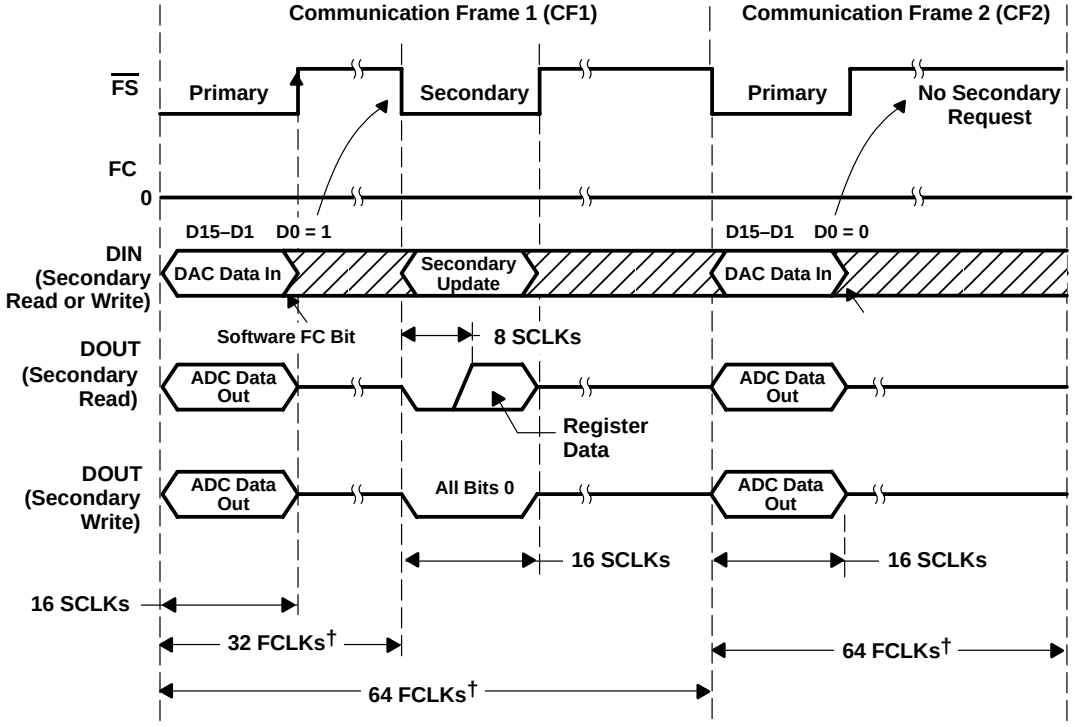


† See Fk divide register in Appendix A.

‡ For a selected MCLK, Fk and Fsclk: SCLK = 2 Fk/Fsclk × FCLK

Figure 3–5. Hardware FC Secondary Request (Phone Mode Disabled)

In Figure 3–6, FC hardware terminal 15 is left in its nonasserted state (0). FC is asserted through software by embedding an asserted high level (1) in the LSB of the 16-bit primary word. This is possible when not in 16-bit mode (control 1 register bit 2 = 0) because the user is using only 15 bits of DAC information.



† See Fk divide register in Appendix A.

NOTE A: For a read cycle, the last 8 bits are don't care.

Figure 3–6. Software FC Secondary Request (Phone Mode Disabled)

Table 3–2 shows the secondary communications format. D13 is the R/$\overline{W}$ bit, the read/not-write bit.

D12 through D8 are address bits. The register map is specified in the register set section in Appendix A. D7 through D0 are data bits. The data bits are values for the specified register addressed by data bits D12 through D8.

Table 3–2. Secondary Communication Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	R/$\overline{W}$	A	A	A	A	A	D	D	D	D	D	D	D	D

3.3 Conversion Rate Versus Serial Port

The SCLK frequency can be programmed independently from the FCLK frequency. This can create a problem with the interpretation of the serial port data. The serial port is designed to initiate a primary communication every 64 SCLKs. There must be an integer number of SCLKs ≥ 40 per sample period. Two examples follow to demonstrate the possible output of the serial port. SCLK must be fast enough to collect all data from each frame.

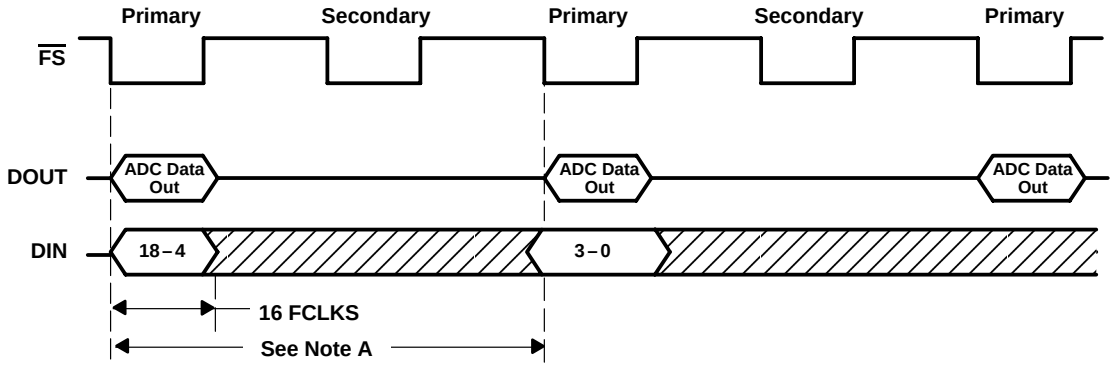
Example 1: MCLK = 4.096 MHz, sample rate = 8 kHz, 8 kHz = MCLK/(Fk × 256), set Fk = 2, SCLK = MCLK/(Fsclk × 2), set Fsclk = 2, SCLK = 1.024 MHz. With this configuration, SCLK = sample rate × 128. Therefore, each primary communication is a valid sample.

Example 2: All variables above remain the same except Fsclk = 1, SCLK = 2.048 MHz = sample rate × 256. In this configuration, two consecutive primary communications represent the same data sample.

3.4 FIR Bypass Mode

An option is provided to bypass the FIR sections of the decimation filter and the interpolation filter. This is selected through the control 2 register. The sinc filters of the two paths cannot be bypassed.

The timing requirements for this mode of operation are shown in Figure 3–7.



NOTE A: The number of clocks between primary cycles is a function of FCLK. When either FIR is bypassed, this period is 16 FCLKs. See Fk divide register in Appendix A.

Figure 3–7. FIR Bypass Timing

3.5 Phone Mode Control

This function is provided for applications that need hardware control and monitor of external events. By allowing the device to drive two FLAG terminals (set through the control 2 register), the host digital signal processor (DSP) is capable of system control through the same serial port connection to the device. Along with this control is the capability for monitoring the value of the ALT DATA terminal during a secondary communication cycle. One application for this function is in monitoring ring detect or offhook detect from a phone answering system. The two FLAG terminals allow response to these incoming control signals. Figure 3–8 shows the timing associated with this operating mode.

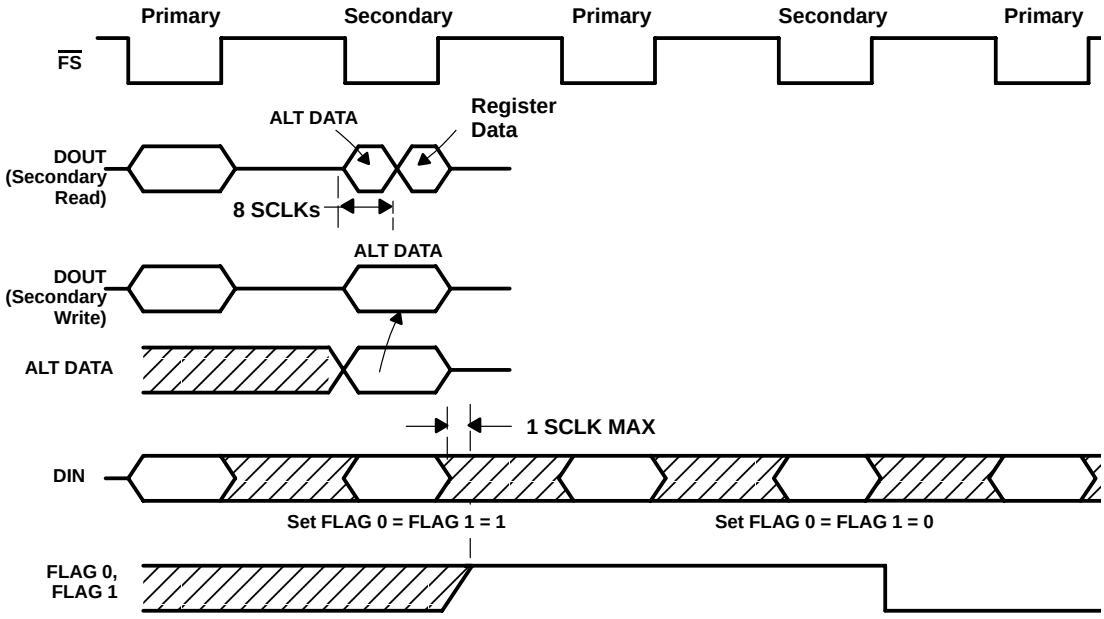


Figure 3–8. Phone Mode Timing

4 Specifications

4.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage range, DV_{DD}, V_{DD}(ADC, DAC)(see Note 1) . . . . . –0.3 V to 6.5 V
Output voltage range, DOUT, $\overline{FS}$, SCLK, FLAG 0, FLAG 1 . . . –0.3 V to DV_{DD} + 0.3 V
Output voltage range, OUTP, OUTM . . . . . –0.3 V to V_{DD} + 0.3 V
Input voltage range, DIN, $\overline{PWRDWN}$, $\overline{RESET}$, ALT DATA,
MCLK, FC . . . . . –0.3 V to DV_{DD} + 0.3 V
Input voltage range, INP, INM, AUXP, AUXM . . . . . –0.3 V to V_{DD} + 0.3 V
Case temperature for 10 seconds, T_C: DW package . . . . . 260°C
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}(DAC) for DAC channel measurements and V_{SS}(ADC) for ADC channel measurements.

4.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}(ADC, DAC)		4.5		5.5	V
Analog signal input voltage, V_I	Differential, (INP – INM) peak, for full scale operation			6	V
Load resistance for OUTP and OUTM, R_L		0.3	10		kΩ
Load capacitance for OUTP and OUTM, C_L				100	pF
ADC or DAC conversion rate (Nyquist)			8		kHz
Operating free-air temperature, T_A		0		70	°C

4.3 Recommended Operating Conditions, DV_{DD} = 5 V

	MIN	NOM	MAX	UNIT
Supply voltage, DV_{DD}	4.5		5.5	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
MCLK frequency (see Note 2), duty cycle = 50 ±10%		16.384		MHz

NOTE 2: The default state for an 8 kHz conversion rate requires a 16.384 MHz MCLK frequency.

4.4 Electrical Characteristics, T_A = 25°C, V_{DD}(ADC) = V_{DD}(DAC) = DV_{DD} = 5 V, MCLK = 16.384 MHz, Fk = 8 (unless otherwise noted)

4.4.1 Digital Inputs and Outputs, Outputs Not Loaded

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, DOUT	I_O = 360 µA	2.4	4.6		V
V_{OL}	Low-level output voltage, DOUT	I_O = 2 mA		0.2	0.4	V
I_{IH}	High-level input current, any digital input	V_{IH} = 5 V			10	µA
I_{IL}	Low-level input current, any digital input	V_{IL} = 0.8 V			10	µA
C_i	Input capacitance			5		pF
C_o	Output capacitance			5		pF

4.4.2 ADC Path Filter (see Note 3)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	20 Hz	–0.5	–0.15	0.2	dB
	200 Hz	–0.5	0.03	0.15	
	300 Hz to 3 kHz	–0.15	0	0.15	
	3.3 kHz	–0.35	–0.5	0.3	
	3.4 kHz	–1	–0.6	–0.1	
	4 kHz		–20	–14	
	≥ 4.6 kHz			–40	

NOTE 3: The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The analog input test signal is a sine wave with 0 dB = 6 $V_{I(PP)}$ as the reference level for the analog input signal. The passband is 0 to 3400 Hz.

4.4.3 ADC Dynamic Performance

4.4.3.1 ADC Signal-to-Noise (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio (SNR)	V_I = –1 dB	80	85		dB
	V_I = –9 dB	72	77		
	V_I = –40 dB	40	45		
	V_I = –65 dB	14	21		
	$V_{I(AUXM, AUXP)}$ = –9 dB	72	78		

NOTE 4: The test condition is the digital equivalent of a 1020 Hz input signal with an 8 kHz conversion rate. The load impedance is 600 Ω. Input and output voltages are referred to V_{DD}/2.

4.4.3.2 ADC Signal-to-Distortion (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion (THD)	V_I = –1 dB	80	92		dB
	V_I = –9 dB	80	94		
	V_I = –40 dB	40	60		
	V_I = –65 dB	15	40		
	$V_{I(AUXM, AUXP)}$ = –9 dB	80	92		

NOTE 4: The test condition is the digital equivalent of a 1020 Hz input signal with an 8 kHz conversion rate. The load impedance is 600 Ω. Input and output voltages are referred to V_{DD}/2.

4.4.3.3 ADC Signal-to-Distortion+Noise (see Note 5)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total harmonic distortion+noise (THD+N)	$V_I = -9$ dB	80	83		dB
	$V_I = -1$ dB	72	76		
	$V_I = -40$ dB	40	45		
	$V_I = -65$ dB	14	20		
	$V_{I(AUXM, AUXP)} = -9$ dB	72	77		

NOTE 5: The test condition is a 1020 Hz input signal with an 8 kHz conversion rate. Input and output voltages are referred to $V_{DD}/2$.

4.4.4 ADC Channel

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Dynamic range			86		dB
	Interchannel isolation		80			dB
	Gain error	$V_I = -1$ dB at 1020 Hz			±0.5	dB
	Gain error, dc	INP = 3 V, INM = 2 V		±0.6		dB
	Off-set error, ADC converter			8		mV
CMRR	Common-mode rejection ratio INM, INP or AUXM, AUXP	V_I = 0 dB at 1020 kHz	80			dB
	Idle channel noise (on-chip reference)				50	μV rms
R_i	Input resistance	T_A = 25°C	70	100		kΩ

4.4.5 DAC Path Filter (see Note 6)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	20 Hz	–0.5	0.08	0.15	dB
	200 Hz	–0.5	0.08	0.15	
	300 Hz to 3 kHz	–0.15	0.08	0.15	
	3.3 kHz	–0.35	0.11	0.3	
	3.4 kHz	–1	–.48	–0.1	
	4 kHz		–20	–14	
	≥ 4.6 kHz			–40	

NOTE 6: The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dB). The nominal differential DAC channel peak-to-peak output voltage with this input condition is 6 V. The pass band is 0 to 3600 Hz.

4.4.6 DAC Dynamic Performance

4.4.6.1 DAC Signal-to-Noise (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio (SNR)	V_O = 0 dB	74	80		dB
	V_O = –9 dB	70	74		
	V_O = –40 dB	38	44		
	V_O = –65 dB	14	18		

NOTE 4: The test condition is the digital equivalent of a 1020 Hz input signal with an 8 kHz conversion rate. The load impedance is 600 Ω. Input and output voltages are referred to $V_{DD}/2$.

4.4.6.2 DAC Signal-to-Distortion (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion (THD)	V_O = 0 dB	74	84		dB
	V_O = –9 dB	74	84		
	V_O = –40 dB	40	58		
	V_O = –65 dB	18	30		

NOTE 4: The test condition is the digital equivalent of a 1020 Hz input signal with an 8 kHz conversion rate. The load impedance is 600 Ω. Input and output voltages are referred to $V_{DD}/2$.

4.4.6.3 DAC Signal-to-Distortion+Noise (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total harmonic distortion+noise (THD+N)	V_O = 0 dB	72	78		dB
	V_O = –9 dB	68	74		
	V_O = –40 dB	38	44		
	V_O = –65 dB	14	20		

NOTE 4: The test condition is the digital equivalent of a 1020 Hz input signal with an 8 kHz conversion rate. The load impedance is 600 Ω. Input and output voltages are referred to $V_{DD}/2$.

4.4.7 DAC Channel

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Dynamic range			80		dB
	Interchannel isolation		80			dB
	Gain error, 0 dB	V_O = 0 dB at 1020 Hz			±0.5	dB
	Gain error, dc	Digital input offset = 1 V dc		±0.2		dB
	Idle channel broad-band noise	See Note 7			100	µV rms
	Idle channel narrow-band noise	0 – 4 kHz, See Note 7			40	µV rms
V_{OO}	Output offset voltage at OUT (differential)	DIN = All 0s		8		mV
V_O	Analog output voltage, peak-to-peak, OUTP – OUTM (differential)	R_L = 600, With internal reference and full-scale digital input, (see Note 8)			6	V

NOTES: 7. The conversion rate is 8 kHz; the out-of-band measurement is made from 4800 Hz to $F_{MCLK}/2$.
8. The digital input to the DAC channel at DIN is in 2s complement.

4.4.8 Power Supplies, V_{DD}(ADC) = V_{DD}(DAC) = DV_{DD} = 5 V, No Load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD} (ADC)	Power supply current, ADC	Operating		12	20	mA
		Power-down		400		µA
I_{DD} (DAC)	Power supply current, DAC	Operating		16	24	mA
		Power-down		2.5		mA
I_{DD} (Digital)	Power supply current, digital	Operating		2	6	mA
		Power-down		300		µA
P_D	Power dissipation	Operating		150	250	mW
		Power-down		16	30	

4.4.9 Timing Requirements (see Notes 9 and 10)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d1}	Delay time, SCLK↑ to $\overline{FS}$↓	C_L = 20 pF		10	15	ns
t_{d2}	Delay time, SCLK↑ to DOUT			6	20	
t_{su}	Setup time, DIN before SCLK↓		20			
t_h	Hold time, DIN after SCLK↓				20	
t_{en}	Enable time, $\overline{FS}$↓ to DOUT			10	25	
t_{dis}	Disable time, $\overline{FS}$↑ to DOUT Hi-Z			20		
t_{d3}	Delay time MCLK↓ to SCLK↑			25	50	

NOTES: 9. Refer to Figure 3–1 for timing diagram.
10. When $\overline{FS}$ occurs after SCLK, it shortens the MSB (D15) duration.

5 Application Information

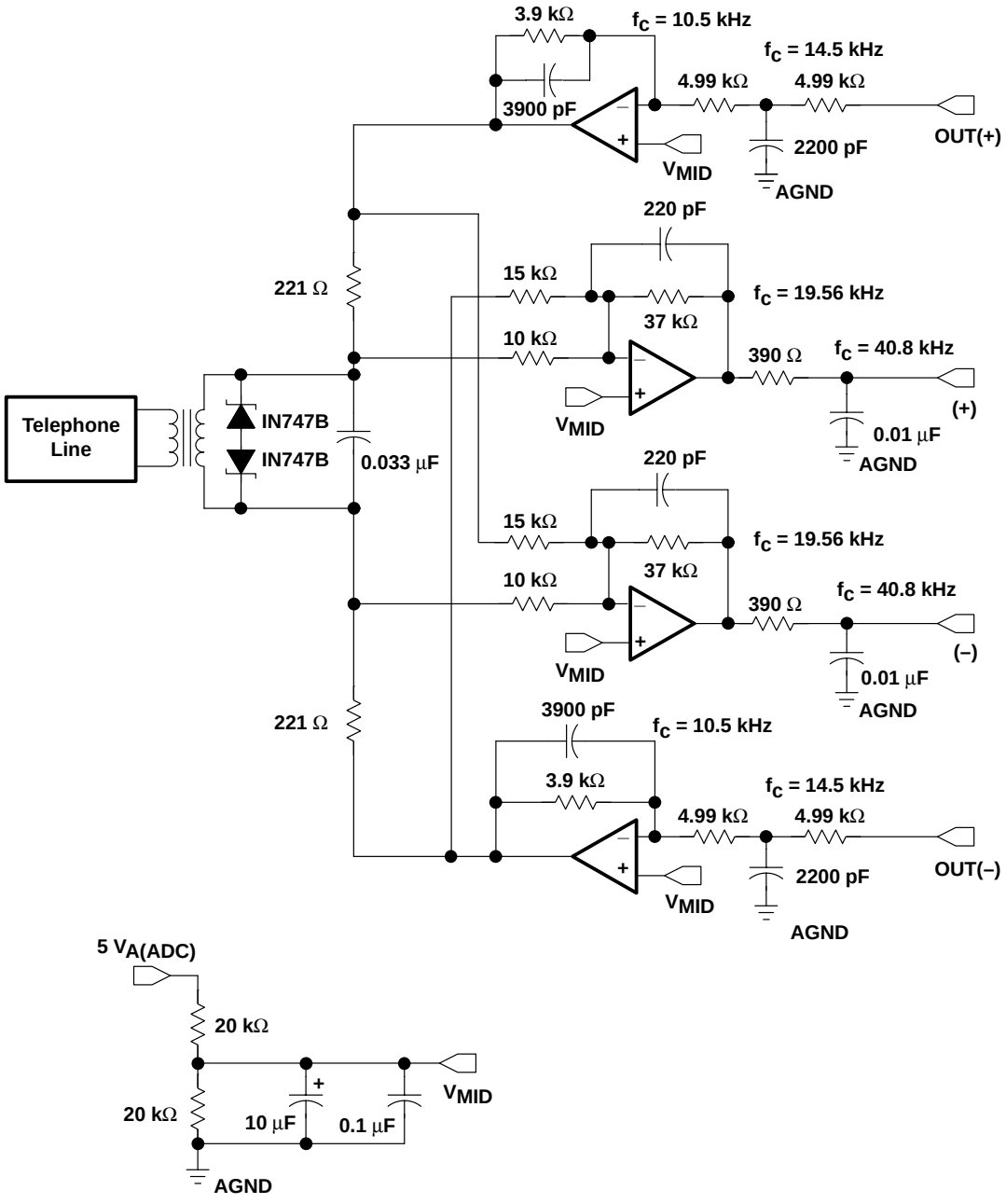


Figure 5–1. TLC320AD55C Application Schematic

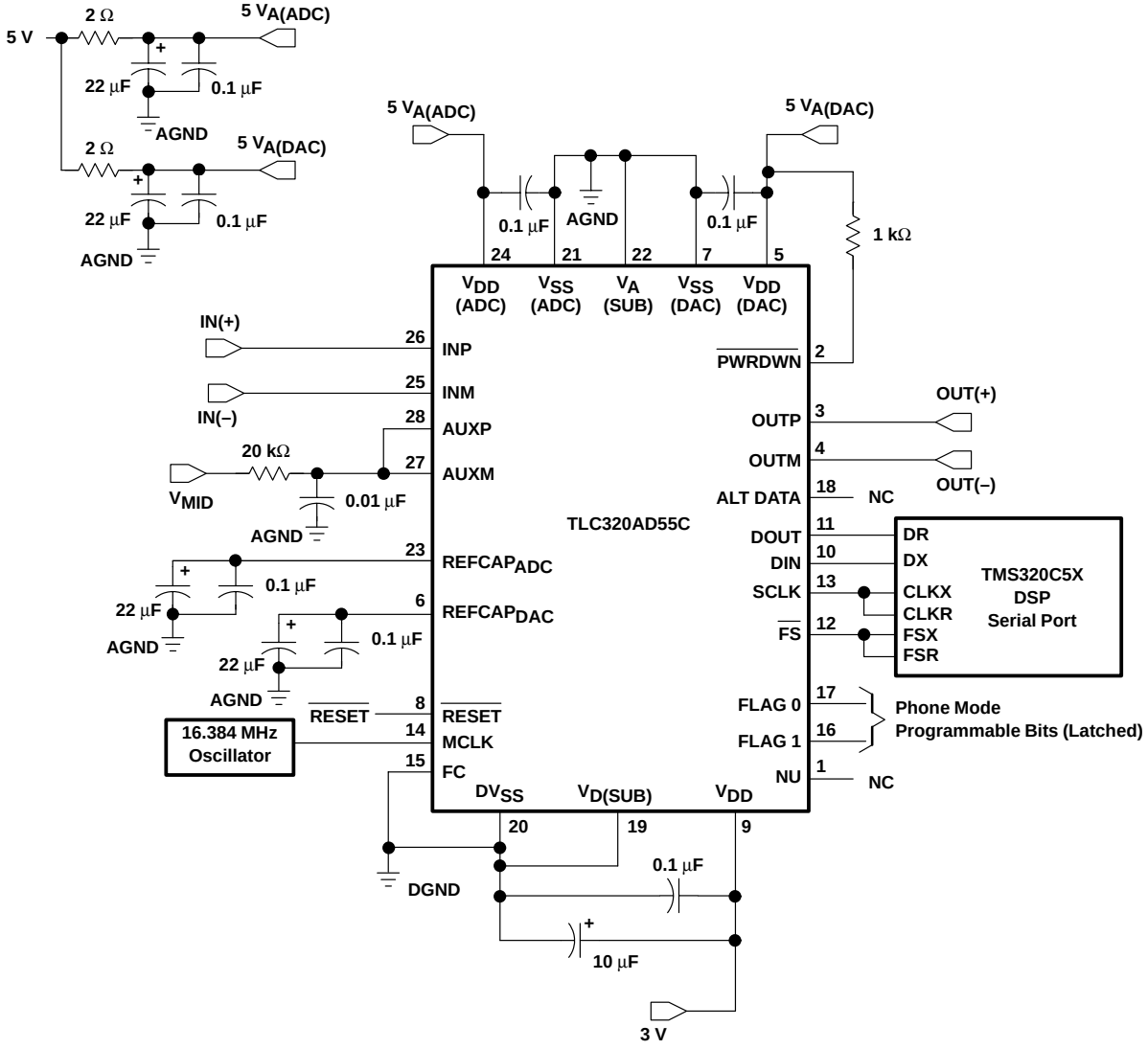


Figure 5–2. TLC320AD55C I/O Buffer and V_{MID} Generator Schematic

Appendix A
Register Set

Data bits D12 through D8 in the secondary serial communication contain the address of the register, and data bits D7 through D0 contain the data that is to be written to the register. Data bit D13 determines a read or write cycle to the addressed register. When data bit D13 is low, a write cycle is selected.

The following table shows the register map:

Table A–1. Register Map

REGISTER NO.	D15	D14	D13	D12	D11	D10	D9	D8	REGISTER NAME
0	0	0	0	0	0	0	0	0	No operation
1	0	0	0	0	0	0	0	1	Control 1
2	0	0	0	0	0	0	1	0	Control 2
3	0	0	0	0	0	0	1	1	Fk divide
4	0	0	0	0	0	1	0	0	Fsclk divide
5	0	0	0	0	0	1	0	1	Control 3

Table A–2. Control 1 Register

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	–	–	–	–	–	–	–	Software reset
0	–	–	–	–	–	–	–	Software reset not asserted
–	1	–	–	–	–	–	–	Software power down (analog and filters)
–	0	–	–	–	–	–	–	Software power down (not asserted)
–	–	1	–	–	–	–	–	Select AUXP and AUXM
–	–	0	–	–	–	–	–	Select INP and INM
–	–	–	0	0	–	–	–	Analog output gain = 1
–	–	–	0	1	–	–	–	Analog output gain = 1/2
–	–	–	1	0	–	–	–	Analog output gain = 1/4
–	–	–	1	1	–	–	–	Analog output gain = 0 (squelch)
–	–	–	–	–	1	–	–	Analog loopback asserted
–	–	–	–	–	0	–	–	Analog loopback not asserted
–	–	–	–	–	–	1	–	Digital loopback asserted
–	–	–	–	–	–	0	–	Digital loopback not asserted
–	–	–	–	–	–	–	1	16-bit mode (hardware secondary requests)
–	–	–	–	–	–	–	0	Not 16-bit mode (software secondary requests)

Default register value: 00000000

The software reset is a one-shot operation and this bit is cleared to zero after reset. It is not necessary to write a zero to end the master reset operation.

Table A–3. Control 2 Register

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
X	X	–	–	–	–	–	–	Reserved
–	–	X	–	–	–	–	–	Decimator FIR overflow flag (valid only during read cycle)
–	–	–	X	–	–	–	–	FLAG 1 output value
–	–	–	–	X	–	–	–	FLAG 0 output value
–	–	–	–	–	1	–	–	Phone mode enabled
–	–	–	–	–	0	–	–	Phone mode disabled
–	–	–	–	–	–	0	–	Normal operation with decimator FIR filter
–	–	–	–	–	–	1	–	Bypass decimator FIR filter
–	–	–	–	–	–	–	0	Normal operation with interpolator filter
–	–	–	–	–	–	–	1	Bypass interpolator FIR filter

Default register value: 00000000

Writing zeros to the reserved bits is suggested.

Table A–4. Fk Divide Register

D7	D6	D5	D4	D3	D2	D1	D0	DIVIDE VALUE
1	1	1	1	1	1	1	1	255
⋮						⋮		
1	0	0	0	0	0	0	0	128
⋮						⋮		
0	0	1	0	0	0	0	0	32
⋮						⋮		
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	256

Default register value: 00001000

The oversampling clock (FCLK) is set as MCLK/(Fk $\times$ 4). MCLK/(Fk $\times$ 256) is the sample frequency (conversion rate) for the converter. When Fk is programmed to zero, its value is interpreted as 256.

Table A–5. Fsclk Divide Register

D7	D6	D5	D4	D3	D2	D1	D0	DIVIDE VALUE
1	1	1	1	1	1	1	1	255
			●			●		
			●			●		
			●			●		
1	0	0	0	0	0	0	0	128
			●			●		
			●			●		
			●			●		
0	0	1	0	0	0	0	0	32
			●			●		
			●			●		
			●			●		
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	256

Default register value: 00001000

SCLK is set by MCLK/(2 × Fsclk). SCLK is for the serial transfer of data to and from the TLC320AD55C. When Fsclk is programmed to zero, its value is interpreted as 256.

Table A–6. Control 3 Register

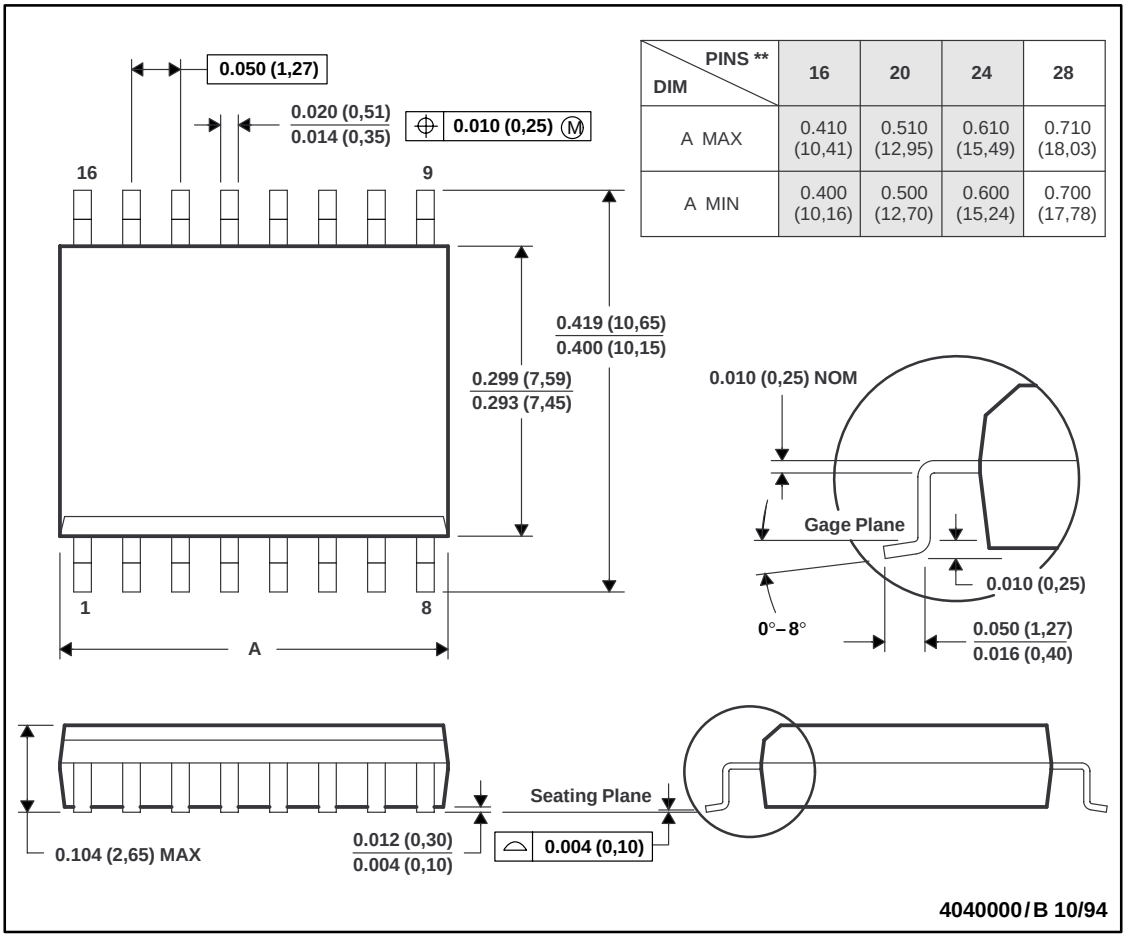
D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
0	0	0	0	1	0	0	0	DAC reference disabled
0	0	0	0	0	0	0	0	DAC reference enabled

Appendix B

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.