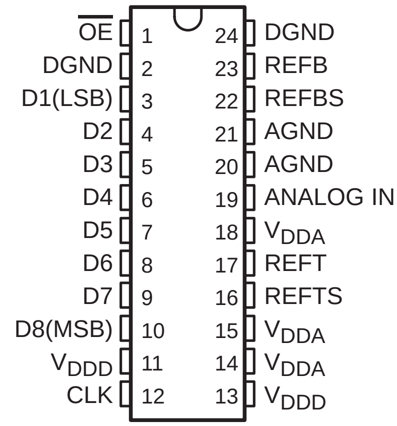
- **8-Bit Resolution**
- **Integral Linearity Error**
  ±0.75 LSB Max (25°C)
  ±1 LSB Max (–35°C to 85°C)
- **Differential Linearity Error**
  ± 0.5 LSB (25°C)
  ±0.75 LSB Max (–35°C to 85°C)
- **Maximum Conversion Rate**
  10 Mega-Samples per Second (MSPS) Min
- **2.7-V to 3.6-V Single-Supply Operation**
- **Low Power Consumption . . . 42 mW Typ at 3 V**
- **Low Voltage Replacement for CXD1175**

Applications

- **Communications**
- **Digital Imaging**
- **Video Conferencing**
- **High-Speed Data Conversion**

NS PACKAGE†
(TOP VIEW)



† Also available in tape and reel and ordered as the TLV5510INSR.

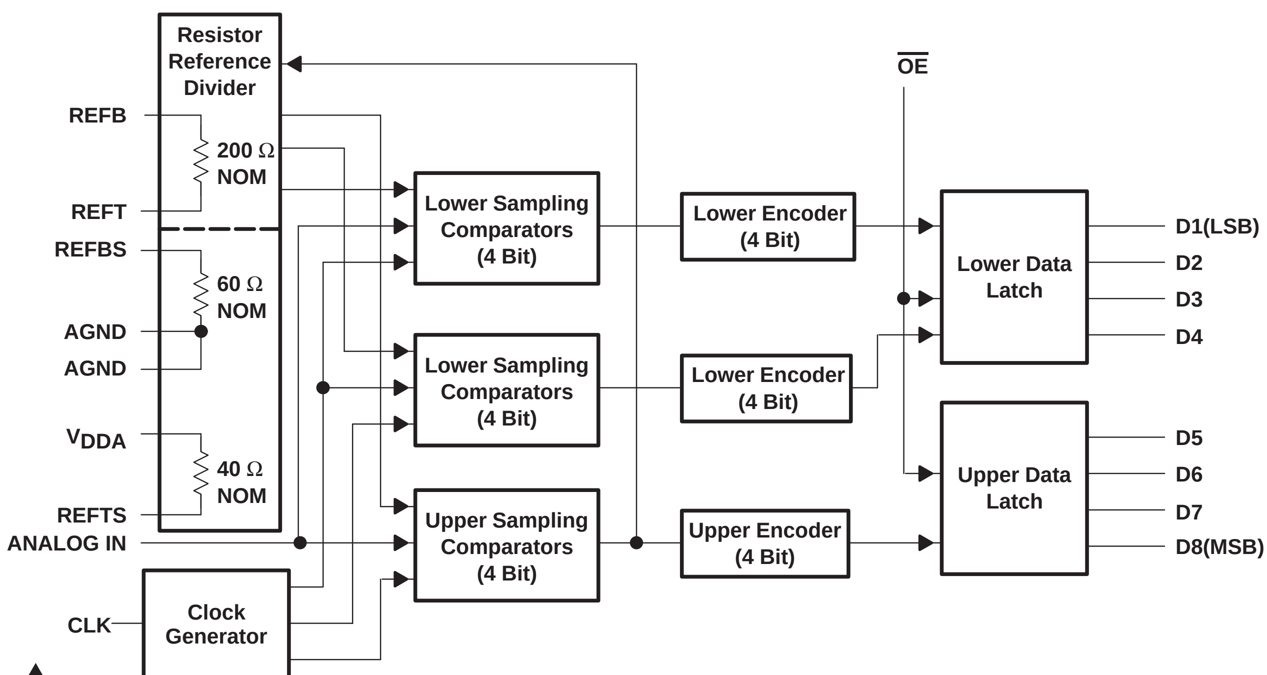
AVAILABLE OPTIONS

T_A	SOP (NS) PACKAGE
–35°C to 85°C	TLV5510INS

description

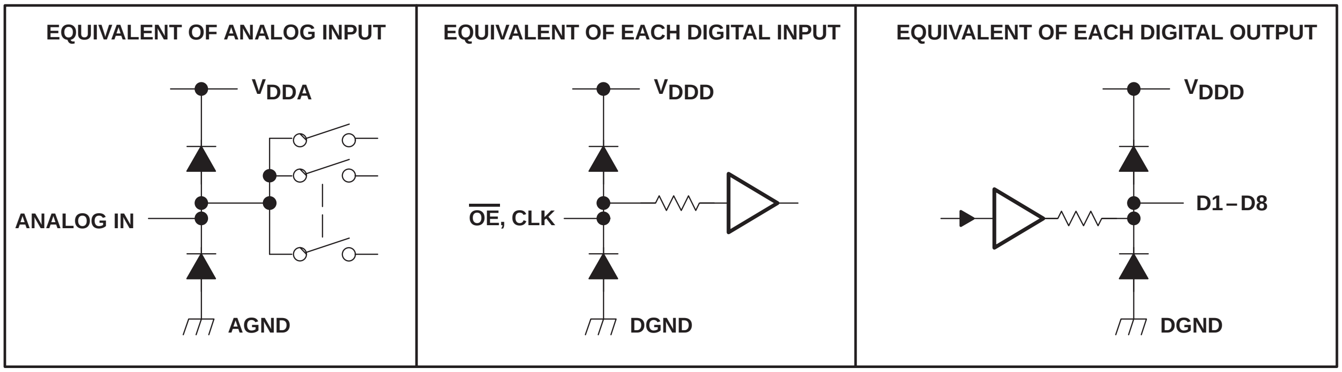
The TLV5510 is a CMOS 8-bit resolution semiflash analog-to-digital converter (ADC) with a 2.7-V to 3.6-V single power supply and an internal reference voltage source. It converts a wide band analog signal (such as a video signal) to a digital signal at a sampling rate of dc to 10 MHz.

functional block diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

schematics of inputs and outputs



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	20, 21		Analog ground
ANALOG IN	19	I	Analog input
CLK	12	I	Clock input
DGND	2, 24		Digital ground
D1 – D8	3 – 10	O	Digital data out. D1:LSB, D8:MSB
$\overline{OE}$	1	I	Output enable. When $\overline{OE}$ = low, data is enabled. When $\overline{OE}$ = high, D1 – D8 is high impedance.
V_{DDA}	14, 15, 18		Analog supply voltage
V_{DDD}	11, 13		Digital supply voltage
REFB	23	I	Reference voltage in (bottom)
REFBS	22		Reference voltage (bottom). When using the internal voltage divider to generate a nominal 2-V reference, this terminal is shorted to the REFB terminal and the REFTS terminal is shorted to the REFT terminal (see Figure 21).
REFT	17	I	Reference voltage in (top)
REFTS	16		Reference voltage (top). When using the internal voltage divider to generate a nominal 2-V reference, this terminal is shorted to the REFT terminal and the REFBS terminal is shorted to the REFB terminal (see Figure 21).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DDA}, V_{DDD} . . . . 7 V
Reference voltage input range, REFT, REFB, REFBS, REFTS . . . . AGND to V_{DDA}
Analog input voltage range, $V_{I(ANLG)}$ . . . . AGND to V_{DDA}
Digital input voltage range, $V_{I(DGTL)}$ . . . . DGND to V_{DDD}
Digital output voltage range, $V_{O(DGTL)}$ . . . . DGND to V_{DDD}
Operating free-air temperature range, T_A . . . . –35°C to 85°C
Storage temperature range, T_{stg} . . . . –55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage	V_{DDA} – AGND	2.7	3	3.6	V
	V_{DDD} – DGND	2.7	3	3.6	V
	AGND – DGND	–100	0	100	mV
Reference input voltage (top), REFT		REFB+2		VDDA–0.3	V
Reference input voltage (bottom), REFB		0	0.6	REFT–2	V
Analog input voltage range, $V_{I(ANLG)}$ (see Note 1)		REFB		REFT	V
High-level input voltage, V_{IH}		2.5			V
Low-level input voltage, V_{IL}				0.5	V
Pulse duration, clock high, $t_{w(H)}$		10			ns
Pulse duration, clock low, $t_{w(L)}$		10			ns
Clock frequency, $f_{(CLK)}$				10	MHz
Sampling frequency, f_S				10	MSPS

NOTE 1: REFT – REFB ≤ 2.4 V maximum

electrical characteristics at V_{DDD} = V_{DDA} = 3 V, REFT = 2.5 V, REFB = 0.5 V, $f_{(CLK)}$ = 10 MHz, T_A = 25°C (unless otherwise noted)

digital I/O

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	V_{DDD} = MAX,	V_{IH} = V_{DDD}				5	µA
I_{IL}	Low-level input current	V_{DDD} = MAX,	V_{IL} = 0				5	µA
I_{OH}	High-level output current	$\overline{OE}$ = GND,	V_{DDD} = MIN,	V_{OH} = V_{DDD} – 0.5 V	–1.6			mA
I_{OL}	Low-level output current	$\overline{OE}$ = GND,	V_{DDD} = MIN,	V_{OL} = 0.4 V	2.6			mA
I_{OZH}	High-level high-impedance-state output leakage current	$\overline{OE}$ = V_{DDD},	V_{DDD} = MAX	V_{OH} = V_{DDD}			15	µA
I_{OZL}	Low-level high-impedance-state output leakage current	$\overline{OE}$ = V_{DDD},	V_{DDD} = MIN	V_{OL} = 0			15	µA

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

power

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	f_{sin} = 1 MHz sine wave, reference resistor dissipation is separate		4	10	mA
I_{ref}	Reference voltage current	ΔREF = REFT – REFB = 2 V	6	10	14	mA

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

electrical characteristics at V_{DDD} = V_{DDA} = 3 V, REFT = 2.5 V, REFB = 0.5 V, $f_{(CLK)}$ = 10 MHz, T_A = 25°C (unless otherwise noted) (continued)

static performance

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
	Self-bias (1), at REFB	Short REFB to REFBS, Short REFT to REFTS		0.54	0.60	0.72	V
	Self-bias (1), REFT – REFB			1.8	2	2.4	
	Self-bias (2), at REFT	Short REFB to AGND, Short REFT to REFTS		2.25	2.5	3	
R_{ref}	Reference voltage resistor	Between REFT and REFB		140	200	260	Ω
C_i	Analog input capacitance	$V_{I(ANLG)}$ = 1.5 V + 0.07 V_{rms}			16		pF
	Integral nonlinearity (INL)	$f_{(CLK)}$ = 10 MHz, V_I = 0.5 V to 2.5 V	T_A = 25°C		±0.3	±0.75	LSB
			T_A = –35°C to 85°C			±1	
	Differential nonlinearity (DNL)	$f_{(CLK)}$ = 10 MHz, V_I = 0.5 V to 2.5 V	T_A = 25°C		±0.2	±0.5	
			T_A = –35°C to 85°C			±0.75	
E_{ZS}	Zero-scale error	ΔREF = REFT – REFB = 2 V		–18	–43	–68	mV
E_{FS}	Full-scale error	ΔREF = REFT – REFB = 2 V		–20	0	20	mV

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

operating characteristics at V_{DDD} = V_{DDA} = 3 V, REFT = 2.5 V, REFB = 0.5 V, $f_{(CLK)}$ = 10 MHz, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{conv}	Maximum conversion rate	f_I = 1-kHz ramp wave form, $V_{I(ANLG)}$ = 0.5 V – 2.5 V		0.2		10	MSPS
BW	Analog input bandwidth	At – 1 dB			17		MHz
		At – 3 dB			36		MHz
$t_{d(D)}$	Digital output delay time	C_L ≤ 10 pF (see Note 1 and Figure 1)			18	30	ns
t_{AJ}	Aperture jitter time				30		ps
$t_{d(s)}$	Sampling delay time				4		ns
t_{en}	Enable time, $\overline{OE}$↓ to valid data	C_L = 10 pF			15		ns
t_{dis}	Disable time, $\overline{OE}$↑ to high impedance	C_L = 10 pF			10		ns
	Spurious free dynamic range (SFDR)	Input tone = 1 MHz	T_A = 25°C		41		dB
			Full range		41		
		Input tone = 1.4 MHz	T_A = 25°C		38		
			Full range		38		
SNR	Signal-to-noise ratio	Input tone = 1.4 MHz	T_A = 25°C		38		dB
			Full range		37		

NOTE 2: C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

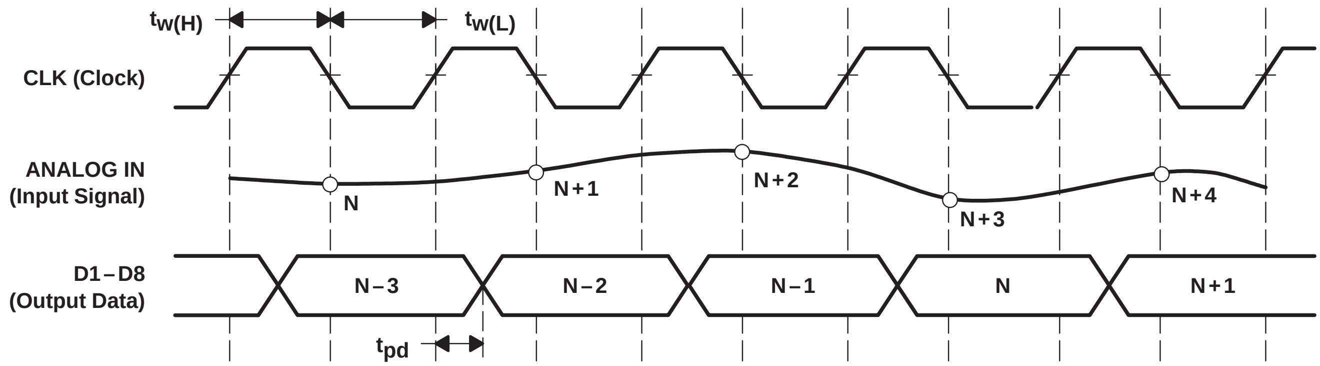


Figure 1. I/O Timing Diagram

TYPICAL CHARACTERISTICS

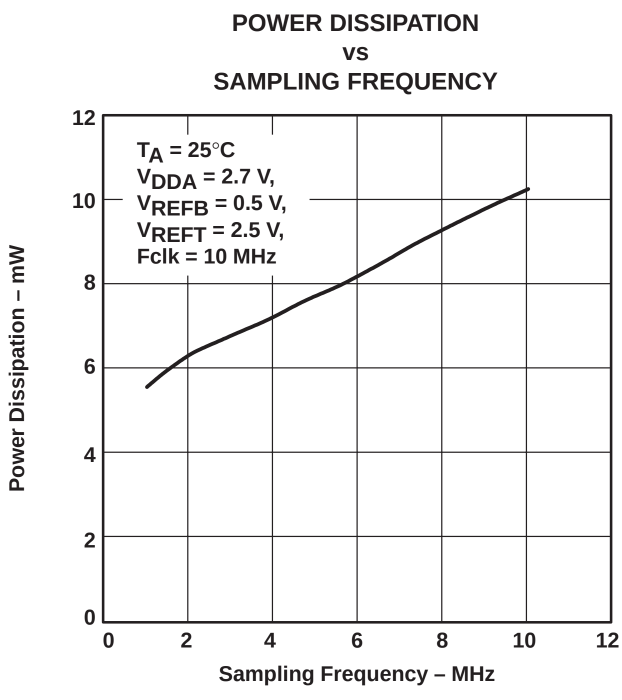


Figure 2

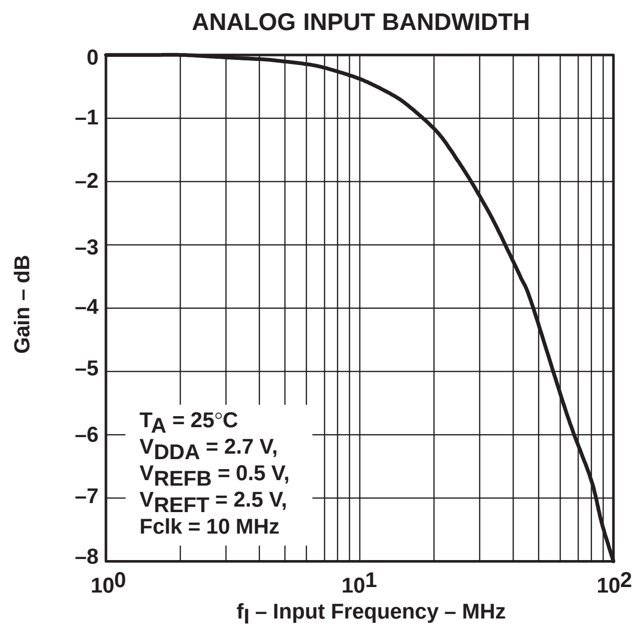


Figure 3

TYPICAL CHARACTERISTICS

SIGNAL-TO-NOISE RATIO
vs
INPUT FREQUENCY

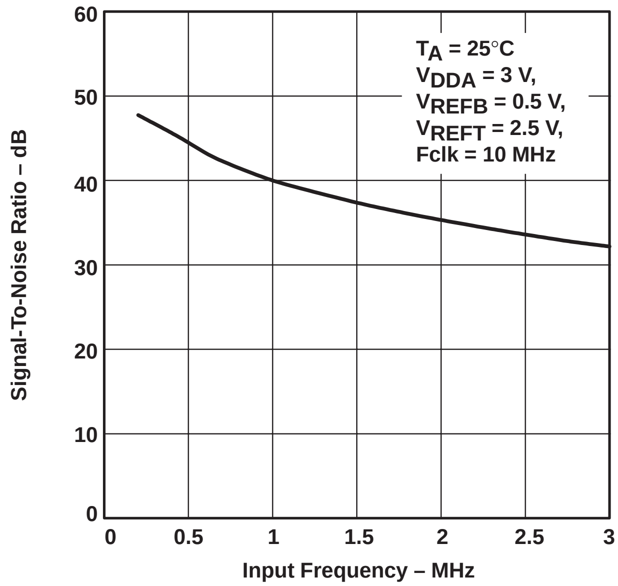


Figure 4

DIFFERENTIAL NONLINEARITY
vs
SAMPLES
(Under Recommended Operating Conditions)

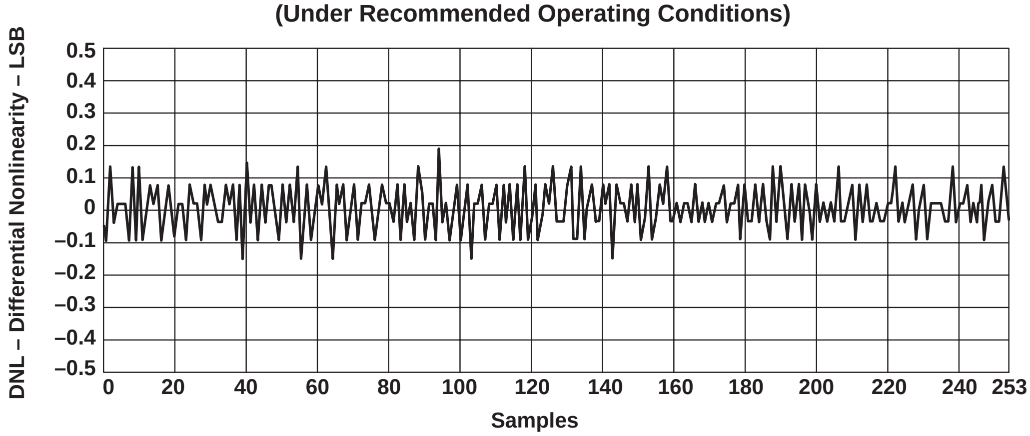


Figure 5

TYPICAL CHARACTERISTICS

EFFECTIVE NUMBER OF BITS
vs
TEMPERATURE

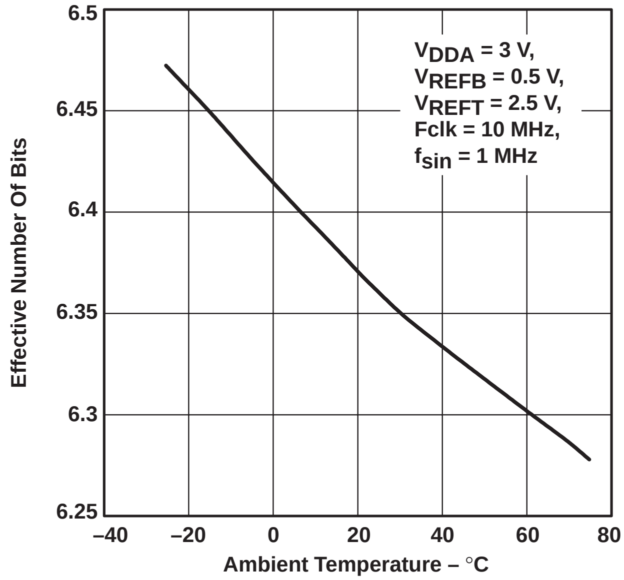


Figure 6

INTEGRAL NONLINEARITY
vs
SAMPLES
(Under Recommended Operating Conditions)

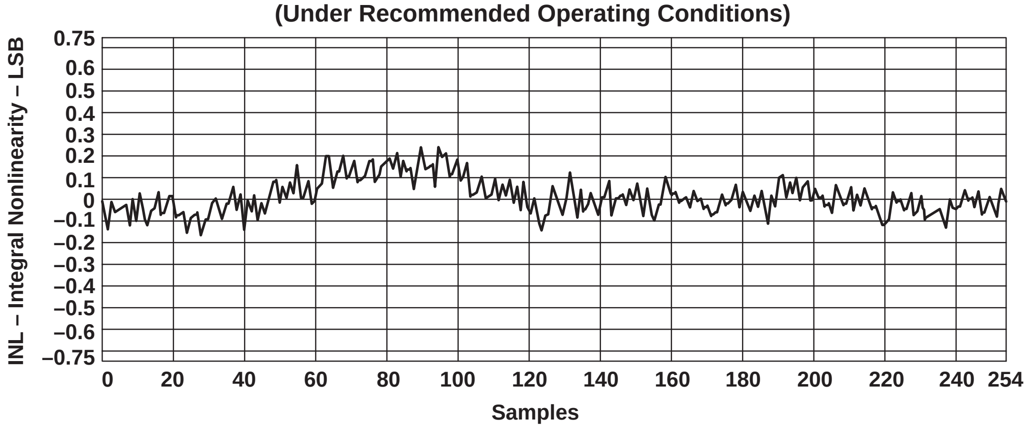


Figure 7

TYPICAL CHARACTERISTICS

FAST FOURIER TRANSFORMER vs FREQUENCY (Under Recommended Operating Conditions)

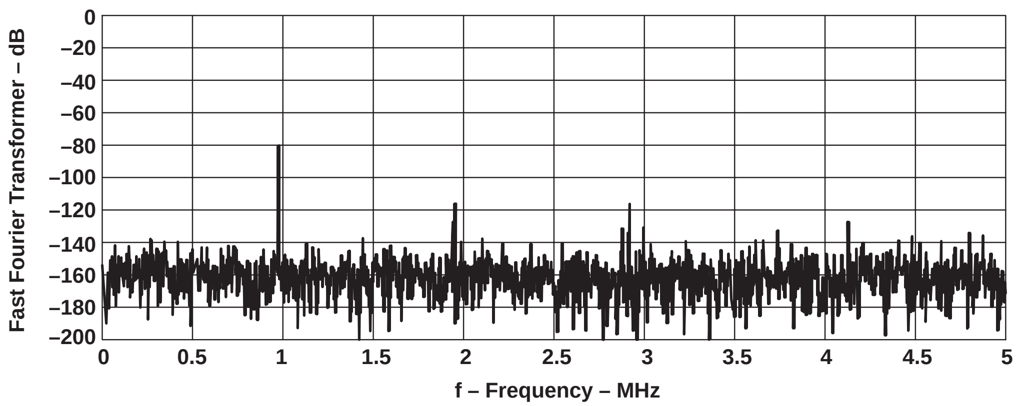


Figure 8

INTEGRAL LINEARITY ERROR vs FREQUENCY

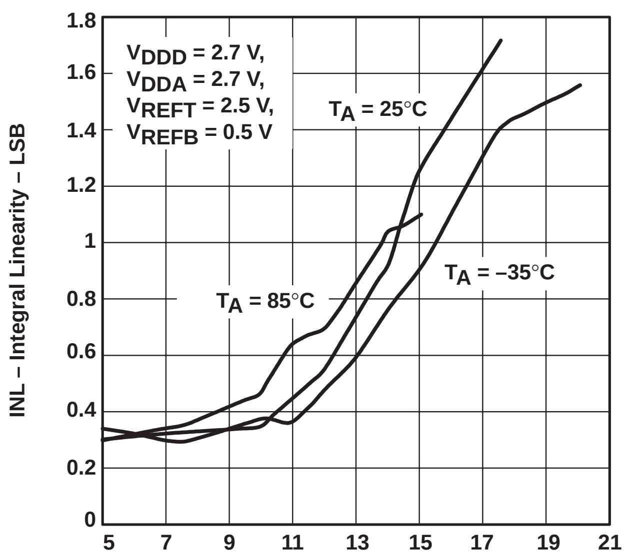


Figure 9

DIFFERENTIAL LINEARITY ERROR vs FREQUENCY

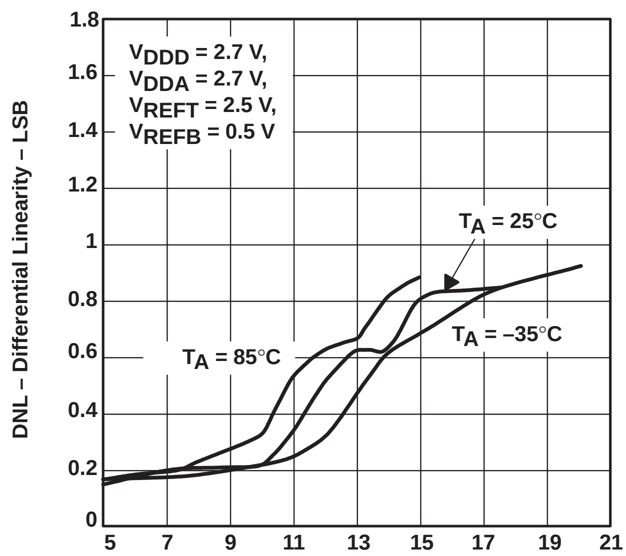


Figure 10

TYPICAL CHARACTERISTICS

INTEGRAL LINEARITY ERROR
vs
FREQUENCY

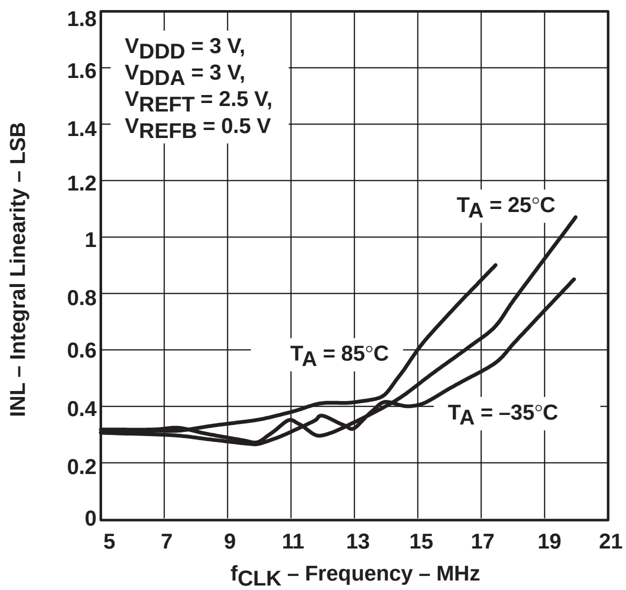


Figure 11

DIFFERENTIAL LINEARITY ERROR
vs
FREQUENCY

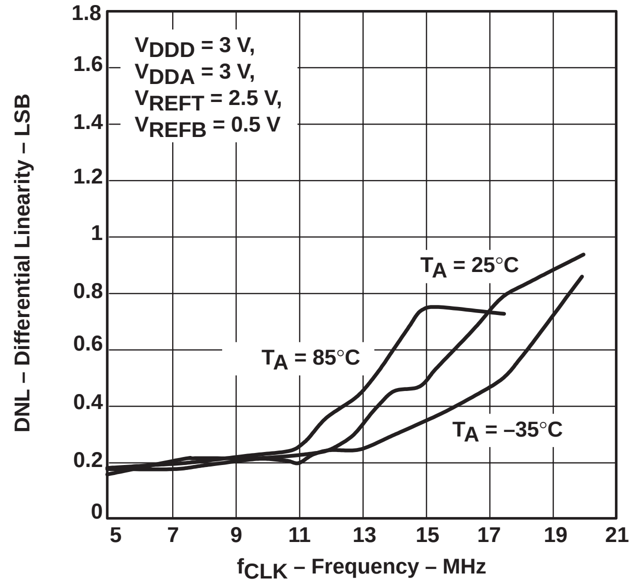


Figure 12

INTEGRAL LINEARITY ERROR
vs
FREQUENCY

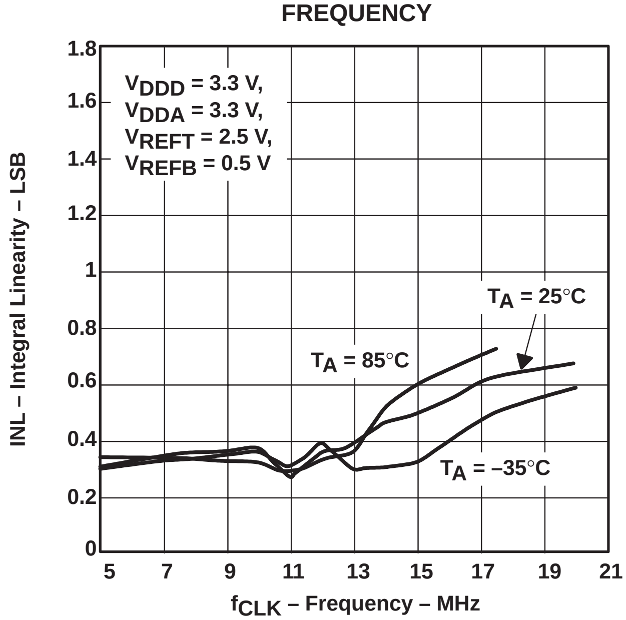


Figure 13

DIFFERENTIAL LINEARITY ERROR
vs
FREQUENCY

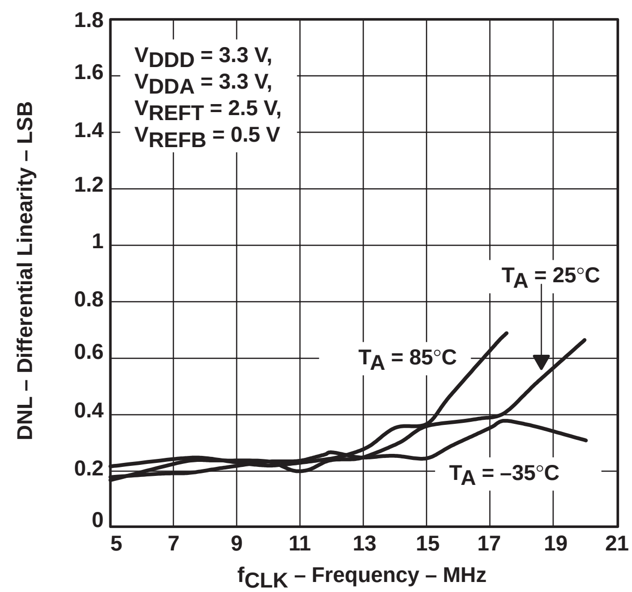


Figure 14

TYPICAL CHARACTERISTICS

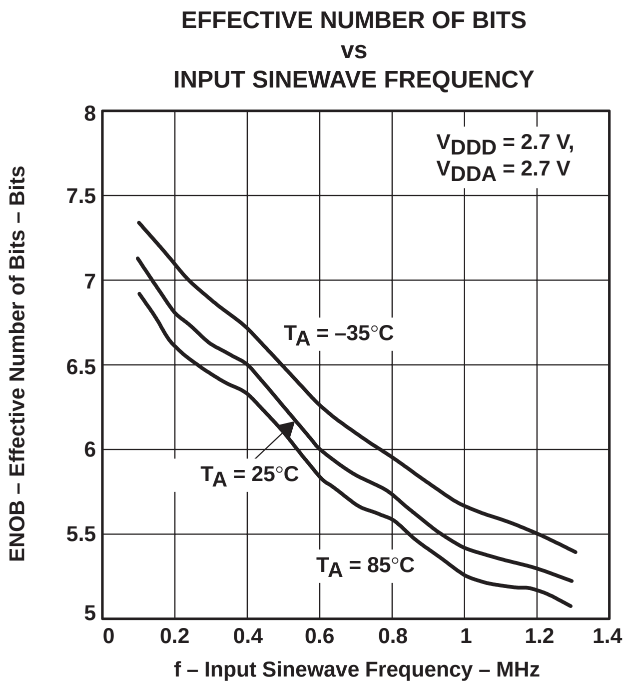


Figure 15

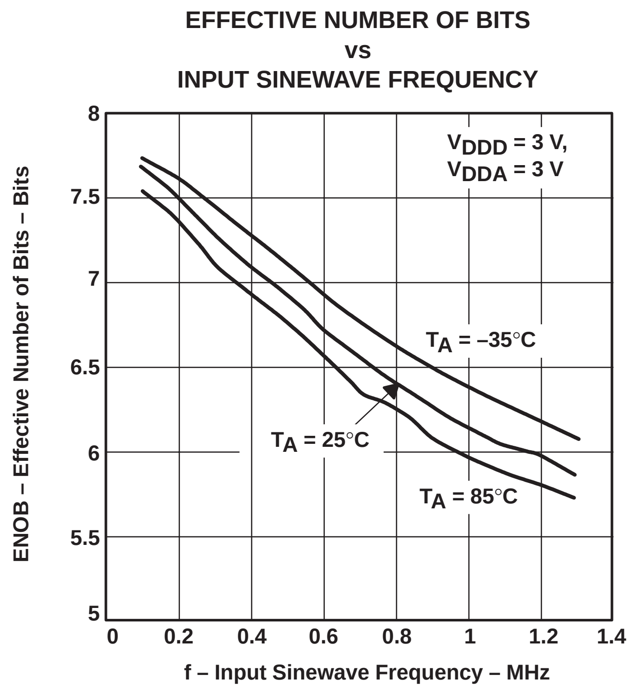


Figure 16

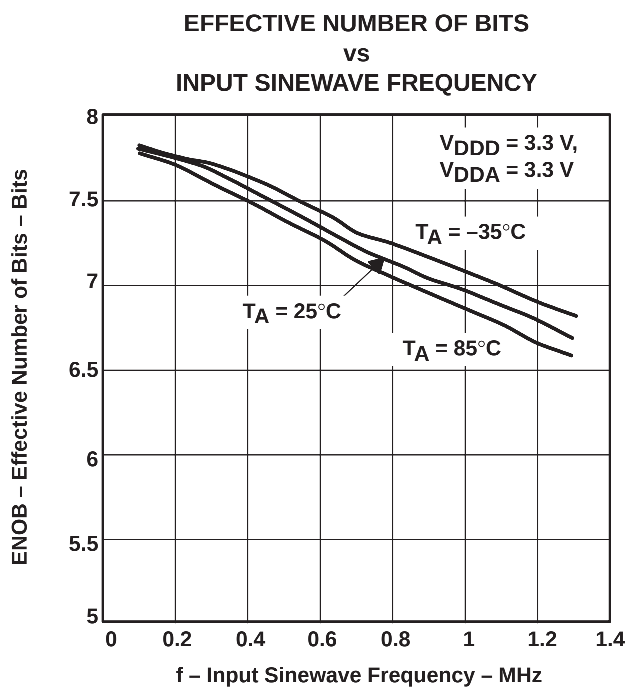


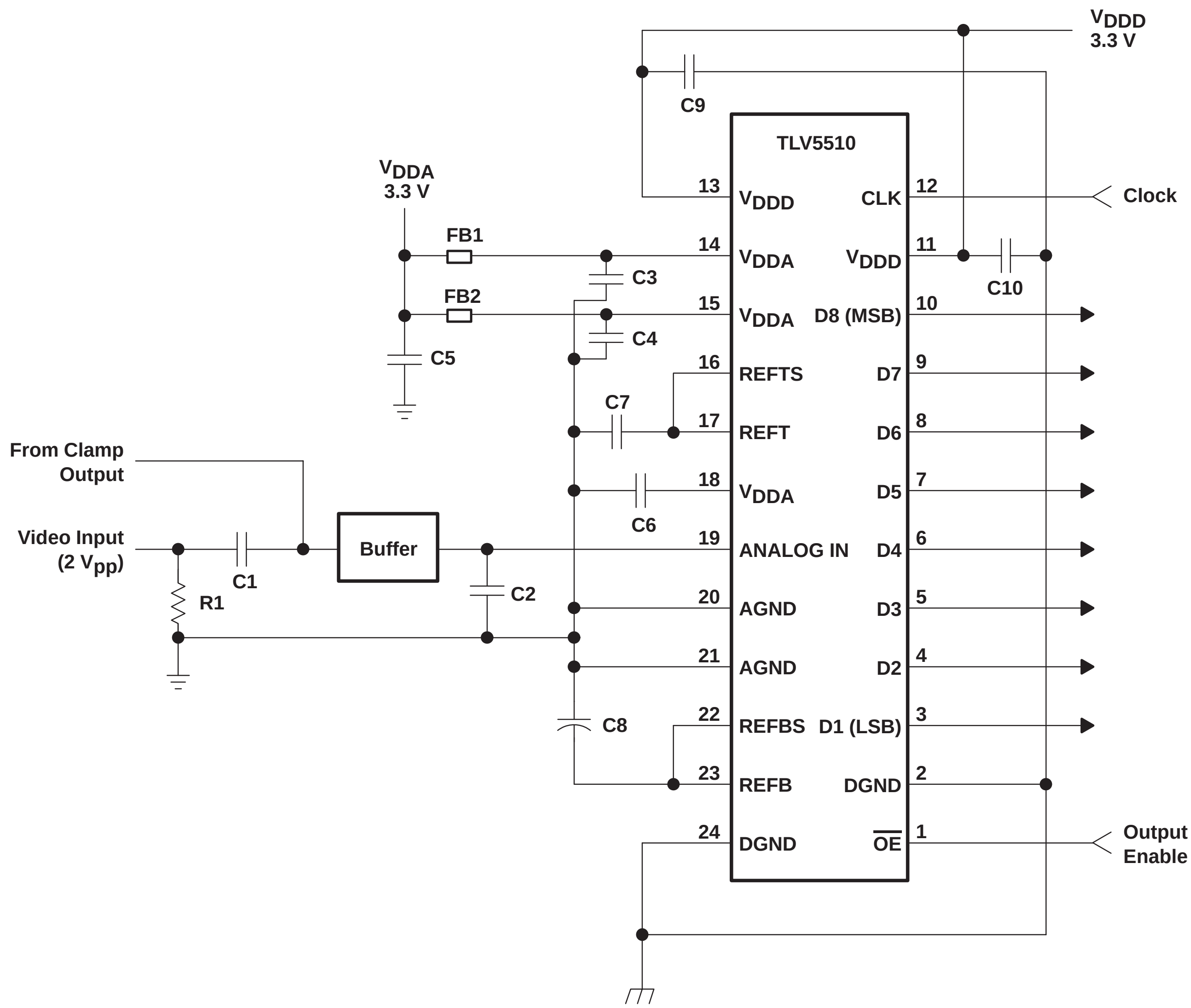
Figure 17

APPLICATION INFORMATION

The following notes are design recommendations that should be used with the TLV5510.

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or printed-circuit-board (PCB) techniques should be used throughout the evaluation and production process. Breadboards should be copper clad for bench evaluation.
- Since AGND and DGND are connected internally, the ground lead in must be kept as noise free as possible. A good method to use is twisted-pair cables for the supply lines to minimize noise pickup. An analog and digital ground plane should be used on PCB layouts when additional logic devices are used. The AGND and DGND terminals of the device should be tied to the analog ground plane.
- V_{DDA} to AGND and V_{DDD} to DGND should be decoupled with 1-µF and 0.01-µF capacitors, respectively, placed as close as possible to the appropriate device terminals. A ceramic chip capacitor is recommended for the 0.01-µF capacitor. Care should be exercised to assure a solid noise-free ground connection for the analog and digital grounds.
- V_{DDA}, AGND, and ANALOG IN terminals should be shielded from the higher frequency terminals, CLK and D0–D7. If possible, AGND traces should be placed on both sides of the ANALOG IN traces on the PCB for shielding.
- In testing or application of the device, the resistance of the driving source connected to the analog input should be 10 Ω or less within the analog frequency range of interest.

APPLICATION INFORMATION



LOCATION	DESCRIPTION
C1, C3, C4, C6 – C10	0.1 µF Capacitor
C2	10 pF Capacitor
C5	47 µF Capacitor
FB1, FB2	Ferrite bead
R1	75 Ω Resistor

Figure 18. Application and Test Schematic

PRINCIPLES OF OPERATION

functional description

The TLV5510 is a semiflash ADC featuring two lower comparator blocks of four bits each.

As shown in Figure 19, input voltage $V_I(1)$ is sampled with the falling edge of CLK1 to the upper comparators block and the lower comparators block(A), S(1). The upper comparators block finalizes the upper data UD(1) with the rising edge of CLK2, and simultaneously, the lower reference voltage generates the voltage RV(1) corresponding to the upper data. The lower comparators block (A) finalizes the lower data LD(1) with the rising edge of CLK3. UD(1) and LD(1) are combined and output as OUT(1) with the rising edge of CLK4. According to the above internal operation described, output data is delayed 2.5 clocks from the analog input voltage sampling point.

Input voltage $V_I(2)$ is sampled with the falling edge of CLK2. UD(2) is finalized with the rising edge of CLK3, and LD(2) is finalized with the rising edge of CLK4 at the lower comparators block(B). OUT(2) is output with the rising edge of CLK5.

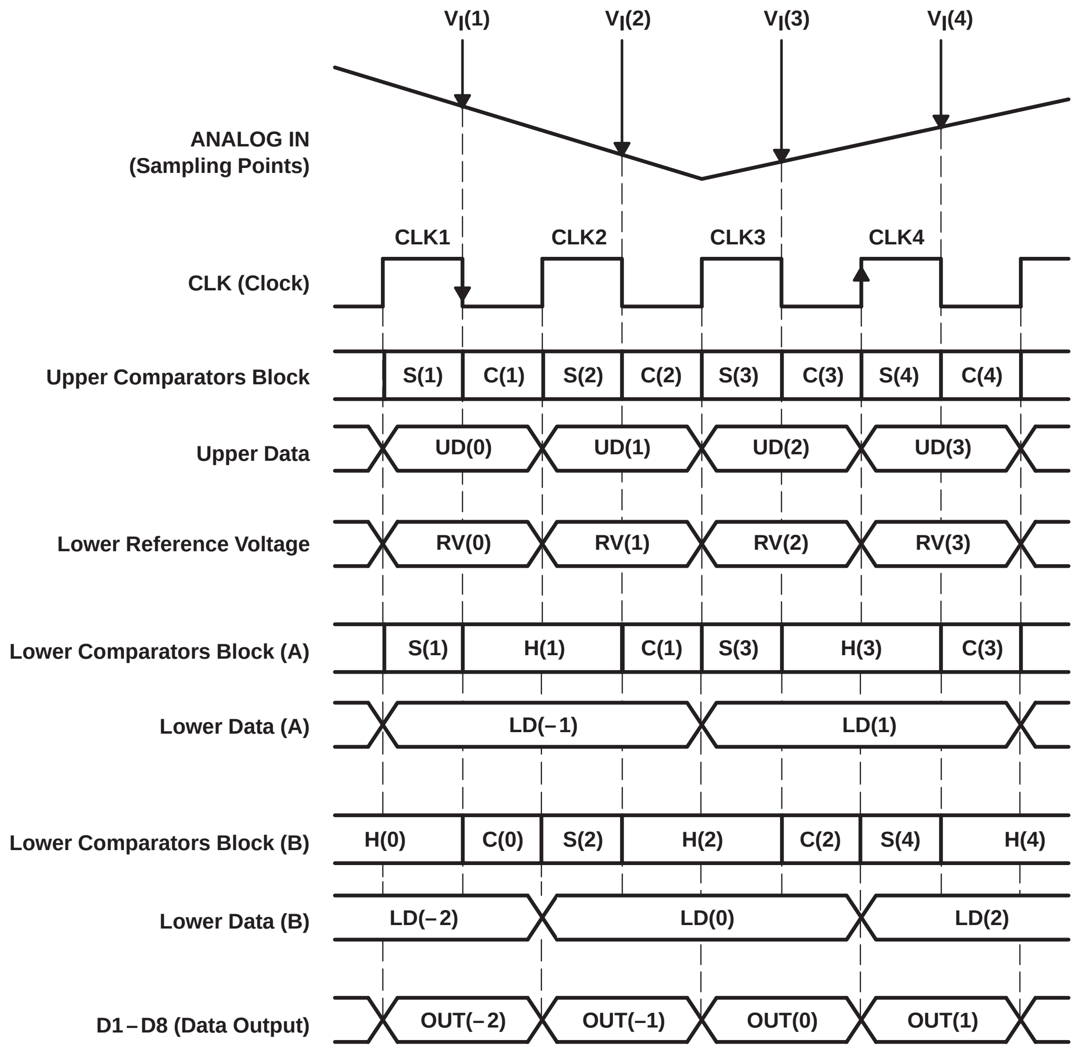


Figure 19. Internal Functional Timing Diagram

PRINCIPLES OF OPERATION

functional description (continued)

The MSB comparator block converts on the falling edge of each applied clock cycle. The LSB comparator blocks CB-A and CB-B convert on the falling edges of the first and second following clock cycles, respectively. The timing diagram of the conversion algorithm is shown in Figure 19.

analog input operation

The analog input stage to the TLV5510 is a chopper-stabilized comparator and is equivalently shown below:

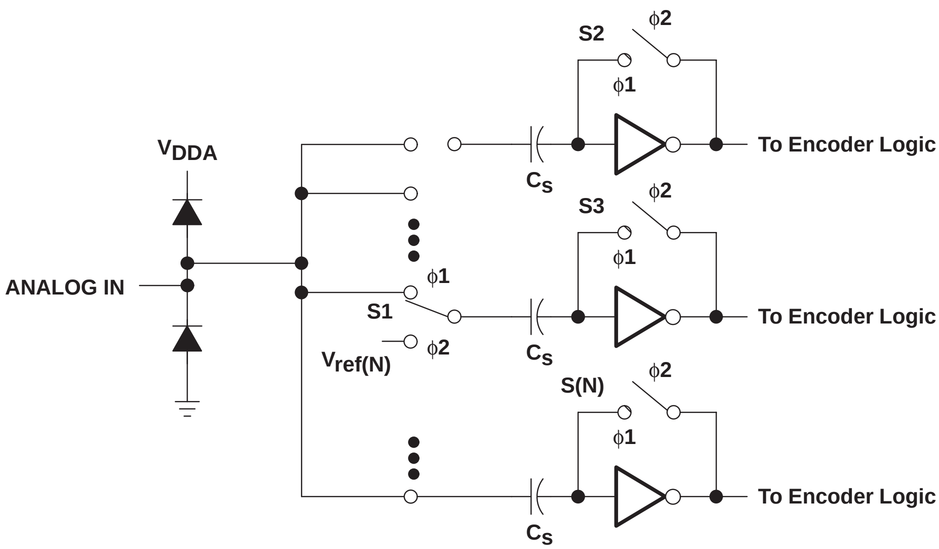


Figure 20. External Connections for Using the Internal Reference Resistor Divider

Figure 20 depicts the analog input for the TLV5510. The switches shown are controlled by two internal clocks, ϕ1 and ϕ2. These are nonoverlapping clocks that are generated from the CLK input. During the sampling period, ϕ1, S1 is closed and the input signal is applied to one side of the sampling capacitor, C_S. Also during the sampling period, S2 through S(N) are closed. This sets the comparator input to approximately 2.5 V. The delta voltage is developed across C_S. During the comparison phase, ϕ2, S1 is switched to the appropriate reference voltage for the bit value N, i.e., $V_{ref(N)}$. S2 is opened and $V_{ref(N)} – VC_S$ toggles the comparator output to the appropriate digital 1 or 0. The small resistance values for the switch, S1, and small value of the sampling capacitor combine to produce the wide analog input bandwidth of the TLV5510. The source impedance driving the analog input of the TLV5510 should be less than 100 Ω across the range of input frequency spectrum.

reference inputs – REFB, REFT, REFBS, REFTS

The range of analog inputs that can be converted are determined by REFB and REFT, REFT being the maximum reference voltage and REFB being the minimum reference voltage. The TLV5510 is tested with REFT = 2.5 V or 2 V and REFB = 0.5 V or 0 V producing a 2-V full-scale range. The TLV5510 can operate with REFT – REFB = 2.4 V, but the power dissipation in the reference resistor increases significantly (49 mW at 3.3 V nominally). It is recommended that a 0.1 µF capacitor be attached to REFB and REFT whether using externally or internally generated voltages.

PRINCIPLES OF OPERATION

internal reference voltage conversion

Three internal resistors allow the device to generate an internal reference voltage. These resistors are brought out on terminals V_{DDA}, REFTS, REFT, REFB, REFBS, and AGND. Two different bias voltages are possible without the use of external resistors.

The internal resistors are provided to develop REFT and REFB as listed in Table 1 (bias option 1) with only two external connections. This is developed with a 3-resistor network connected to V_{DDA}. When using this feature, connect REFT to REFTS and connect REFB to REFBS. For applications where the variance associated with V_{DDA} is acceptable, this internal voltage reference saves space and cost (see Figure 21).

A second internal bias option (bias two option) is shown in Figure 22. Using this scheme REFB = AGND and REFT is as shown in Table 1 (bias option 2). These bias voltage options can be used to provide the values listed in the following table.

Table 1. Bias Voltage Options for Different V_{DDA}

BIAS OPTION	V_{DDA}	BIAS VOLTAGE		
		V_{REFB}	V_{REFT}	$V_{REFT} - V_{REFB}$
1	2.7 V	0.54	2.34	1.8
	3 V	0.6	2.60	2
	3.3 V	0.66	2.86	2.2
	3.6 V	0.72	3.12	2.4
2	2.7 V	AGND	2.25	2.25
	3 V	AGND	2.5	2.5
	3.3 V	AGND	2.75	2.75
	3.6 V	AGND	3	3

To use the internally-generated reference voltage, terminal connections should be made as shown in Figure 21 or Figure 22.

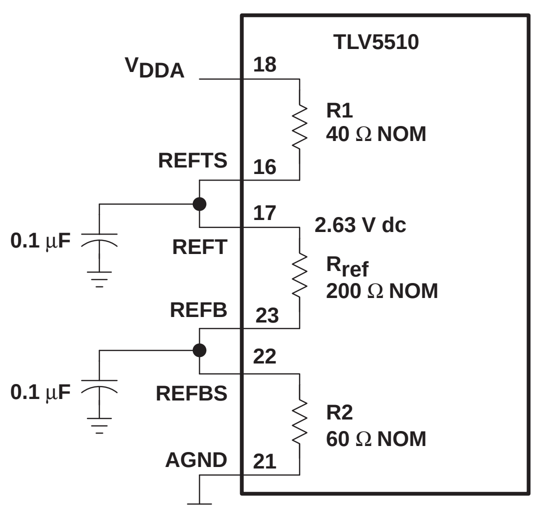


Figure 21. External Connections Using the Internal Bias One Option

PRINCIPLES OF OPERATION

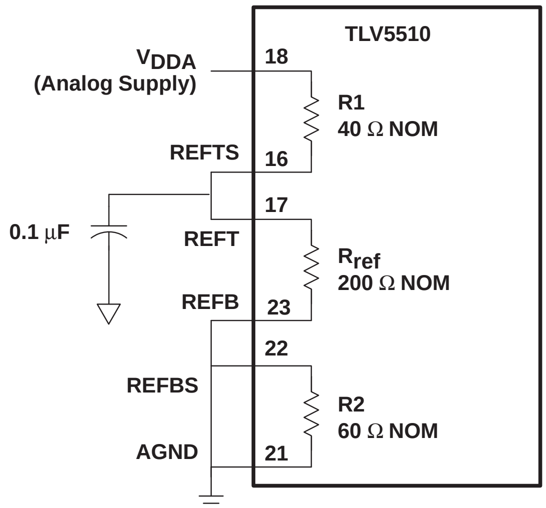


Figure 22. External Connections for Using the Internal Reference Resistor Divider

functional operation

The TLV5510 functions as shown in the Table 2.

Table 2. Functional Operation

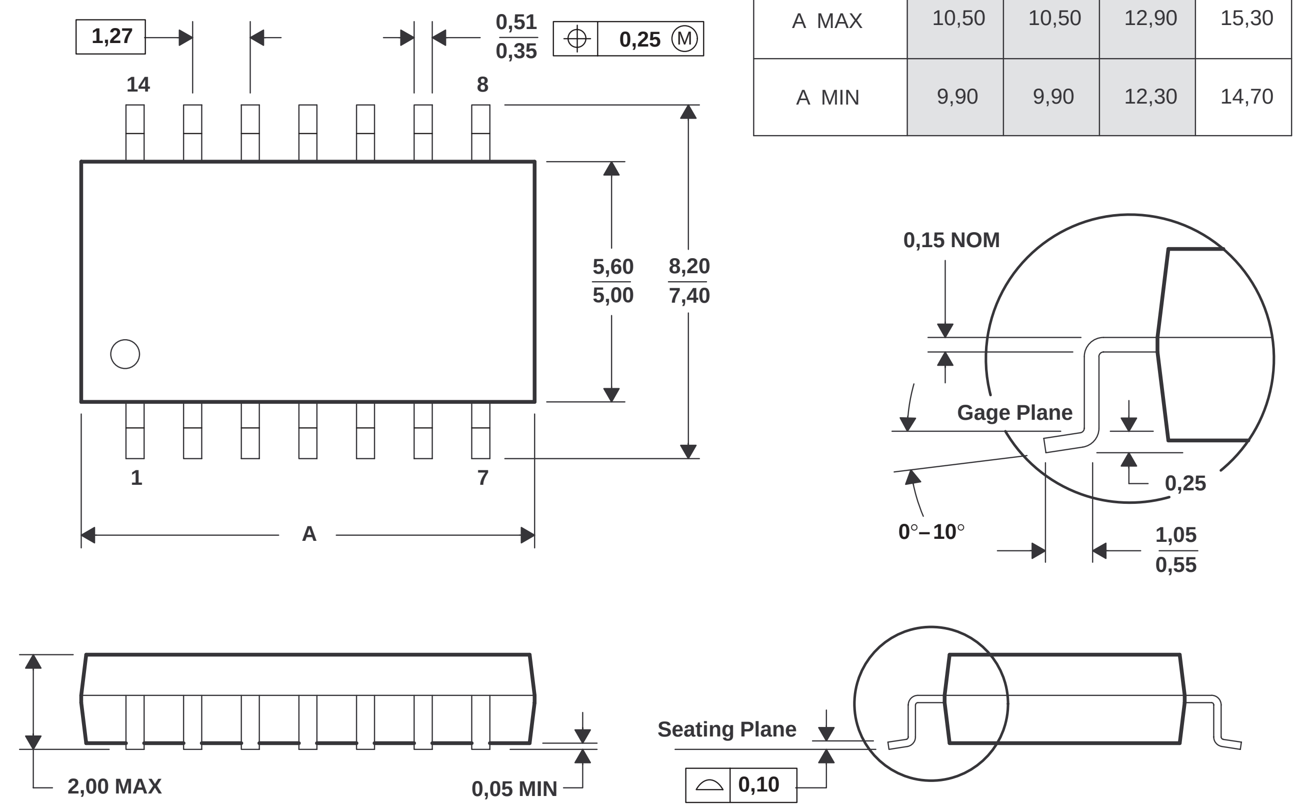
INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE MSB							LSB
REFT	255	1	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	128	1	0	0	0	0	0	0	0
•	127	0	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
REFB	0	0	0	0	0	0	0	0	0

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70



4040062/B 2/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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