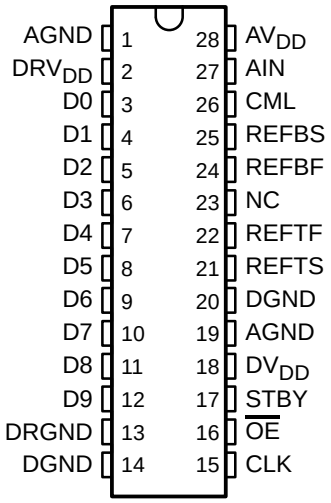
- **10-Bit Resolution 20 MSPS Sampling Analog-to-Digital Converter (ADC)**
- **Power Dissipation . . . 107 mW Typ**
- **5-V Single Supply Operation**
- **Differential Nonlinearity . . . ±0.5 LSB Typ**
- **No Missing Codes**
- **Power Down (Standby) Mode**
- **Three State Outputs**
- **Digital I/Os Compatible With 5-V or 3.3-V Logic**
- **Adjustable Reference Input**
- **Small Outline Package (SOIC), Super Small Outline Package (SSOP), or Thin Small Outline Package (TSOP)**
- **Pin Compatible With the Analog Devices AD876**

DB, DW, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

applications

- **Communications**
- **Multimedia**
- **Digital Video Systems**
- **High-Speed DSP Front-End . . . TMS320C6x**

description

The TLC876 is a CMOS, low-power, 10-bit, 20 MSPS analog-to-digital converter (ADC). The speed, resolution, and single-supply operation are suited for applications in video, multimedia, imaging, high-speed acquisition, and communications. The low-power and single-supply operation satisfy requirements for high-speed portable applications. The speed and resolution ideally suit charge-coupled device (CCD) input systems such as color scanners, digital copiers, electronic still cameras, and camcorders. A multistage pipelined architecture with output error correction logic provides for no missing codes over the full operating temperature range. Force and sense connections to the reference inputs provide a more accurate internal reference voltage to the reference resistor string.

A standby mode of operation reduces the power to typically 15 mW. The digital I/O interfaces to either 5-V or 3.3-V logic and the digital output terminals can be placed in a high-impedance state. The format of the output data is straight binary coding.

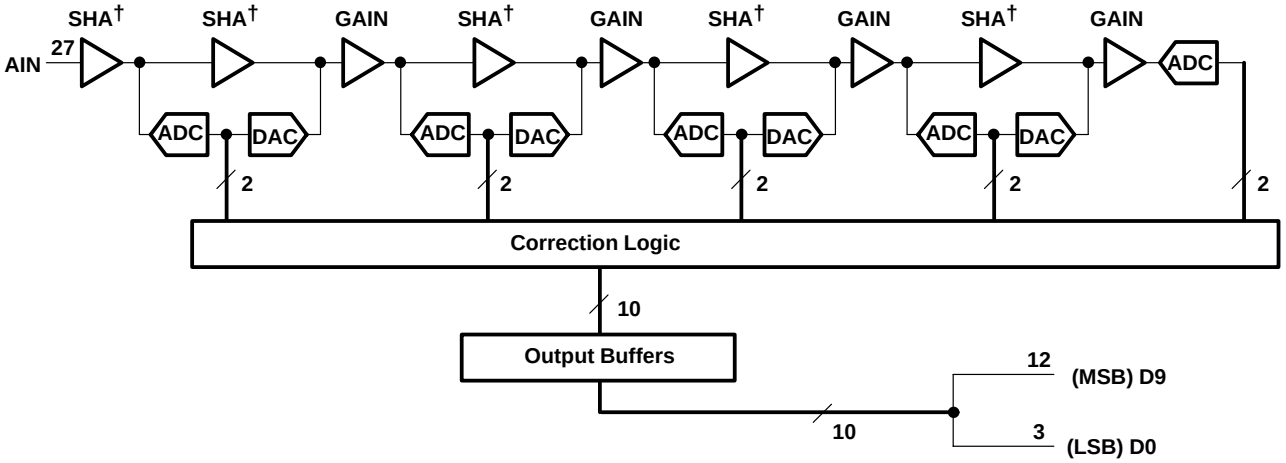
A pipelined multistaged architecture achieves a high sample rate with low power consumption. The TLC876 distributes the conversion over several smaller ADC sub-blocks, refining the conversion with progressively higher accuracy as the device passes the results from stage to stage. This distributed conversion requires a small fraction of the 1023 comparators used in a traditional flash ADC. A sample-and-hold amplifier (SHA) within each of the stages permits the first stage to operate on a new input sample while the second through the fifth stages operate on the four preceding samples.

The TLC876C is characterized for operation from 0°C to 70°C, and the TLC876I is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGE		
	SUPER SMALL OUTLINE (DB)	SMALL OUTLINE (DW)	TSSOP (PW)
0°C to 70°C	TLC876CDB	TLC876CDW	TLC876CPW
–40°C to 85°C	TLC876IDB	TLC876IDW	TLC876IPW

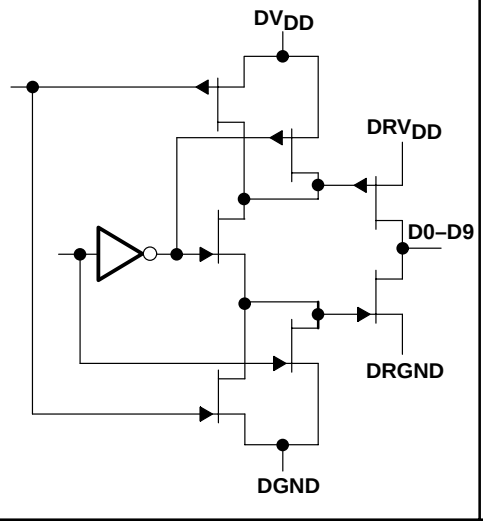
functional block diagram



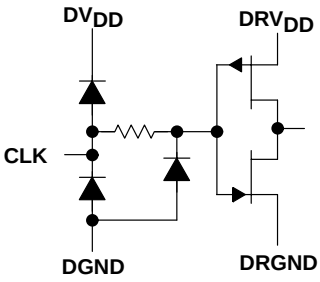
† Sample and hold amplifier

equivalent input and output circuits

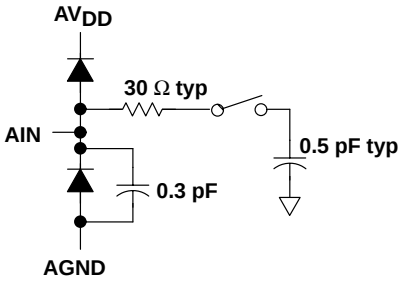
D0–D9 OUTPUT CIRCUIT



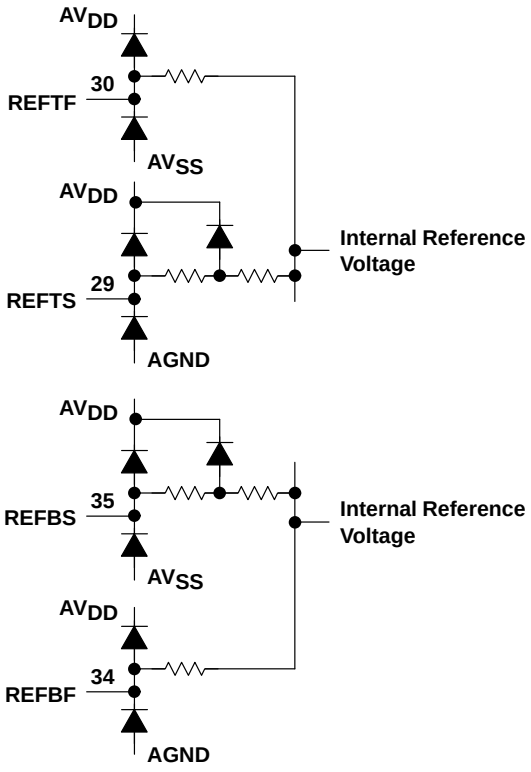
ALL DIGITAL INPUT CIRCUITS



AIN INPUT CIRCUIT



REFERENCE INPUT CIRCUIT



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	1, 19		Analog ground
AIN	27	I	Analog input
AV_{DD}	28		5-V analog supply
CLK	15	I	Clock input
CML	26	O	Bypass for an internal bias point. Typically a 0.1 μF capacitor minimum is connected from this terminal to ground.
DGND	14, 20		Digital ground
DV_{DD}	18		5-V digital supply
DRV_{DD}	2		3.3-V/5-V digital supply. Supply for digital input and output buffers.
DRGND	13		3.3-V/5-V digital ground. Ground for digital input and output buffers.
D0–D9	3–12	O	Digital data out. D0:LSB, D9:MSB
$\overline{OE}$	16	I	Output enable. When $\overline{OE}$ = low or NC, the device is in normal operating mode. When $\overline{OE}$ = high, D0–D9 are high impedance.
REFBF	24	I	Reference bottom force
REFBS	25	I	Reference bottom sense
REFTF	22	I	Reference top force
REFTS	21	I	Reference top sense
STBY	17	I	Standby enable. When STBY = low or NC, the device is in normal operating mode. When STBY = high, the device is in standby mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, AV_{DD} to AGND, DV_{DD} to DGND . . . . . –0.3 V to 6.5 V
Reference voltage input range to AGND, $V_{I(REFTF)}$, $V_{I(REFBF)}$, $V_{I(REFBS)}$, $V_{I(REFTS)}$ . . . . . –0.3 V to AV_{DD} + 0.3 V
Analog input voltage range to AGND . . . . . –0.3 V to AV_{DD} + 0.3 V
Digital input voltage range . . . . . –0.3 V to DV_{DD} + 0.3 V
Digital output voltage range applied from external source . . . . . –0.5 V to DV_{DD}
Operating virtual junction temperature range, T_J . . . . . –40°C to 150°C
Operating free-air temperature range, T_A: TLC876C . . . . . 0°C to 70°C
TLC876I . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

analog and reference inputs

	MIN	NOM	MAX	UNIT
Reference input voltage (top), $V_{I(REFT)}$	$V_{I(REFB)}$ + 1	3.6	4.5	V
Reference input voltage (bottom), $V_{I(REFB)}$	0	1.6	$V_{I(REFT)}$ – 1	V
Analog input voltage, $V_{I(AIN)}$	1	2		V_{pp}

power supply

		MIN	NOM	MAX	UNIT
Supply voltage	AV_{DD} ‡	4.5		5.25	V
	DV_{DD}‡	4.5		5.25	
	DRV_{DD}	3		5.25	

‡ The voltage difference between AV_{DD} and DV_{DD} terminals cannot exceed 0.5 V to maintain performance specifications.

digital inputs

		MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	DRV_{DD} = 3 V	2.4			V
	DRV_{DD} = 5 V	4			
	DRV_{DD} = 5.25 V	4.2			
Low-level input voltage, V_{IL}	DRV_{DD} = 3 V			0.6	V
	DRV_{DD} = 5 V			1	
	DRV_{DD} = 5.25 V			1.05	
Clock period, t_c (see Figure 1)			50		ns
Pulse duration, clock high, $t_{w(CLKH)}$		23	25		ns
Pulse duration, clock low, $t_{w(CLKL)}$		23	25		ns
Operating free-air temperature, T_A	TLC876C	0		70	°C
	TLC876I	–40		85	°C

electrical characteristics at AV_{DD} = DV_{DD} = 5 V, DRV_{DD} = 3.3 V, $V_{I(REFT)}$ = 3.6 V, $V_{I(REFB)}$ = 1.6 V, f_{CLK} = 20 MSPS (unless otherwise noted)

power supply

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Operating supply current	AV_{DD}†				17	25	mA
		DV_{DD}†				2.7	5	mA
		DRV_{DD}				25	100	µA
P_D	Power dissipation					107	150	mW
$P_{D(STBY)}$	Standby power		STBY = High	CLK running		45	85	mW
				CLK inhibited at V_{DD} or 0 V		15	35	

† The voltage difference between AV_{DD} and DV_{DD} terminals cannot exceed 0.5 V to maintain performance specifications.

digital logic inputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	DV_{DD} = 5 V	–10		10	µA
I_{IL}	Low-level input current	DV_{DD} = 5V	–50		50	
$I_{IL(CLK)}$	Low-level input current, CLK	DV_{DD} = 5V	–10		10	µA
C_i	Input capacitance			5		pF

logic outputs

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 50 µA	DRV_{DD} = 3 V	2.4			V
			DRV_{DD} = 5 V	3.8			
		I_{OH} = 0.5 mA	DRV_{DD} = 5 V	2.4			
V_{OL}	Low-level output voltage	I_{OL} = 50 µA	DRV_{DD} = 3.6 V			0.7	V
			DRV_{DD} = 5.25 V			1.05	
		I_{OL} = 0.6 mA	DRV_{DD} = 5.25 V			0.4	
C_o	Output capacitance				5		pF
I_{OZ}	High-impedance-state output current			–10		10	µA

dc accuracy

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Integral nonlinearity (INL)			±1.5		LSB
Differential nonlinearity (DNL) (see Note 1)			±0.5	<±1	
Offset error			–0.4		%FSR
Gain error			0.2		%FSR

NOTE 1: A differential nonlinearity error of less than ±1 LSB ensures no missing codes.

analog input

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i Input capacitance			5		pF

reference input

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ref} Reference input resistance		350	500	750	Ω
I_{ref} Reference input current			4		mA
Reference top offset voltage			35		mV
Reference bottom offset voltage			35		mV

operating characteristics at AV_{DD} = DV_{DD} = 5 V, DRV_{DD} = 3.3 V, $V_{I(REFT)}$ = 3.6 V, $V_{I(REFB)}$ = 1.6 V, f_{CLK} = 20 MSPS (unless otherwise noted)

dynamic performance†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Effective number of bits (ENOB)	f_I = 1 MHz		8.5		Bits
		f_I = 3.58 MHz	8	8.5		
		f_I = 10 MHz		8.1		
	Signal-to-total harmonic distortion+noise (S/(THD+N))	f_I = 1 MHz		53		dB
		f_I = 3.58 MHz	50	53		
		f_I = 10 MHz		51		
	Total harmonic distortion (THD)	f_I = 1 MHz		–63		dB
		f_I = 3.58 MHz		–62	–56	
		f_I = 10 MHz		–61		
	Spurious free dynamic range	f_I = 3.58 MHz		–64		dB
BW	Analog input full-power bandwidth			200		MHz
	Differential phase			0.5		degrees
	Differential gain			1%		

† The voltage difference between AV_{DD} and DV_{DD} cannot exceed 0.5 V to maintain performance specifications. At input clock rise times less than 20 ns, the offset full-scale error increases approximately by a factor of $(20/t_r)^{0.5}$ where t_r equals the actual rise time in nanoseconds.

timing requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{conv}	Maximum conversion rate (see Note 2)		20			MHz
$t_{d(o)}$	Delay time, output	C_L = 20 pF	5	20		ns
$t_{d(pipe)}$	Delay time, pipeline, latency				3.5	Clock cycles
$t_{d(A)}$	Delay time, aperture			4		ns
	Aperture jitter			22		ps
$t_{dis(DD)}$	Disable time, $\overline{OE}\uparrow$ to Hi-Z	C_L = 20 pF		5	15	ns
$t_{en(HL)}$	Enable time, $\overline{OE}\downarrow$ to valid data			5	15	ns

NOTE 2: The conversion rate can be a minimum of 10 kHz without degradation in specified performance.

PARAMETER MEASUREMENT INFORMATION

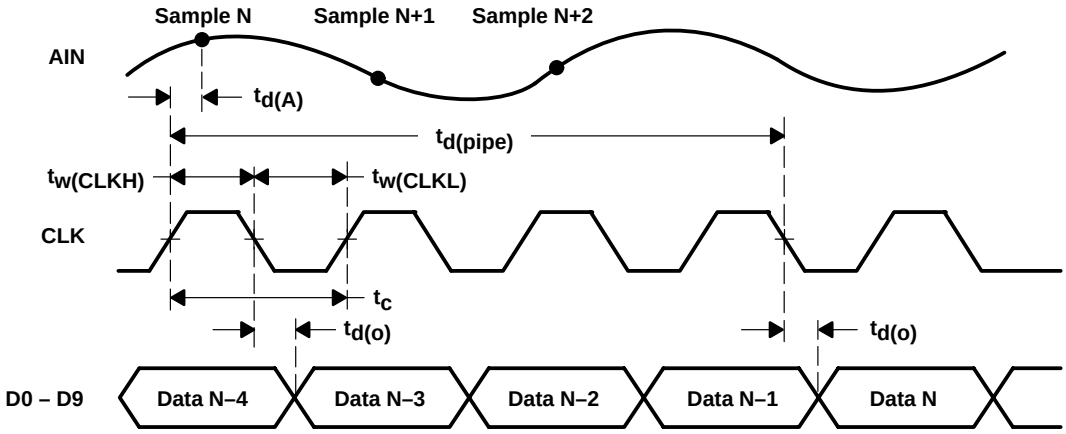


Figure 1. Timing Diagram

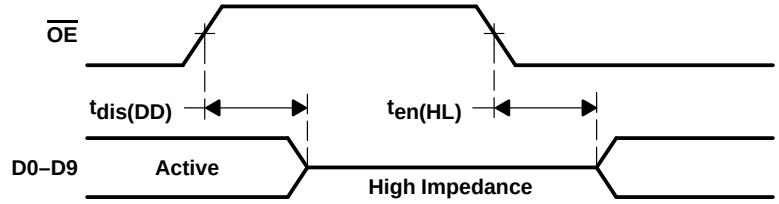


Figure 2. Output Enable to Data Output Timing Diagram

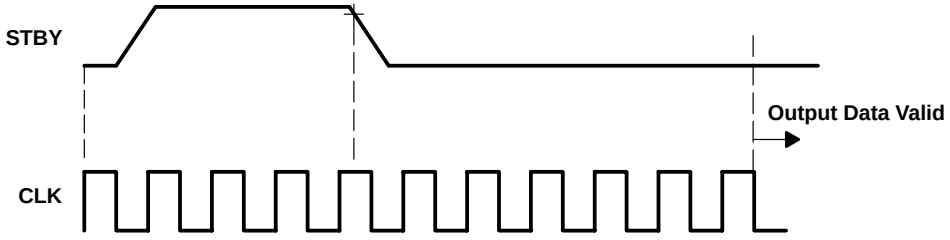


Figure 3. Standby Timing

TYPICAL CHARACTERISTICS

GAIN vs INPUT FREQUENCY

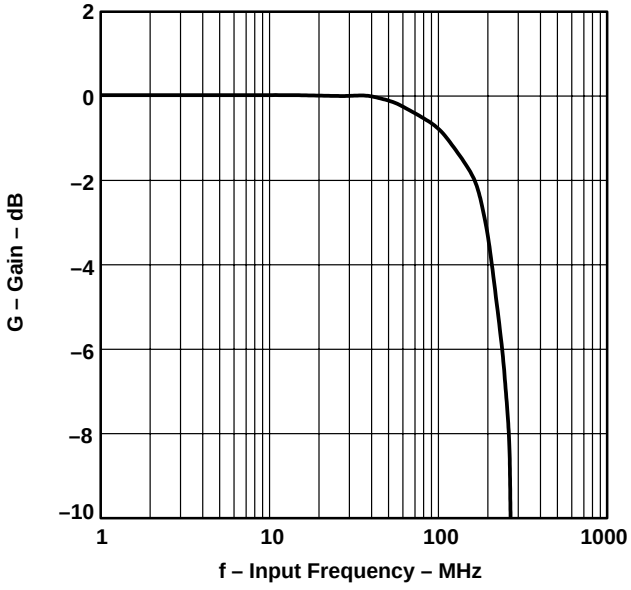


Figure 4

SIGNAL-TO-NOISE AND DISTORTION vs INPUT FREQUENCY

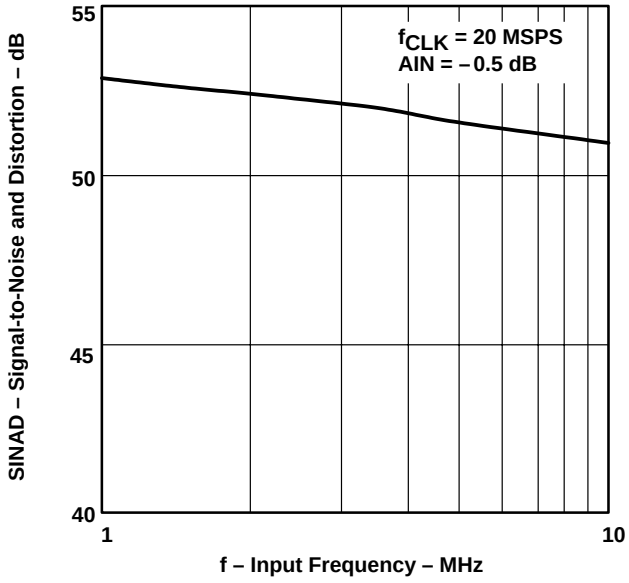


Figure 5

TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

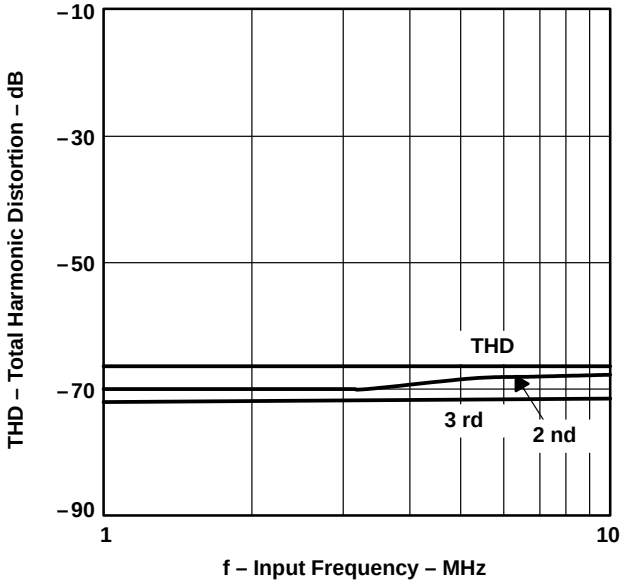


Figure 6

SIGNAL-TO-NOISE AND DISTORTION vs CLOCK FREQUENCY

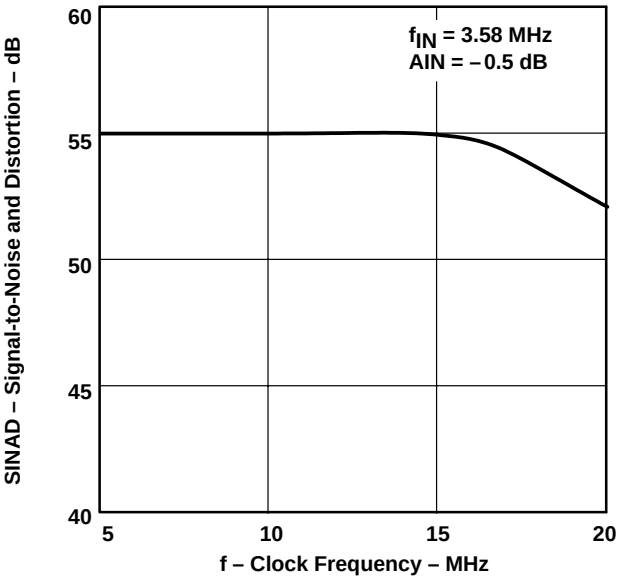


Figure 7

TYPICAL CHARACTERISTICS

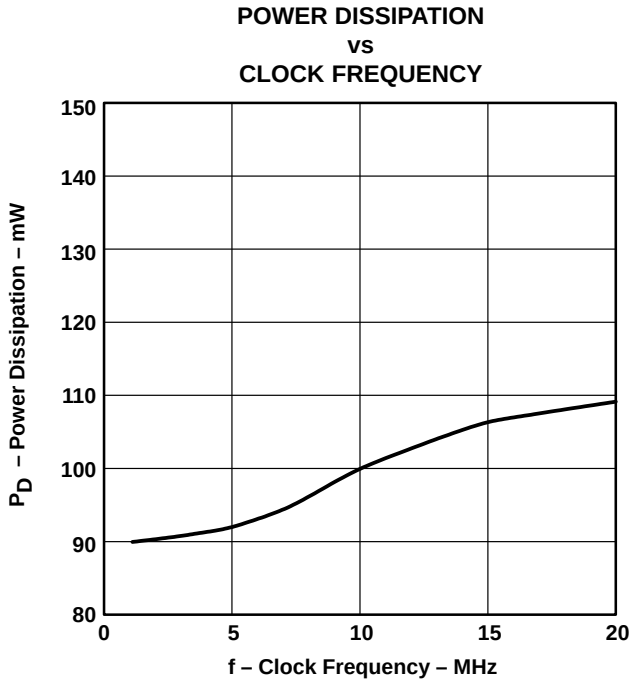


Figure 8

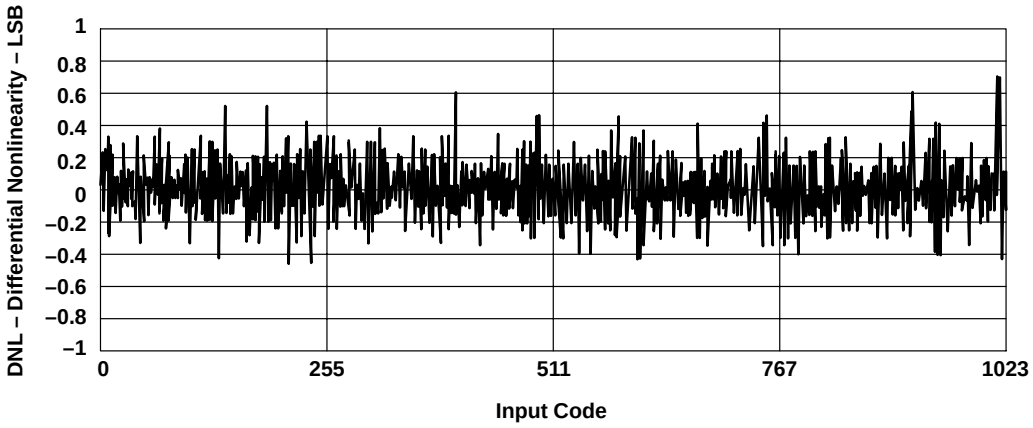


Figure 9. Differential Nonlinearity

TYPICAL CHARACTERISTICS

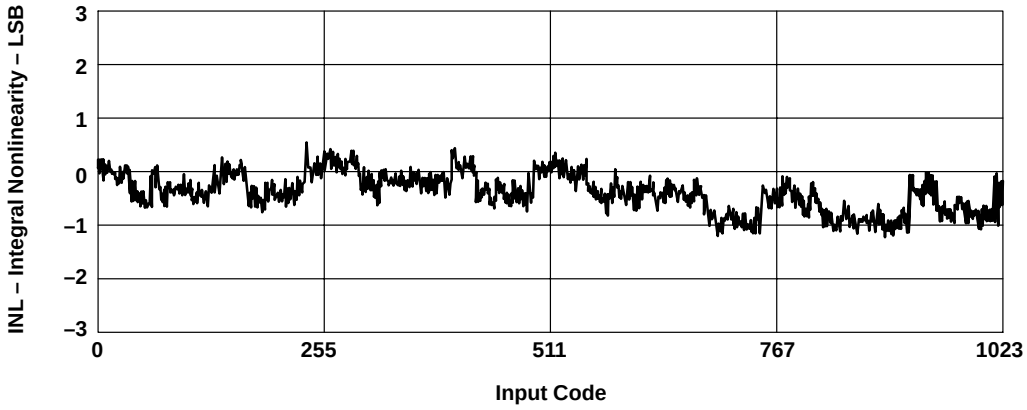


Figure 10. Integral Nonlinearity

SFDR	: –64 dB	4th	: –68 dB
SNRD	: 52 dB	5th	: –71 dB
SNR	: 55 dB	6th	: –71 dB
THD	: –62 dB	7th	: –70 dB
2nd	: –69 dB	8th	: –70 dB
3rd	: –72 dB	9th	: –80 dB

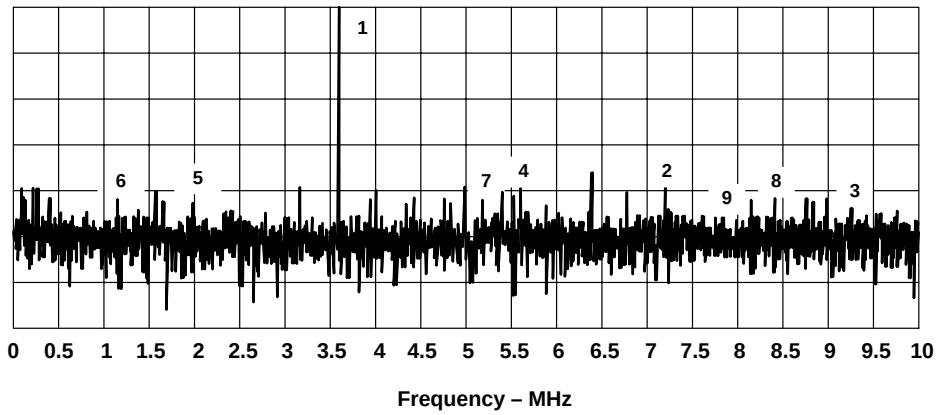


Figure 11. FFT Plot of Dynamic Performance

PRINCIPLES OF OPERATION

definitions of specifications and terminology

integral nonlinearity (INL)

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full-scale point is defined as a level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points. This parameter is sometimes referred to as linearily error.

differential nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ± 1 LSB ensures no missing codes. This parameter is sometimes referred to as differential error.

offset error

The first transition should occur at a level 1/2 LSB above zero. Offset is defined as the deviation of the actual first code transition from that point.

gain error

The first code transition should occur for an analog value 1/2 LSB above nominal negative full scale (the voltage applied to the REFBF terminal). The last transition should occur for an analog value 1 1/2 LSB below nominal positive full scale (the voltage applied to the REFTF terminal). Gain error is the deviation of the actual difference between the first and last code transitions from the ideal difference between the first and last code transitions.

pipeline delay (latency)

The number of clock cycles between conversion initiation on an input sample and the corresponding output data being made available. Once the data pipeline is full, new valid output data are provided every clock cycle.

reference top/bottom offset

Resistance between the reference input and comparator input tap points causes offset errors. These errors can be nulled out by using the force-sense connection as shown in the driving the reference terminals section.

driving the analog input

Figure 12 shows an equivalent input circuit of the TLC876 sample-and-hold amplifier and it represents an excellent first order approximation.

The total equivalent capacitance, C_E, is typically less than 5 pF and the input source must be able to charge or discharge this capacitance to 10-bit accuracy in the sample period of one half of a clock cycle. When the switch S1 closes, the input source must charge or discharge the capacitor C_E from the voltage already stored on C_E (the previously captured sample) to the new voltage. In the worst case, a full-scale voltage step on the input, the input source must provide the charging current through the switch resistance R_{SW} (50 Ω) of S1 and quickly settle (within 1/2 CLK period), and, therefore, the source is driving a low input impedance. However, when the source voltage equals the value previously stored on C_E, the hold capacitor requires no input current to maintain the charge and the equivalent input impedance is extremely high.

Adding series resistance between the output of the source and the AIN terminal reduces the drive requirements placed on the source, as shown in Figure 13. To maintain the frequency performance outlined in the specifications, the resistor should be limited to 200 Ω minus the source resistance or less. The maximum source resistance, R_S, for 10-bit, 1/2 LSB accuracy is given by equation 1.

PRINCIPLES OF OPERATION

driving the analog input (continued)

$$R_S \leq \frac{1}{2f_{(CLK)}\,(C_E \ln 2048)} - R_{SW} \quad (1)$$

For $f_{(CLK)}$ = 20 MHz, C_E = 10 pF, and R_{SW} = 100 Ω, this equation gives 228 Ω as a maximum value; hence the 200 Ω limit on the total source resistance. For applications with an input clock less than 20 MHz, the size of the series resistor can increase proportionally. Alternatively, adding a shunt capacitor between the AIN terminal and analog ground can lower the ac source impedance. This capacitance value depends on the source resistance and the required signal bandwidth.

The input span is determined by the reference voltages (see driving the reference terminals section).

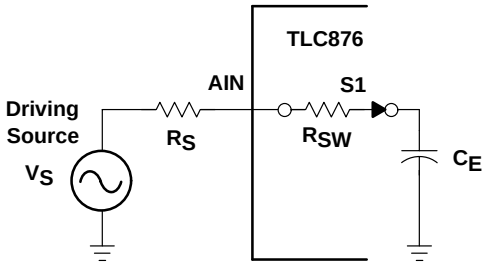


Figure 12. TLC876 Simplified Equivalent Input

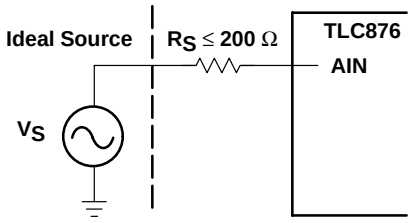


Figure 13. Sample TLC876 Drive Requirements

For many applications, particularly in single supply operation, ac coupling offers a convenient way of biasing the analog input signal at the proper signal range. Figure 14 shows a typical configuration for ac coupling the analog input signal to the TLC876. Maintaining the outlined specifications requires careful selection of the component values. The most important concern is the $f_{-3\ dB}$ high-pass corner that is a function of R2, and the parallel combination of C1 and C2. The $f_{-3\ dB}$ point can be approximated by equation 2.

$$f_{-3\ dB} = \frac{1}{2\pi \times (R2)\,Ceq} \quad (2)$$

where Ceq is the parallel combination of C1 and C2. Since C1 is typically a large electrolytic or tantalum capacitor, the impedance becomes inductive at high frequencies. Adding a small ceramic or polystyrene capacitor, C2 of approximately 0.01 µF, which is not inductive within the frequency range of interest, maintains a low impedance. If the minimum expected input signal frequency is 20 kHz, and R2 equals 1 kΩ and R1 equals 50 Ω, the parallel capacitance of C1 and C2 must be a minimum of 0.008 µF to avoid attenuating signals close to 20 kHz.

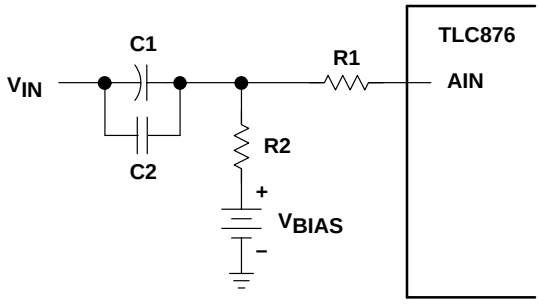


Figure 14. AC-Coupled Inputs

PRINCIPLES OF OPERATION

driving the analog input (continued)

The expanded input circuit shown in Figure 15 aids in understanding the voltage offset generation when using the external input circuit in Figure 14.

The ac coupling capacitors, C1 and C2, integrate the switching transients present at the input of the TLC876 causing a net dc bias current, I_B, to flow into the input. The magnitude of this bias current increases with increasing the dc signal level, V_B, and also increases with sample frequency. When the sample clock frequency is 20 MHz, the dc bias current is approximately 30 μA† at V_{BIAS} equal to 3 V dc. This bias current causes an offset error of (R1 + R2) x I_B at the AIN terminal. Making R2 negligibly small or modifying V_{BIAS} to account for the resultant offset can compensate for this error. Note however that R2 loads the signal driving source and the value must be sufficient for the application.

For example, as shown in Figure 15, when V_{BIAS} is 3 V and the resistor values stated above, the bias current causes a 31.5 mV‡ offset from the 3 V bias, V_{BIAS}, at the AIN terminal. For the TLC876, V_{BIAS} can be as low as 1 V for a 2 V peak-to-peak input signal swing.

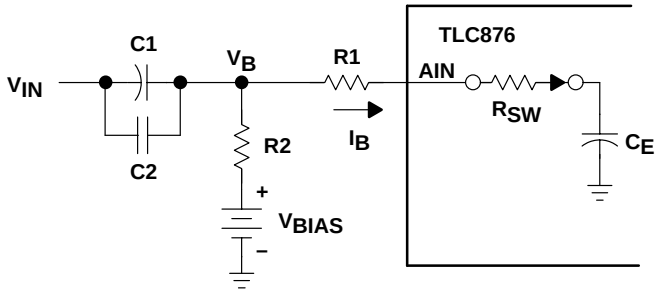


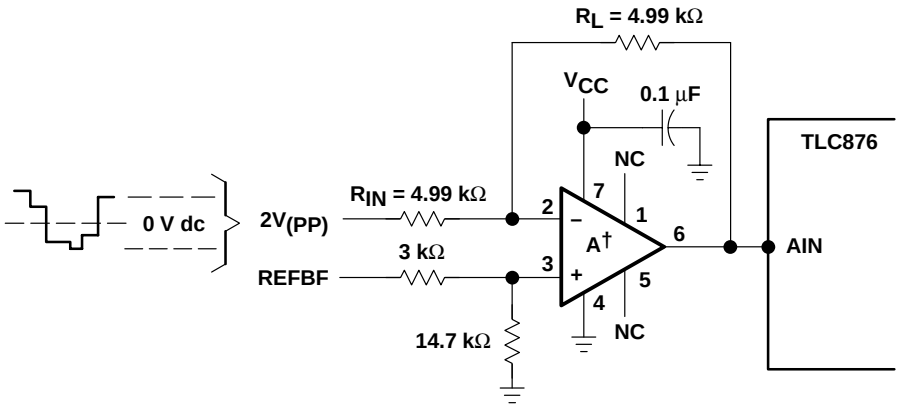
Figure 15. Bias Current and Offset

For systems that require dc-coupling, an op-amp can level-shift a ground-referenced signal to comply with the input requirements of the TLC876. Figure 16 shows an amplifier in an inverting mode with ac signal gain of –1. The dc voltage at the noninverting input of the op-amp controls the amount of dc level shifting. A resistive voltage divider attenuates the REFBF signal and the op-amp then multiplies the attenuated signal by 2. In the case where REFBF = 1.6 V, the dc output level is 2.6 V which is approximately equal to (V(REFTF) – V(REFBF)/2.

† $I_{B(AVG)} = C_E (V_B) f_{CLK} \approx 30$ μA, with $R_{SW} = 50$ Ω, $C_E = 5$ pF, R1 = 50 Ω, and R2 = 1 kΩ
‡ $V_{OFFSET} = I_{B(AVG)} (R1 + R2)$

PRINCIPLES OF OPERATION

driving the analog input (continued)



† Amplifier A can be an AD817 or AD818 with terminal numbers as shown. The AD817 and AD818 are wide bandwidth single supply op-amps.

Figure 16. Bipolar Level Shift

driving the reference terminals

dc considerations

The TLC876 requires an external reference on terminals REFTF and REFBF and a resistor array, nominally 500 Ω, is connected between terminals REFTF and REFBF. A Kelvin connection, using the TLC876 reference sense terminals REFTS and REFBS, minimizes voltage drops caused by external and internal wiring resistance.

Figure 17 shows the equivalent input structure for the reference terminals. There is approximately 5 Ω of resistance between both REFTF and REFBF terminals and the reference ladder. If the force-sense connections are not used, the voltage drop across the 5-Ω resistors results in a reduced voltage appearing across the ladder resistance. This reduces the input span of the converter. Applying a slightly larger span between the REFTF and REFBF terminals compensates for this error. Note that the temperature coefficients of the 5-Ω resistors are 1350 ppm. The effects of temperature should be considered when a force-sense reference configuration is not used.

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dc considerations (continued)

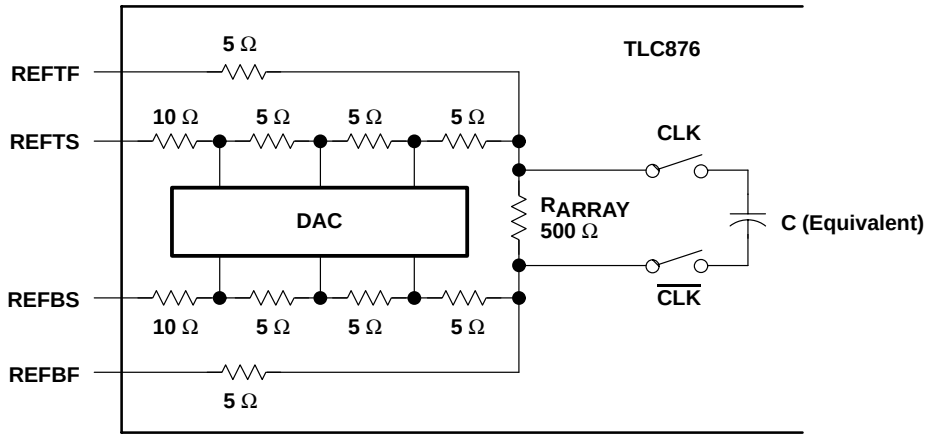

Figure 17. TLC876 Equivalent Reference Structure

The REFTS and REFBS terminals should not be connected in configurations that do not use a force-sense reference. Connecting the force and sense lines together allows current to flow in the sense lines. Any current allowed to flow through these lines must be negligibly small. Current flow causes voltage drops across the resistance in the sense lines. Because the internal DACs tap different points along the sense lines, each DAC would receive a slightly different reference voltage if current were flowing in these lines. To avoid this undesirable condition, leave the sense lines unconnected. Any current allowed to flow through these lines must be negligibly small (< 100 μA).

The voltage drop across the internal resistor array (R_{ARRAY}) determines the input span. The nominal differential voltage is 2 V_{pp}. The full-scale input span is given by equation 3.

$$\text{Input Voltage Span} = V(\text{REFTS}) - V(\text{REFBS}) \quad (3)$$

Therefore, a full-scale input span is approximately 2 V when [V(REFTS) – V(REFBS)] = 2 V. The external reference must provide approximately 4 mA for a 2-V drop across the internal resistor array.

Figure 18 shows the flexibility in determining both the full-scale span of the analog input and where to center this voltage without degrading the typical performance.

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dc considerations (continued)

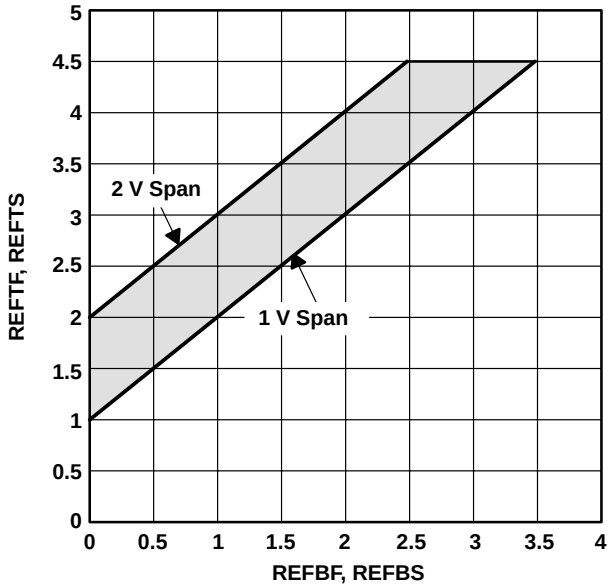


Figure 18. TLC876 Reference Ranges

ac considerations

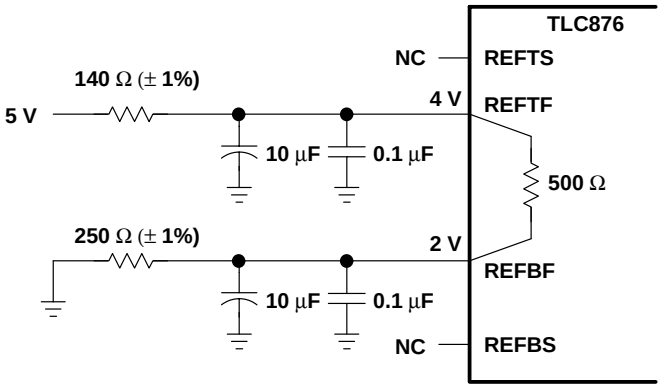
The simplified diagram of Figure 17 shows that the reference terminals connect to a capacitor for one half of the clock period. The size of the capacitor is a function of the analog input voltage, therefore producing dynamic impedance changes at the reference inputs.

The external reference source must be able to maintain a low impedance over all frequencies of interest to provide the charge required by the capacitance. By supplying the requisite charge, the reference voltages remain relatively constant maintaining specified performance. For some reference configurations, voltage transients are present on the reference lines, especially during the falling edge of CLK. The reference must recover from the transients and settle to the desired level of accuracy prior to the rising edges of CLK.

Several useful reference configurations can be used depending on the application, desired level of accuracy, and cost tradeoffs. The simplest configuration, shown in Figure 19, utilizes a resistor divider to generate the reference voltages from the converters analog power supply. The 0.1 μF bypass capacitors reduce high frequency transients. The 10 μF capacitors reduce the impedances at the REFTF and REFBF terminals at lower frequencies; however, as input frequencies approach dc, the capacitors become ineffective, and small voltage deviations appear across the biasing resistors. This reference method maintains 10-bit accuracy for input frequencies above approximately 200 Hz and 8-bit accuracy applications for input frequencies above approximately 50 Hz.

PRINCIPLES OF OPERATION

ac considerations (continued)



NC – No connect

Figure 19. Low Cost Reference Circuit

The reference configuration in Figure 19 provides the lowest cost, but the disadvantages include reduced dc power supply rejection and reduced accuracy due to the variability of the internal and external resistors.

The force-sense reference connections can eliminate the voltage drops associated with the internal connections to the reference ladder. Figure 20 shows a circuit using a dual, rail-to-rail single-supply operational amplifier. The operational amplifier should provide stable 3.6 V and 1.6 V reference voltages. Each half of the amplifier is compensated to drive 1 μF and 0.1 μF decoupling capacitors at the REFTF and REFBF terminals maintaining stability. The operational amplifiers are connected as voltage followers.

By connecting the operational amplifier feedback through the sense connections of the TLC876, the outputs of the operational amplifiers automatically adjust to compensate for the voltage drops that occur within the converter.

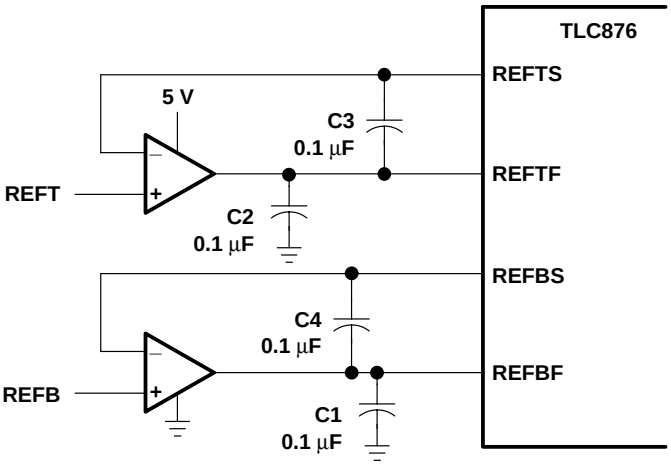
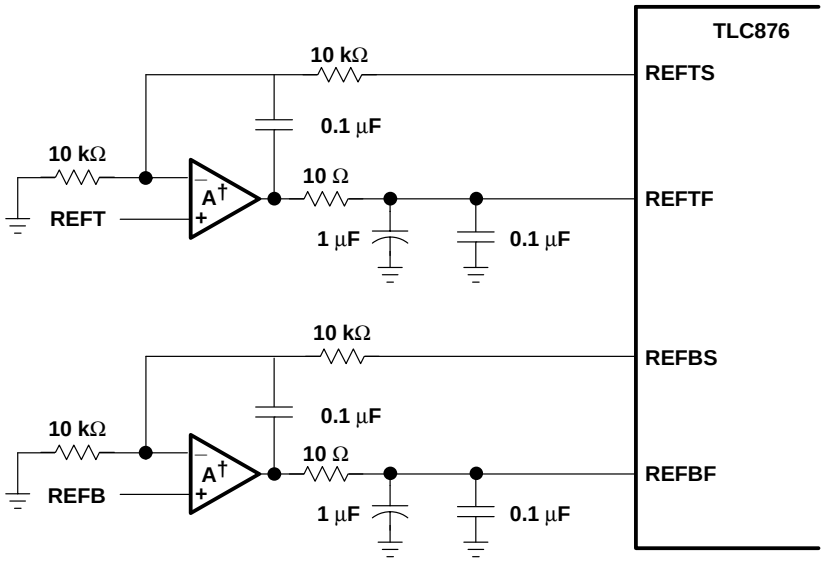


Figure 20. Kelvin Connection Reference Using an Operational Amplifier with Unlimited Capacitive Load Drive Capability

PRINCIPLES OF OPERATION

ac considerations (continued)

Figure 21 shows a circuit using a dual operational amplifier with unlimited capacitive load drive. The operational amplifier should provide stable 3.6 V and 1.6 V reference voltages for REFTF and REFBF, respectively. The amplifier must be able to maintain stability while driving unlimited capacitive loads, so the 0.1 μF capacitors C1 and C2 can connect directly to the outputs of the operational amplifiers, which reduces high frequency transients. Capacitors C3 and C4 shunt across the internal resistors of the force-sense connections and prevent instability. The stability of any operational amplifier used must be examined closely when driving capacitive loads.



† This device is 1/2 of a TLV2442. The TLV2442 is a rail-to-rail output dual operational amplifier.

Figure 21. Kelvin Connection Reference Using an Operational Amplifier with Unlimited Capacitive Load Drive Capability

PRINCIPLES OF OPERATION

layout and decoupling

With high-frequency high-resolution converters, the layout and decoupling of the reference is critical. The actual voltage digitized by the TLC876 is relative to the reference voltages. In Figure 22, for example, the reference return and the bypass capacitors are connected to the shield of the incoming analog signal. Disturbances in the ground of the analog input, that are common mode to the REFTF, REFBF, and AIN terminals because of the common ground, are effectively removed by the TLC876 high common mode rejection. Also, these capacitors should be connected as close to reference terminals as possible.

High-frequency noise sources, V_{N1} and V_{N2}, are shunted to ground by decoupling capacitors. Any voltage drops between the analog input ground and the reference bypassing points are treated as input signals by the converter using the reference inputs. Consequently, the reference decoupling capacitors should be connected to the same physical analog ground point used by the analog input voltage (see the grounding and layout rules section).

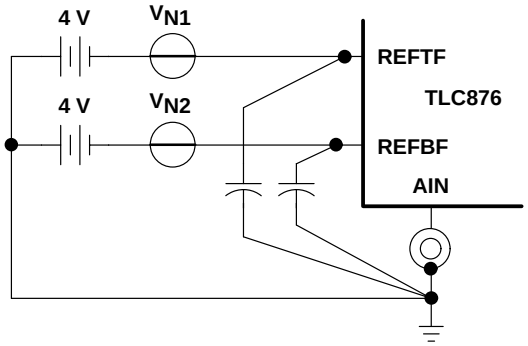


Figure 22. Recommended Bypassing For The Reference

clock input

The clock input is buffered internally with an inverter powered from the DRV_{DD} terminal, which accommodates either 5-V or 3.3-V CMOS logic input signal swings with the input threshold for the CLK terminal nominally at $DRV_{DD}/2$.

The internal pipelined architecture operates on both rising and falling edges of the input clock. To minimize duty cycle variations, the recommended logic family to drive the clock input is high-speed or advanced CMOS (HC/HCT, AC/ACT) logic. CMOS logic provides both symmetrical voltage threshold levels and sufficient rise and fall times to support 20 MSPS operation.

The power dissipated by the correction logic and output buffers is largely proportional to the clock frequency. Figure 8 illustrates this tradeoff between clock rates and a reduction in power consumption.

PRINCIPLES OF OPERATION

digital inputs and outputs

Each of the digital control inputs, $\overline{OE}$ and STBY, has an input buffer powered from the DRV_{DD} supply terminal. With DRV_{DD} set to 5 V, all digital inputs readily interface with 5 V CMOS logic. Using lower voltage CMOS logic, DRV_{DD} can be set to 3.3 V, lowering the nominal input threshold of all digital inputs to (3.3 V)/2 = 1.65 V, typically.

The digital output format is straight binary. For example, Table 1 shows the output format for voltage levels of V(REFTS) = 4 V and V(REFBS) = 2 V.

A low power mode feature is provided such that when STBY is high and the clock is disabled, the static power of the TLC876 drops significantly (see electrical characteristics table).

Table 1. Output Data Format

AIN VOLTAGE (APPROXIMATE)	THREE STATE	DATA									
		D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
> 4 V	0	1	1	1	1	1	1	1	1	1	1
4 V	0	1	1	1	1	1	1	1	1	1	1
3 V	0	1	0	0	0	0	0	0	0	0	0
2 V	0	0	0	0	0	0	0	0	0	0	0
< 2 V	0	0	0	0	0	0	0	0	0	0	0
X	1	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

grounding and layout rules

Proper grounding and layout techniques are essential for achieving optimal performance. The analog and digital grounds on the TLC876 have been separated to optimize the management of return currents in a system. A printed circuit board (PCB) of at least 4 layers employing a ground plane and power planes should be used with the TLC876. The use of ground and power planes offers distinct advantages:

- Minimizes the loop area encompassed by a signal and its return path
- Minimizes the impedance associated with ground and power paths
- The inherent distributed capacitor formed by the power plane, PCB insulation, and ground plane

These characteristics produce a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

A properly designed layout prevents noise from coupling onto the input signal. Digital signal traces should not run parallel with the input signal traces and should be routed away from the input circuitry. The separate analog and digital grounds should be joined together directly under the TLC876. A solid ground plane under the TLC876 is also acceptable if no significant currents are flowing in that portion of the ground plane under the device. The general rule for mixed signal layouts is that return currents from digital circuitry should not pass through or under critical analog circuitry. The system design should minimize the analog lead-in to reduce potential noise pickup.

PRINCIPLES OF OPERATION

digital outputs

The DRV_{DD} supply terminal powers each of the on-chip buffers for the output bits (D0–D9) and is a separate lead from AV_{DD} or DV_{DD}. The output drivers are sized to drive a variety of logic families while minimizing the amount of glitch energy generated. A recommended fan-out of one keeps the capacitive load on the output data drivers below the specified 20 pF level.

For DRV_{DD} = 5 V, the output signal swing can drive both high-speed CMOS and TTL logic families. For TTL, the on-chip output drivers are designed to support several of the high-speed TTL families (F, AS, S). For applications where the clock rate is below 20 MSPS, other TTL families are appropriate. For interfacing with lower voltage CMOS logic, the TLC876 sustains 20 MSPS operation with DRV_{DD} = 3.3 V. Refer to logic family data sheets for compatibility with the TLC876 digital specifications.

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