- **Supports FLEX™ Protocol Messaging Systems With The TLV559X FLEX Decoder**
- **3-Pole Butterworth Low-Pass Selectable Dual-Bandwidth Audio Filter**
  - **BW 1 = 1 kHz ±5% (– 3 dB)**
  - **BW 2 = 2 kHz ±5% (– 3 dB)**
- **Both Peak and Valley Detectors Available**
- **2-Bit Analog-to-Digital Converter**
- **Operating Temperature Range –20°C to 65°C**
- **Four Modes of Operation:**
  - **Fast Track**
  - **Slow Track**
  - **Hold**
  - **Standby**
- **1.8-V to 2.5-V Single Power Supply Operation**

applications

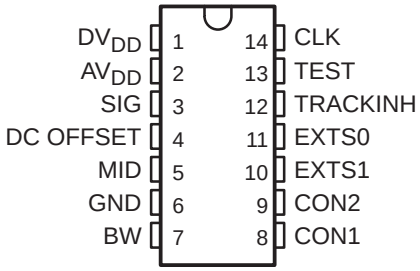
- **FLEX Protocol Numeric and Alphanumeric Messaging Systems**
- **One-Way or Two-Way**

description

The Texas Instruments (TI™) TLV5592 analog-to-digital converter (ADC) is a system level solution to interface a 4-level baseband audio signal to a digital decoder. The TLV5592 is a direct interface to the TLV559X FLEX decoder. Designed primarily for messaging applications, the TLV5592 incorporates signal conditioning, both peak and valley detection along with analog-to-digital conversion. A selectable third-order Butterworth filter with cutoff frequencies of 1 kHz and 2 kHz is included.

The peak and valley detectors are implemented with a unique design that does not require external capacitors. Two 8-bit digital-to-analog converters (DACs) are used in a feedback loop to automatically adjust to the peak and valley levels. The DAC outputs are used to set V_{ref+} and V_{ref-} for the 2-bit ADC. Modes of operation include fast track, slow track, hold, and standby. The standby mode maximizes battery life. The TLV5592 operates on a single power supply from 1.8 V to 2.5 V.

D PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A	PACKAGE
	SMALL OUTLINE (D)
–25°C to 65°C	TLV5592ED

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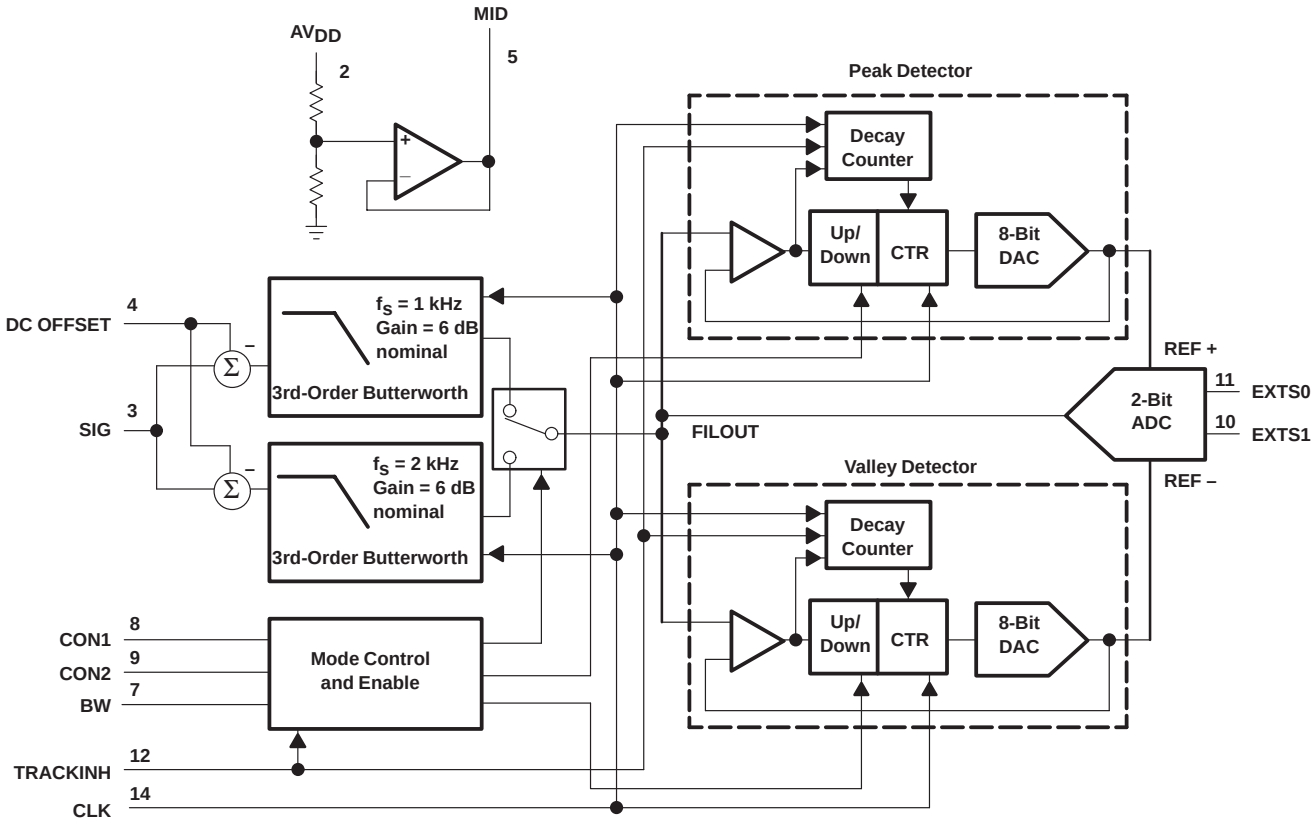
functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AV_{DD}	2	I	Analog supply voltage
BW	7	I	Digital bandwidth select. A high level on BW selects the 2-kHz filter cutoff and a low level selects the 1-kHz filter cutoff.
CON1	8	I	Digital control 1 input. In conjunction with CON2, CON1 selects fast track, slow track, hold, or standby mode.
CON2	9	I	Digital control 2 input. In conjunction with CON1, CON2 selects fast track, slow track, hold, or standby mode.
CLK	14	I	Digital clock input. CLK input is a 50% duty cycle transistor-transistor logic (TTL)-level clock input with nominal frequency of 38.4 kHz. The CLK input is edge sensitive in all non-test modes. For all test modes, the CLK input is level sensitive.
DC OFFSET	4	I	Analog dc offset correction input. The dc component of the audio signal should be applied to DC OFFSET.
DV_{DD}	1	I	Digital supply voltage
EXTS0	11	O	Digital output 0 of the ADC. Data bit 0 is the least significant bit (LSB).
EXTS1	10	O	Digital output 1 of the ADC. Data bit 1 is the most significant bit (MSB).
GND	6		Return terminal for the IC current
MID	5	O	Analog midpoint output. MID is a buffered output of $AV_{DD}/2$.
SIG	3	I	Analog audio signal input. An appropriate resistance capacitance (RC) low-pass filter (antialiasing filter) should be connected to SIG.
TEST	13	I	Digital test input enable. TEST should be connected to ground in normal operation.
TRACKINH	12	I	Digital track inhibit logic input. A high level on TRACKINH disables the peak and valley detector counters; a low level enables the peak and valley detector counters. The counters continue to decay at the decay rate while TRACKINH is a low level.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, AV_{DD}, DV_{DD} . . . . . –0.5 V to 6.5 V
Input voltage range, V_I . . . . . –0.3 V to AV_{DD} + 0.3 V
Output voltage range, EXTS0, EXTS1 . . . . . –0.3 V to DV_{DD} + 0.3 V
Offset input voltage, V_{IO} . . . . . –0.3 V to AV_{DD} + 0.3 V
Peak input current (any input) . . . . . ±20 mA
Operating free-air temperature range, T_A . . . . . –20°C to 65°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, AV_{DD}, DV_{DD}		1.8		2.5	V
Power supply ripple				0.001	V_{pp}
Input clock frequency, $f_{(CLK)}$			38.4		kHz
Input clock duty cycle		45	50	55	%
Voltage offset applied at DC OFFSET, $V_{I(DC\ OFFSET)}$ (see Note 2)		0.25		V_{DD}–0.25	V
Analog input voltage, $V_{I(pp)}$ (See Note 1)	V_{DD} = 2.0 V	V_{IO}–0.355		V_{IO}+0.355	V_{pp}
High-level control input voltage, V_{IH}	V_{DD} = 1.8 V to 2.4 V			0.2 DV_{DD}	V
Low-level control input voltage, V_{IL}	V_{DD} = 1.8 V to 2.4 V	0.8 DV_{DD}			V
Operating free-air temperature, T_A		–25		65	°C

NOTES: 1. The TLV5592 functions and operates down to 1.8 V. Full electrical specifications are ensured from 1.8 to 2.5 V, unless otherwise noted.

2. $$V_{I(MAX/MIN)} = V_{IO} \pm \left(\frac{V_{DD}}{2} - 0.25\right)/(\text{FILTER MAX GAIN})$$

This equation is valid for input sinusoids of less than 800 Hz.

electrical characteristics over recommended operating free-air temperature range, $AV_{DD} = DV_{DD} = 1.8$ V to 2.5 V, $f_{(CLK)} = 38.4$ kHz (unless otherwise noted)

power

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
I_{DD}	Operating supply current	Fast track, slow track, or hold mode		250	μA
$I_{DD(standby)}$	Standby supply current	$V_{I(DC\ OFFSET)} = 0.8$ V, $V_{I(SIG)} = 0.8$ V For all digital inputs, $0 < V_I < 0.5$ V or $V_I > DV_{DD} - 0.5$ V.		1	μA

digital

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -100$ μA	$DV_{DD} - 0.5$			V
V_{OL}	Low-level output voltage	$I_{OL} = 100$ μA			0.5	V
I_{IH}	High-level input current	$V_I = DV_{DD}$		1	2.5	μA
I_{IL}	Low-level input current	$V_I = 0$		–1	–2.5	μA
C_i	Input capacitance, digital input			10		pF

analog

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Voltage accuracy at MID	$V_{DD} = 2$ V, $C_{L(MID)} = 220$ nF	1.42	1.0	1.05	V
Z_i	Input impedance at SIG (see Note 3)	$f_{(IN)} = 1.0$ kHz		1		MΩ
$Z_{i(offset)}$	Input impedance at DC OFFSET (see Note 3)		1	3		MΩ
$I_{I(SIG)}$	Average input current into SIG	$GND < V_I < AV_{DD}$			100	nA
C_i	Input capacitance, all inputs			10		pF

NOTE 3: The input is capacitive and, therefore, is dynamic. Impedance specifications are based on $f_{(CLK)} = 38.4$ kHz.

operating characteristics over recommended operating free-air temperature range, $AV_{DD} = DV_{DD} = 3$ V, $f_{(CLK)} = 38.4$ kHz (unless otherwise noted)

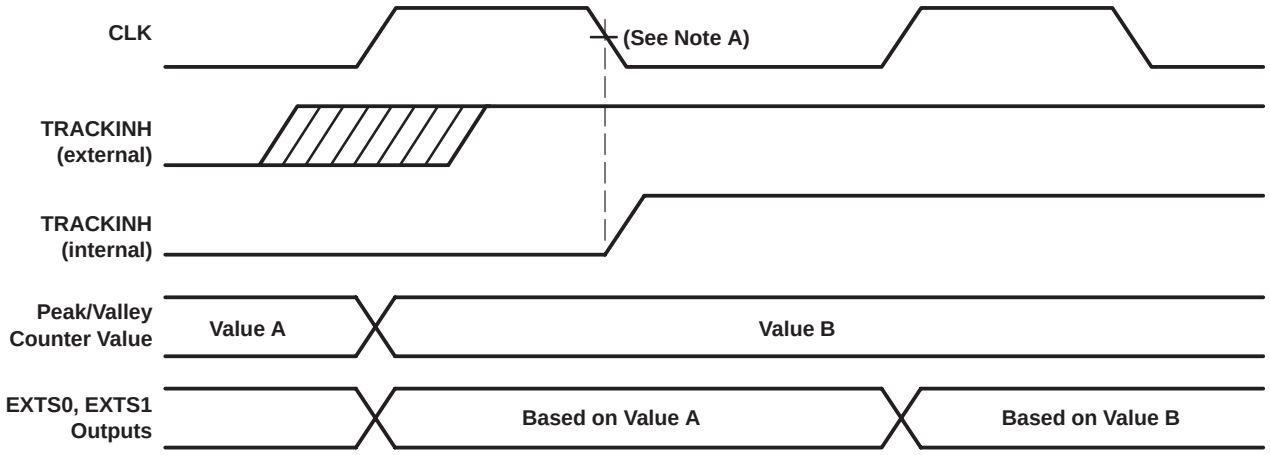
peak-and-valley DACs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Step size, LSB			$V_{DD}/255$		V
E_{FS}	Full-scale error				1	LSB
E_{ZS}	Zero-code error				3	LSB
	Voltage output drift	Hold mode		0		mV/ms
E_D	Differential nonlinearity (DNL) error				1	LSB

low-pass filter

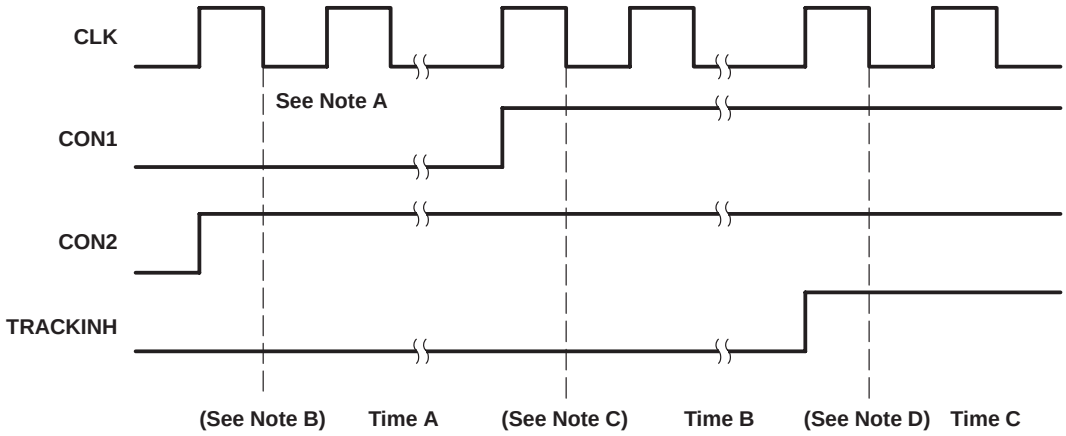
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
G	Pass-band filter gain		$V_{I(DC\ OFFSET)} = 0.8$ V, $V_I = \pm 125$ mV	5.75	6	6.25	dB
	Filter attenuation	1-kHz filter	$V_I = \pm 500$ mV $f_{I(SIG)} = 1$ kHz	2	3	4	dB
		2-kHz filter	$V_I = \pm 500$ mV $f_{I(SIG)} = 2$ kHz	2	3	4	
t_s	Stabilization time		Off mode to hold mode (see Table 1)			5	ms

PARAMETER MEASUREMENT INFORMATION



NOTE A: Internally the device recognizes input conditions on the falling edge of the clock only.

Figure 1. Timing Diagram



NOTES: A. Internally the device recognizes input conditions on the falling edge of the clock only.
B. On the next falling edge of the clock with the input conditions shown, the TLV5592 tracks signal in fast track mode (peak DAC counter counts down by 8 and up by 4) in time A.
C. On the next falling edge of the clock with the input conditions shown, the TLV5592 tracks signal in slow track mode (peak DAC counter counts up by 2 and down by 1 every 40 clock cycles) in time B.
D. On the next falling edge of the clock with the input conditions shown, the TLV5592 holds previous peak and valley levels in time C. For the 2-bit output, when TRACKINH = 1, EXTS0 and EXTS1 outputs respond in real time to the condition of SIG and DC OFFSET as long as the CLK signal is present.

Figure 2. Track and Lock Timing

TYPICAL CHARACTERISTICS

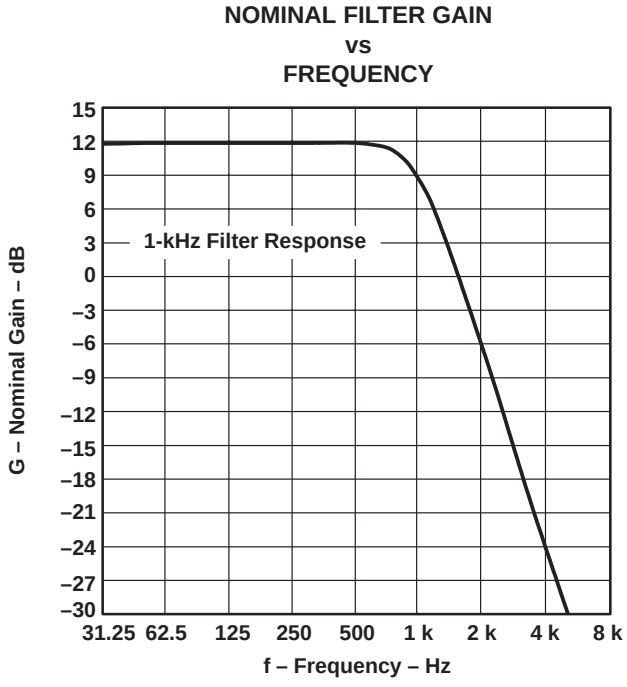


Figure 3

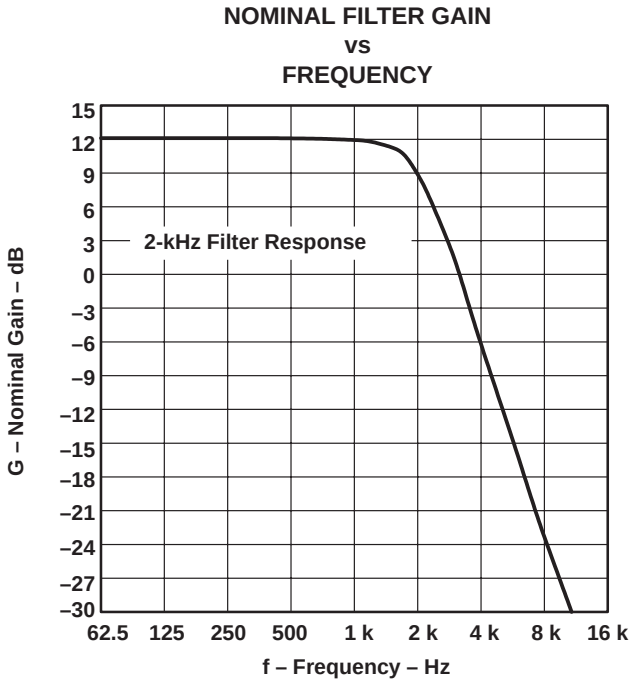


Figure 4

PRINCIPLES OF OPERATION

analog input operation

As shown in the functional block diagram, the signal input is dc-coupled using a single input terminal, SIG. A voltage equivalent to the nominal dc voltage of the signal input at SIG should be supplied on an additional terminal, DC OFFSET. This allows the device to increase the signal to acceptable levels for threshold detection without saturating against the supplies. The signal processed by the device is effectively the voltage difference between the SIG and DC OFFSET terminals.

There is no antialiasing filter incorporated in the device. TI recommends that an external RC filter be added and set at the appropriate cutoff (see Figure 5).

The maximum peak analog signal voltage that can be applied to the SIG input terminal is given by:

$$V_{I(MAX/MIN)} = V_{IO} \pm \left(\frac{V_{DD}}{2} - 0.25\right)/(\text{FILTER MAX GAIN})$$

where:

$V_{I(MIN/MAX)}$ = Analog input voltage (SIG)

V_{IO} = Input offset voltage (dc offset)

$V_{DD}/2$ = the nominal output voltage at the MID terminal

The main signal path consists of a third-order switched-capacitor Butterworth filter, with a bandwidth that is switchable between 1 kHz and 2 kHz to remove the noise from the input signal. The peak and valley amplitudes of the filter output signal are detected and subsequently used to convert the 4-level audio into 2-level digital signals using three switched capacitor comparators.

digital operation

The peak and valley detection is performed by a mixed mode solution using an 8-bit DAC and an up/down counter that has nonsymmetrical up and down count rates. Various modes are included to force the peak and valley circuits to slow track, fast track, or hold. An off mode is included that forces the device into a low-power condition. The decay rate of the peak and valley circuits is controlled by independent counters.

The device is clocked with a 38.4-kHz square wave supplied externally. The attack and decay times of the peak and valley circuits and the filter cutoff frequencies are directly related to this clock frequency. The decay timer is gated by the track inhibit input, TRACKINH, which is reset to 1 after an attack occurs and reset to 40 after a decay enable. The TRACKINH also prevents attack enable inputs from affecting the peak and valley counters.

PRINCIPLES OF OPERATION

digital control

Five digital inputs and the CLK input control the TLV5592. The five signals are BW, CON1, CON2, TRACKINH and TEST. All digital control inputs are latched internally on the falling edge of the CLK input. The BW input selects the cutoff frequency of the input signal third-order Butterworth switched-capacitor filter. The CON1 and CON2 inputs determine when the TLV5592 is in tracking fast, tracking slow, hold, or low-power standby mode. In test mode the CLK input is level sensitive, and in all other modes the CLK input is edge sensitive.

Table 1 lists the functions for the five control inputs.

Table 1. Control Inputs Function Table

BW		SWITCHED-CAPACITOR FILTER (– 3 dB POINT)
Low		1-kHz filter cutoff
High		2-kHz filter cutoff
CON1	**CON2**	**MODE**
Low	Low	Low-power standby (off) mode
Low	High	Fast track mode
High	Low	Hold mode
High	High	Slow track mode
TRACKINH		**RESULT**
Low		Tracking enabled
High		Tracking disabled

track inhibit

The TRACKINH input enables the counters to the peak and valley detector DACs. When enabled, the counters adjust to create a DAC output that is the same as the filtered input signal peak and valley. The counters decay at the fast or slow decay rates while the TRACKINH input is held low. The TRACKINH line should be connected to SYMCLK terminal on the TLV559X decoder.

analog-to-digital conversion

The TLV5592 employs a 2-bit ADC to convert a 4-level analog signal to digital data. The digital output is presented on EXTS0 and EXTS1 with EXTS0 being the LSB. The peak and valley DACs provide the maximum and minimum voltages (V_{ref+} and $V_{ref–}$) to the ADC. The input to the 2-bit ADC is the output of the Butterworth low-pass filter, FILOUT, as shown in the block diagram. The ADC transfer function is shown in Table 2.

Table 2. Filter Output Voltage Selection (see Note 4)

EXTS1	EXTS0	FILTER OUTPUT VOLTAGE (FILOUT)
Low	Low	FILOUT < ((peak – valley) x 50/256) + valley
High	Low	((peak – valley) x 50/256) + valley < FILOUT < ((peak – valley) x 134/256) + valley
High	High	((peak – valley) x 134/256) + valley < FILOUT < ((peak – valley) x 217/256) + valley
Low	High	FILOUT > ((peak – valley) x 217/256) + valley

NOTE 4: The constants 50/256, 134/256, and 217/256 have a ± 5% tolerance.

PRINCIPLES OF OPERATION

The thresholds for the ADC comparators are set by capacitor ratios in switched-capacitor comparators. For a 2-bit ADC, three comparators are used with thresholds set as shown in Table 3.

Table 3. Comparators and Associated Threshold Values (see Notes 4 and 5)

COMPARATOR	VALUE	UNIT
Lower threshold	((peak – valley) x 50/256) + valley	V
Middle threshold	((peak – valley) x 134/256) + valley	V
Upper threshold	((peak – valley) x 217/256) + valley	V

NOTES: 4. The constants 50/256, 134/256, and 217/256 have a ± 5% tolerance.
5. The comparator thresholds are measured with the input voltage level of the SIG terminal at 125 mV ac centered on 800 mV dc, and the input voltage at the DC OFFSET terminal is 800 mV dc.

peak and valley timing

The peak and valley attack and delay times are controlled by two 8-bit up-down counters clocked by the CLK input. The rate that the counters are clocked depends on whether the counters are in attack or decay mode. The peak counter is in attack mode when the input signal amplitude is greater than the output voltage from the peak DAC, and it is in decay mode when the input signal amplitude is less that the peak DAC output voltage. The valley counter is in attack mode when the input signal amplitude is less than the output voltage from the valley DAC, and it is in decay mode when the input signal amplitude is greater than the valley DAC output voltage.

When TRACKINH is held high, the attack and decay enable inputs to the peak and valley counters are disabled. When TRACKINH is held low, the attack and decay enable inputs to the peak and valley counters are enabled. The effect of the TRACKINH signal is exactly the same as when the device is configured in hold mode.

slow track mode attack and decay times

The attack rate is calculated equal to $[V_{DD} \times f_{(CLK)} \times 2] / 256 /$ (TRACKINH duty cycle). So the peak and valley counter is incremented or decremented by 2 on every clock cycle when the input signal amplitude is greater than or less than the peak and valley DAC output voltage.

The decay rate is calculated equal to $[V_{DD} \times f_{(CLK)}] / (256 \times 40) /$ (TRACKINH duty cycle). So the peak and valley counter is decremented or incremented once every 40 clock cycles when the input signal amplitude is less than or greater than the peak and valley DAC output voltage.

When the counters receive an attack enable at the same time as a decay enable, the attack enable takes precedence. The decay counter is reset to 1 after an attack and reset to 40 following a decay.

The attack and decay times for a V_{DD} supply variation of 1.8 V to 2.5 V and a fixed clock input of 38.4 kHz are given in Table 4.

Table 4. Slow Track Mode Attack and Decay Times

DESCRIPTION	CONDITIONS	MIN	MAX	UNIT
Attack rate (ATTR)	TRACKINH = Low	810	990	mV/ms
Decay rate (DECR)	TRACKINH = Low	10.125	12.375	mV/ms

PRINCIPLES OF OPERATION

fast track mode attack and decay times

The attack rate is calculated equal to $[V_{DD} \times f_{(CLK)} \times 4] / 256 /$ (TRACKINH duty cycle). So the peak and valley counter is incremented or decremented by a count of 4 on every clock cycle when the input signal amplitude is greater than or less than the peak and valley DAC output voltage.

The decay rate is calculated equal to $[V_{DD} \times f_{(CLK)} \times 8] / 256 /$ (TRACKINH duty cycle). So the peak and valley counter is decrement or increment by 8 on every clock cycle when the input signal amplitude is less than or greater than the peak and valley DAC output voltage.

When the device is in fast track mode, the decay counter is reset to 1.

The attack and decay times for a V_{DD} supply variation of 1.8 V to 2.5 V and a fixed clock input of 38.4 kHz are given in Table 5.

Table 5. Fast Track Mode Attack and Decay Times

DESCRIPTION	CONDITIONS	MIN	MAX	UNIT
Attack rate (ATTR)	TRACKINH = Low	1620	1980	mV/ms
Decay rate (DECR)	TRACKINH = Low	3240	3960	mV/ms

hold mode

In hold mode the peak and valley counters are disabled from counting when either attack or decay enable signals are present. There is no change to the peak and valley DAC output voltages in this mode.

When the device is in hold mode, the decay counter is reset to 1.

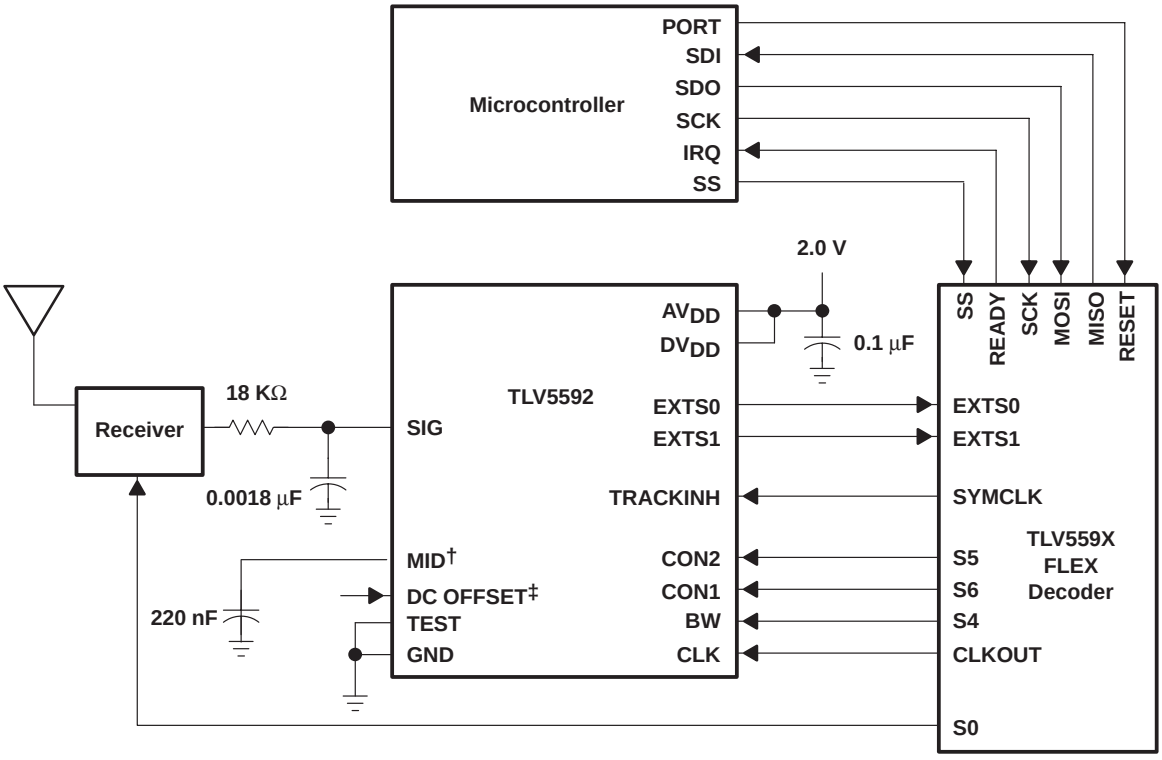
off mode

In off mode, the peak and valley counters are disabled from counting, and the device is set to low-power standby mode. Both peak and valley voltages float to the V_{DD} voltage as the resistor string element within the DAC structure is isolated from the ground (GND) supply to conserve power. When the off state is released, the peak and valley voltages return to the previously set values.

When the device is in off mode, the decay counter is reset to 1.

APPLICATION INFORMATION

The TLV5592 converter is optimized for messaging applications. The TLV5592 optimizes the filtering and conversion resolution to meet the specific requirements of FLEX messaging devices. The combination of the TLV5592 converter and TLV559X decoder reduces overall system cost by allowing a low-cost microcontroller to be used in the messaging system. Figure 5 shows the basic connections between system elements.



† The voltage on the MID terminal is nominally $AV_{DD}/2$.
‡ The voltage applied to the DC OFFSET terminal is equal to the dc offset voltage of the input signal applied to the SIG terminal.

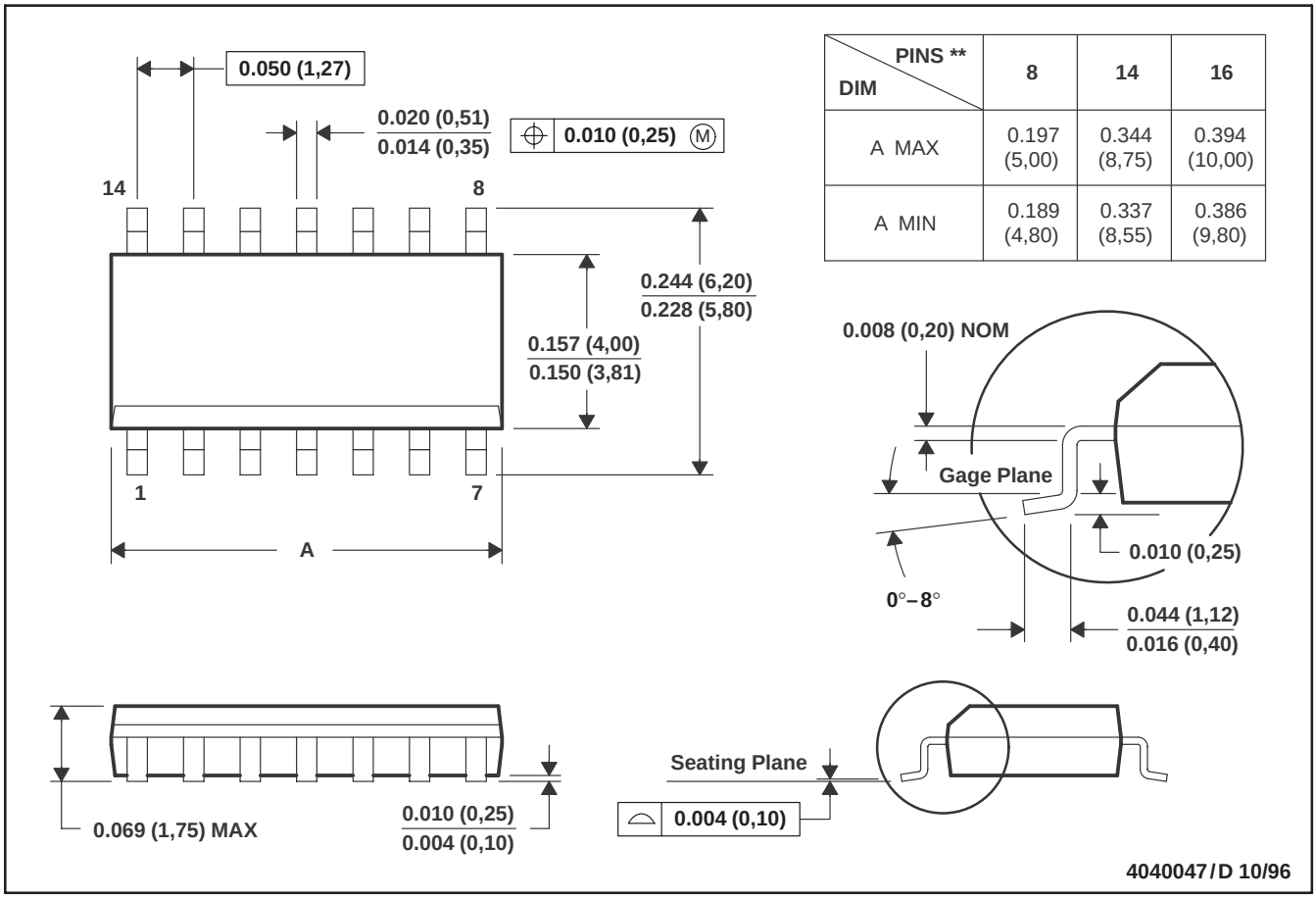
Figure 5. TLV5592 Application Schematic

At least one bit of warm-up time in fast track mode followed by five bits of warm-up time in slow track mode is necessary before valid data can be present. Hold mode is used during a data transfer, and fast track mode is used for warm-up. Slow track mode is used for tracking during the synchronization portion of the data.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



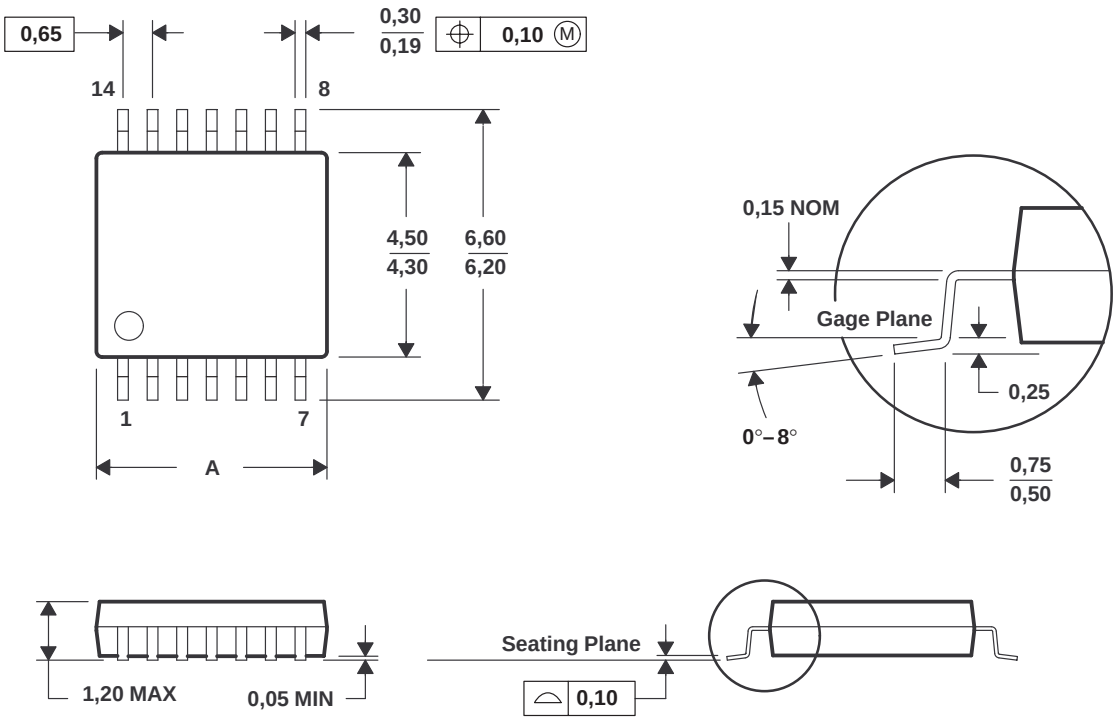
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/E 08/96

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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