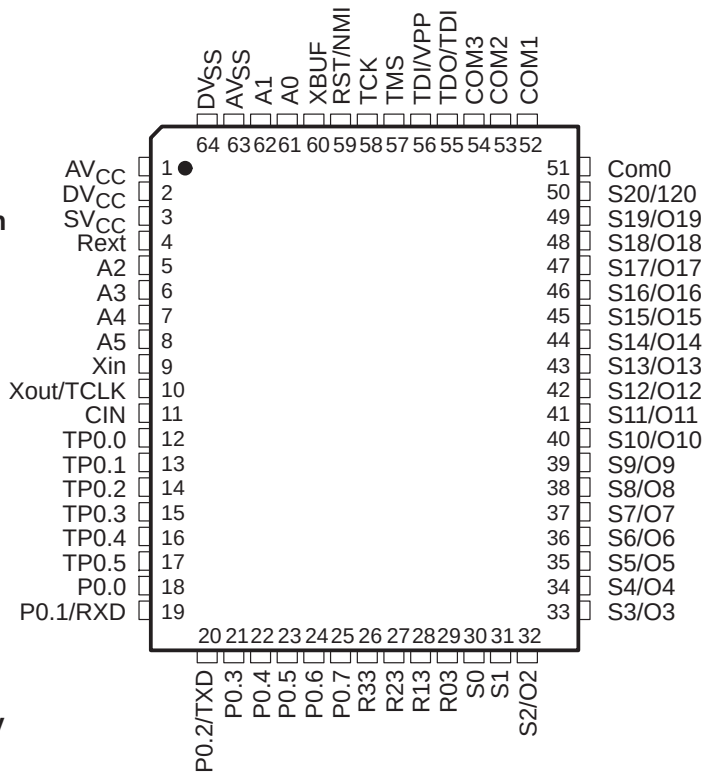
SLAS164 – FEBRUARY 1998

- **Low Supply Voltage Range, 2.5 V – 5.5 V**
- **Low Operation Current, 400 μA at 1 MHz, 3 V**
- **Ultra-Low Power Consumption (Standby Mode Down to 0.1 μA)**
- **Five Power-Saving Modes**
- **Wakeup From Standby Mode in 6 μs**
- **16-Bit RISC Architecture, 300 ns Instruction Cycle Time**
- **Single Common 32 kHz Crystal, Internal System Clock Up to 3.3 MHz**
- **Integrated LCD Driver for Up to 84 Segments**
- **Integrated 12+2 Bit A/D Converter**
- **Family Members Include:**
  - **MSP430C323, 8KB ROM, 256 Byte RAM**
  - **MSP430C325, 16KB ROM, 512 Byte RAM**
  - **MSP430P325, 16KB OTP, 512 Byte RAM**
- **EPROM Version Available for Prototyping: PMS430E325**
- **Serial On-Board Programming**
- **Programmable Code Protection by Security Fuse**
- **Avaliable in 64 Pin Quad Flatpack (QFP), 68 Pin Plastic J-Leaded Chip Carrier (PLCC), 68 Pin J-Leaded Ceramic Chip Carrier (JLCC) Package (EPROM Version)**

PG Package
(TOP VIEW)



description

The Texas Instruments MSP430 series is a ultra low-power microcontroller family consisting of several devices which feature different sets of modules targeted to various applications. The microcontroller is designed to be battery operated for an extended application lifetime. With 16-bit RISC architecture, 16 bit integrated registers on the CPU, and the constant generator, the MSP430 achieves maximum code efficiency. The digitally-controlled oscillator, together with the frequency-locked-loop (FLL), provides a fast wakeup from a low-power mode to active mode in less than 6 μs.

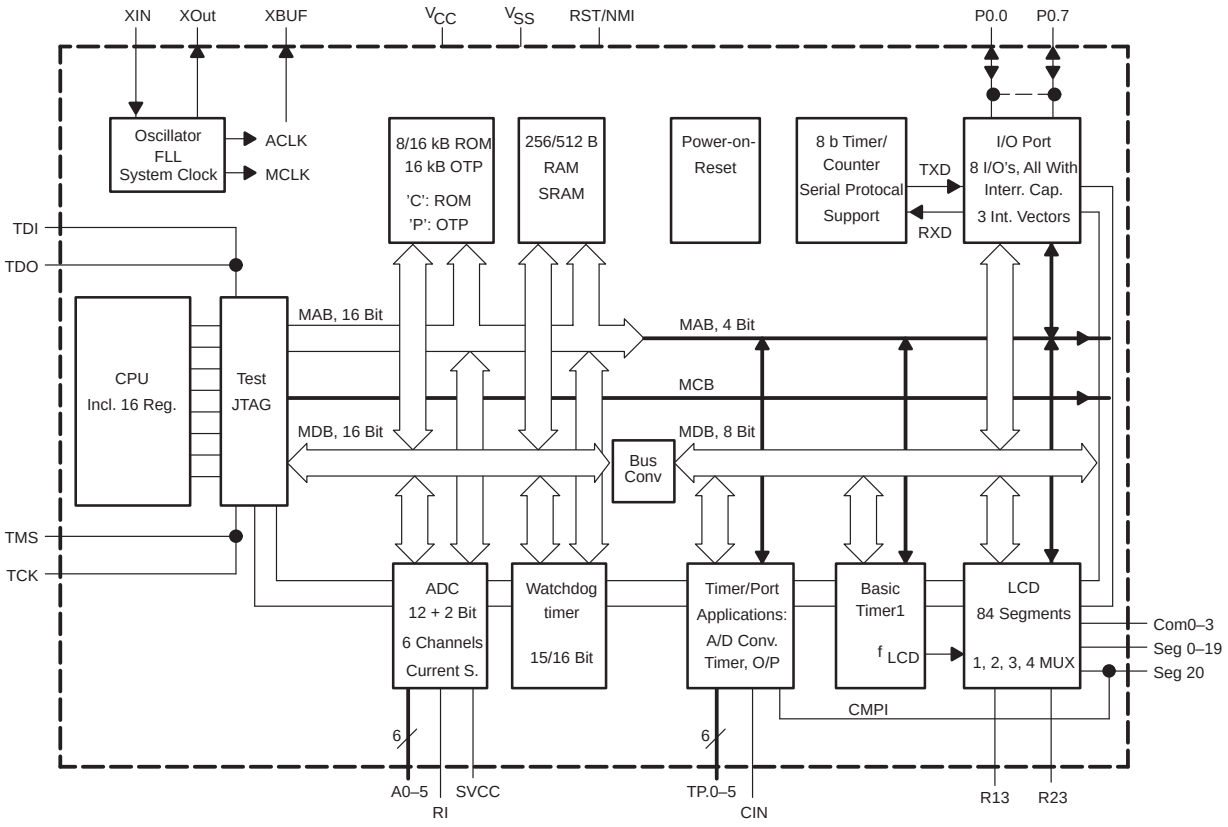
Typical applications include sensor systems that capture analog signals, converts them to digital values, and then processes the data and displays them or transmits them to a host system. The MSP430x32x offers an integrated 12+2 bit A/D converter with six multiplexed inputs.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			
	PLASTIC QFP (PG)	PLASTIC QFP (PM)	PLASTIC PLCC (FN)	CERAMIC JLCC (FZ)
–40°C to 85°C	MSP430C323IPG MSP430C325IPG MSP430P325IPG	MSP430C323IPM MSP430C325IPM MSP430P325IPM	MSP430C323IFN MSP430C325IFN MSP430P325IFN	—
25°C	—	—	—	PMS430E325FZ

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO. PG	I/O	DESCRIPTION
AV_{CC}	1		Positive analog supply voltage
AV_{SS}	63		Analog ground reference
A0	61	I	Analog-to-digital converter input port 0 or digital input port 0
A1	62	I	Analog-to-digital converter input port 1 or digital input port 1
A2–A5	5–8	I	Analog-to-digital converter inputs ports 2–5 or digital inputs ports 2–5
CIN	11	I	Input used as enable of counter TPCNT1 – timer/port
COM0–3	51–54	O	Common outputs, used for LCD backplanes – LCD
DV_{CC}	2		Positive digital supply voltage
DV_{SS}	64		Digital ground reference
P0.0	18	I/O	General purpose digital I/O
P0.1/RXD	19	I/O	General purpose digital I/O, receive digital inport port, 8-bit timer/counter
P0.2/TXD	20	I/O	General purpose digital I/O, transmit data output port, 8-bit timer/counter
P0.3–P0.7	21–25	I/O	Five general purpose digital I/Os, bit 3 to bit 7
Rext	4	I	Programming resistor input of internal current source
RST/NMI	59	I	Reset input or non-maskable interrupt input
R03	29	I	Input of fourth positive analog LCD level (V4) – LCD
R13	28	I	Input of third positive analog LCD level (V3) – LCD
R23	27	I	Input of second positive analog LCD level (V2) – LCD
R33	26	O	Output of first positive analog LCD level (V1) – LCD
SV_{CC}	3		Switched AV_{CC} to analog-to-digital converter
S0	30	O	Segment line S0 – LCD
S1	31	O	Segment line S1 – LCD
S2–S5/O2–O5	32–35	O	Segment lines S2 to S5 or digital output ports O2–O5, group 1 – LCD
S20/I20	50	I/O	Segment line S20 can be used as comparator input port CMP1 – timer/port
S6–S9/O6–O9	36–39	O	Segment lines S6 to S9 or digital output ports O6–O9, group 2 – LCD
S10–S13/O10–O13	40–43	O	Segment lines S10 to S13 or digital output ports O10–O13, group 3 – LCD
S14–S17/O14–O17	44–47	O	Segment lines S14 to S17 or digital output ports O14 to O17, group 4 – LCD
S18-S19/O18-O19	48, 49	O	Segment lines S18 and S19 or digital output port O18 and O19, group 5 – LCD
TCK	58	I	Test clock, clock input terminal for device programming and test
TDO/TDI	55	I/O	Test data output, data output terminal or data input during programming
TDI/VPP	56	I	Test data input, data input terminal or input of programming voltage
TMS	57	I	Test mode select, input terminal for device programming and test
TP0.0	12	O	General purpose 3-state digital output port, bit 0 – timer/port
TP0.1	13	O	General purpose 3-state digital output port, bit 1 – timer/port
TP0.2	14	O	General purpose 3-state digital output port, bit 2 – timer/port
TP0.3	15	O	General purpose 3-state digital output port, bit 3 – timer/port
TP0.4	16	O	General purpose 3-state digital output port, bit 4 – timer/port
TP0.5	17	I/O	General purpose digital input/output port, bit 5 – timer/port
XBUF	60	O	Clock signal output of system clock MCLK or crystal clock ACLK
Xin	9	I	Input terminal of crystal oscillator
Xout/TCLK	10	I/O	Output terminal of crystal oscillator or test clock input

short-form description

processing unit

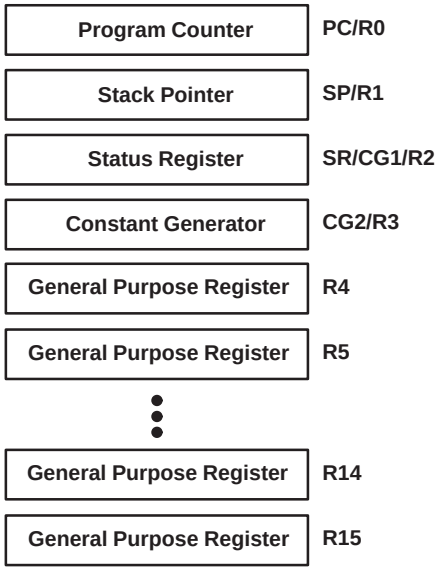
The processing unit is based on a consistent and orthogonal designed CPU and instruction set. This design structure results in a RISC-like architecture, highly transparent to the application development and is distinguished due to ease of programming. All operations other than program-flow instructions are consequently performed as register operations in conjunction with seven addressing modes for source and four modes for destination operand.

cpu

Sixteen registers are located inside the CPU, providing reduced instruction execution time. This reduces a register-register operation execution time to one cycle of the processor frequency.

Four of the registers are reserved for special use as a program counter, a stack pointer, a status register and a constant generator. The remaining registers are available as general purpose registers.

Peripherals are connected to the CPU using a data address and control bus and can be handled easily with all instructions for memory manipulation.



instruction set

The instruction set for this register-register architecture provides a powerful and easy-to-use assembler language. The instruction set consists of 52 instructions with three formats and seven addressing modes. Table 1 provides a summation and example of the three types of instruction formats; the addressing modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD	R4, R5	R4 + R5 → R5
Single operands, destination only	e.g. CALL	R8	PC → (TOS), SR → (TOS), R8 → PC
Relative jump, un-/conditional	e.g. JNE		Jump-on equal bit = 0

Each instruction that operates on word and byte data is identified by the suffix B.

Examples:	Instructions for word operation		Instructions for byte operation	
	MOV	ede, toni	MOV.B	ede, toni
	ADD	#235h, & MEM	ADD.B	#35h, & MEM
	PUSH	R5	PUSH.B	R5
	SWPB	R5	—	

Table 2. Address Mode Descriptions

ADDRESS MODE	s	d	SYNTAX	EXAMPLE	OPERATION
Register	√	√	MOV Rs, Rd	MOV R10, R11	R10 → R11
Indexed	√	√	MOV X(Rn), Y(Rm)	MOV 2(R5), 5(R6)	M(2 + R5) → M(6 + R6)
Symbolic (PC relative)	√	√	MOV EDE, TONI		M(EDE) → M(TONI)
Absolute	√	√	MOV &MEM, &TCDAT		M(MEM) → M(TCDAT)
Indirect	√		MOV @Rn, Y(Rm)	MOV @R10, Tab(R6)	M(R10) → M(Tab + R6)
Indirect autoincrement	√		MOV @Rn+, RM	MOV @R10+, R11	M(R10) → R11, R10 + 2 → R10
Immediate	√		MOV #X, TONI	MOV #45, TONI	#45 → M(TONI)

NOTE: s – source d = destination

Computed branches (BR) and subroutine calls (CALL) instructions use the same addressing modes as the other instructions. These addressing modes provide *indirect* addressing, ideally suited for computed branches and calls. The full use of this programming capability permits a program structure different from conventional 8- and 16-bit controllers. For example, numerous routines can easily be designed to deal with pointers and stacks instead of using Flag type programs for flow control.

operation modes and interrupts

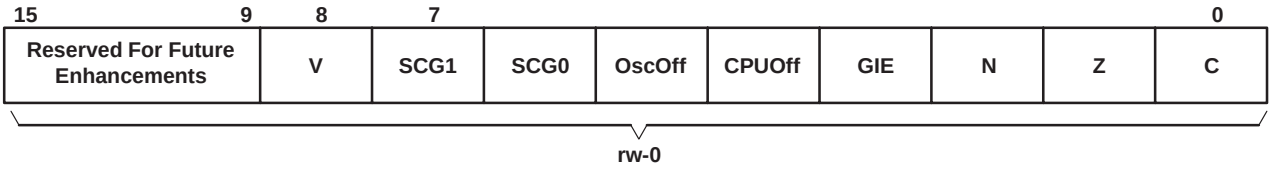
The MSP430 operating modes support various advanced requirements for ultra-low power and ultra-low energy consumption. This is achieved by the intelligent management of the operations during the different module operation modes and CPU states. The requirements are fully supported during interrupt event handling. An interrupt event awakens the system from each of the various operating modes and returns with the RETI instruction to the mode that was selected before the interrupt event. The clocks used are ACLK and MCLK. ACLK is the crystal frequency and MCLK is a multiple of ACLK and is used as the system clock.

There are five operating modes the software can configure:

- Active mode (AM). The CPU is enabled with different combinations of active peripheral modules.
- Low power mode 0 (LPM0). The CPU is disabled, peripheral operation continues, ACLK and MCLK signals are active, and loop control for MCLK is active.
- Low power mode 1 (LPM1). The CPU is disabled, peripheral operation continues, ACLK and MCLK signals are active, and loop control for MCLK is inactive.
- Low power mode 2 (LMP2). The CPU is disabled, peripheral operation continues, ACLK signal is active, and MCLK and loop control for MCLK are inactive.
- Low power mode 3 (LMP3). The CPU is disabled, peripheral operation continues, ACLK signal is active, MCLK and loop control for MCLK are inactive, and the dc generator for the digital controlled oscillator (DCO) (→MCLK generator) is switched off.
- Low power mode 4 (LMP4). The CPU is disabled, peripheral operation continues, ACLK signal is inactive (crystal oscillator stopped), MCLK and loop control for MCLK are inactive, and the dc generator for the DCO is switched off.

The special function registers (SFR) include module-enable bits that stop or enable the operation of the specific peripheral module. All registers of the peripherals may be accessed if the operational function is stopped or enabled. However, some peripheral current-saving functions are accessed through the state of local register bits. An example is the enable/disable of the analog voltage generator in the LCD peripheral which is turned on or off using one register bit.

The most general bits that influence current consumption and support fast turn-on from low power operating modes are located in the status register (SR). Four of these bits control the CPU and the system clock generator: SCG1, SCG0, OscOff, and CPUOff.



interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the ROM with an address range of 0FFFFh-0FFE0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up, external reset, watchdog	RSTI, WDI (see Note1)	Reset	0FFFEh	15, highest
NMI, oscillator fault	RSTI, OFIFG (see Note 1)	non-maskable, (non)-maskable	0FFFCh	14
Dedicated I/O	P0.0IFG	maskable	0FFFAh	13
Dedicated I/O	P0.1IFG	maskable	0FFF8h	12
			0FFF6h	11
Watchdog timer	WDTIFG	maskable	0FFF4h	10
			0FFF2h	9
			0FFF0h	8
			0FFEEh	7
			0FFECh	6
ADC	ADCIFG	maskable	0FFEAh	5
Timer/Port	See Note 2	maskable	0FFE8h	4
			0FFE6h	3
			0FFE4h	2
Basic timer	BTIFG	maskable	0FFE2h	1
I/O port 0	P0.27IFG (see Note 1)	maskable	0FFE0h	0, lowest

NOTES: 1. Multiple source flags
2. Timer/port interrupt flags are located in the T/P registers

special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits that are not allocated to a functional purpose are not physically present in the device. Simple SW access is provided with this arrangement.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h					P0IE.1	P0IE.0	OFIE	WDTIE
					rw-0	rw-0	rw-0	rw-0

WDTIE: Watchdog timer enable signal
OFIE: Oscillator fault enable signal
P0IE.0: Dedicated I/O P0.0
P0IE.1: P0.1 or 8-bit timer/counter, RXD

Address	7	6	5	4	3	2	1	0
01h	BTIE				TPIE	ADIE		
	rw-0				rw-0	rw-0		

ADIE: A/D converter enable signal
TPIE: Timer/port enable signal
BTIE: Basic timer enable signal

interrupt flag register 1 and 2

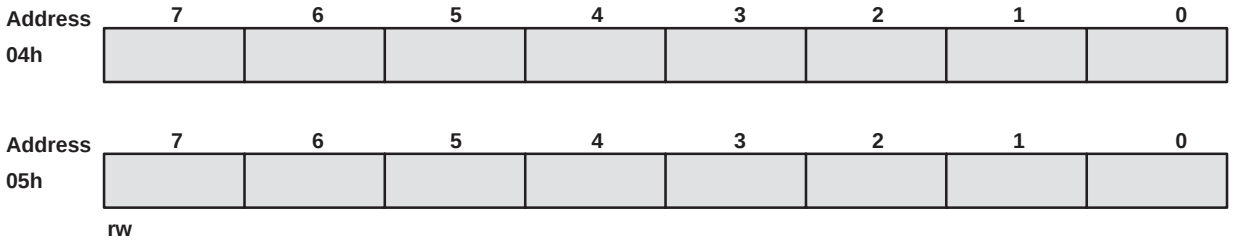
Address	7	6	5	4	3	2	1	0
02h				NMIIFG	P0IFG.1	P0IFG.0	OFIFG	WDTIFG
				rw-0	rw-0	rw-0	rw-1	rw-0

WDTIFG: Set on overflow or security key violation
or
Reset on V_{CC} power on or reset condition at RST/NMI-pin
OFIFG: Flag set on oscillator fault
P0.0IFG: Dedicated I/O P0.0
P0.1IFG: P0.1 or 8-bit timer/counter, RXD
NMIIFG: Signal at RST/NMI-pin

Address	7	6	5	4	3	2	1	0
03h	BTIFG					ADIFG		
	rw					rw-0		

BTIFG Basic timer flag
ADFIG Analog-to-digital converter flag

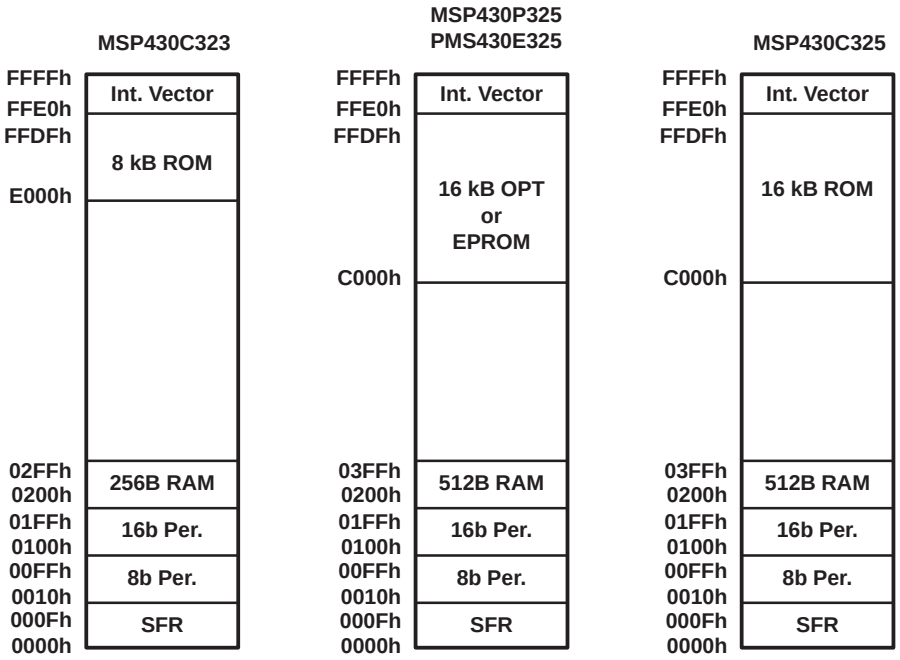
module enable register 1 and 2



Legend

rw:	Bit can be read and written
rw-0:	Bit can be read and written. It is reset by PUC
	SFR bit not present in device

memory organization



peripherals

Peripherals connect to the CPU through data, address, and control busses and can be handled easily with all instructions for memory manipulation.

oscillator and system clock

Two clocks are used in the system, the system (master) clock (MCLK) and the auxiliary clock (ACLK). The MCLK is a multiple of the ACLK. The ACLK runs with the crystal oscillator frequency. The special design of the oscillator supports the feature of low current consumption and the use of a 32 768 Hz crystal. The crystal is connected across two terminals without any other external components being required.

The oscillator starts after applying VCC, due to a reset of the control bit (OscOff) in the status register (SR). It can be stopped by setting the OscOff bit to a 1. The enabled clock signals ACLK, ACLK/2, ACLK/4, OR MCLK are accessible for use by external devices at output terminal XBUF.

The controller system clock has to operate with different requirements according to the application and system conditions. Requirements include:

- High frequency in order to react quickly to system hardware requests or events
- Low frequency in order to minimize current consumption, EMI, etc.
- Stable frequency for timer applications e.g. real time clock (RTC)
- Enable start-stop operation with a minimum of delay.

These requirements cannot all be met with fast frequency high-Q crystals or with RC-type low-Q oscillators. The compromise selected for the MSP430 uses a low-crystal frequency which is multiplied to achieve the desired nominal operating range:

$$f_{(system)} = N \times f_{(crystal)}$$

The crystal frequency multiplication is acheived with a frequency locked loop (FLL) technique. The factor N is recommended to be 32. The FLL technique, in combination with a digital controlled oscillator (DCO) provides immediate start-up capability together with long term crystal stability. The frequency variation of the DCO with the FLL inactive is typically 330 ppm which means that with a cycle time of 1 μs the maximum possible variation is 0.33 ns. For more precise timing, the FLL can be used which forces longer cycle times if the previous cycle time was shorter than the selected one. This switching of cycle times makes it possible to meet the chosen system frequency over a long period of time.

The start-up operation of the system clock depends on the previous machine state. During a power-up clear (PUC), the DCO is reset to its lowest possible frequency. The control logic starts operation immediately after recognition of PUC.

digital I/O

There is one 8-bit I/O port (Port0) implemented. Six control registers give maximum flexibility of digital input/output to the application:

- All individual I/O bits are programmable independently.
- Any combination of input, output, and interrupt conditions is possible.
- Interrupt processing of external events is fully implemented for all eight bits of port P0.
- Provides read/write access to all registers with all instructions.

The six registers are:

- Input register — contains information at the pins
- Output register — contains output information
- Direction register — controls direction
- Interrupt flags — indicates if interrupt(s) are pending
- Interrupt edge select — contains input signal change necessary for interrupt
- Interrupt enable — contains interrupt enable pins

All six registers contain eight bits except for the interrupt flag register and the interrupt enable register. The two LSBs of the interrupt flag and interrupt enable registers are located in the special functions register (SFR). Three interrupt vectors are implemented, one for Port0.0, one for Port0.1, and one commonly used for any interrupt event on Port0.2, to Port0.7. The Port0.1 and Port0.2 pin function is shared with the 8-bit timer/counter.

LCD drive

Liquid crystal displays (LCDs) for static, 2-, 3- and 4-MUX operations can be driven directly. The controller LCD logic operation is defined by software using memory-bit manipulation. LCD memory is part of the LCD module, not part of data memory. Eight mode and control bits define the operation and current consumption of the LCD drive. The information for the individual digits can be easily obtained using table programming techniques combined with the correct addressing mode. The segment information is stored in LCD memory using instructions for memory manipulation.

The drive capability is mainly defined by the external resistor divider that supports the analog levels for 2-, 3- and 4-MUX operation. Groups of the LCD segment lines can be selected for digital output signals. The MSP430x32x configuration has four common signal lines and 21 segment lines.

A/D converter

The analog-to-digital converter (ADC) is a cascaded converter type that converts analog signals from V_{CC} to GND. It is a 12+2 bit converter with a software or automatically-controlled range select. Five inputs can be selected for analog or digital function. A ratiometric current source can be used on four of the analog pins. The current is adjusted by an external resistor and is enabled/disabled by bits located in the control registers. The conversion is started by setting the start-of-conversion bit (SOC) in the control register and the end-of-conversions sets the interrupt flag. The analog input signal is sampled starting with SOC during the next twelve MCLK clocks. The power-down bit in the control register controls the operating mode of the ADC peripheral. The current consumption and operation is stopped when it is set. The system reset PUC sets the power-down bit.

basic timer 1

The Basic Timer1 (BT1) divides the frequency of MCLK or ACLK, as selected with the SSEL bit, to provide low frequency control signals. This is done within the system by one central divider, the basic timer, to support low current applications. The BTCTL control register contains the flags which controls or selects the different

operational functions. When the supply voltage is applied or when a reset of the device (RST/NMI pin), a watchdog overflow, or a watchdog security key violation occurrs, all bits in the register hold undefined or unchanged status. The user software usually configures the operational conditions on the BT1 during initialization.

The basic timer has two 8-bit timers which can be cascaded to a 16-bit timer. Both timers can be read and written by software. Two bits in the SFR address range handle the system control interaction according to the function implemented in the basic timer. These two bits are the Basic Timer Interrupt Flag (BTIFG) and the Basic Timer Interrupt Enable (BTIE) bit.

watchdog timer

The primary function of the Watchdog Timer (WDT) module is to perform a controlled system restart after a software upset has occurred. If the selected time interval expires, a system reset is generated. If this watchdog function is not needed in an application, the module can work as an interval timer, which generates an interrupt after the selected time interval.

The watchdog timer counter (WDTCNT) is a 15/16-bit upcounter which is not directly accessible by software. The WDTCNT is controlled using the watchdog timer control register (WDTCTL), which is an 8-bit read/write register. Writing to WDTCTL, in both operating modes (watchdog or timer) is only possible by using the correct password in the high-byte. The low-byte stores data written to the WDTCTL. The high-byte password is 05Ah. If any value other than 05Ah is written to the high-byte of the WDTCTL, a system reset PUC is generated. *When the password is read its value is 069h that minimizes accidental write operations to the WDTCTL register.* A read-access to WDTCTL is only possible by writing 05Ah as the password in the high-byte of the WDTCTL. This avoids an accidental write-access on the WDTCTL. Additionally to the watchdog timer control bits, there are two bits included in the WDTCTL that configure the NMI pin.

8-bit timer/counter

The 8-bit interval timer supports three major functions for the application:

- Serial communication or data exchange
- Pulse counting or pulse accumulation
- Timer

The 8-bit Timer/Counter peripheral includes the following major blocks: an 8-bit Up-Counter with preload register, an 8-bit Control Register, an Input clock selector, an Edge detection (e.g. Start bit detection for asynchronous protocols), and an input and output data latch, triggered by the carry-out-signal from the 8-bit counter.

The 8-bit counter counts up with an input clock which is selected by two control bits from the control register. The four possible clock sources are MCLK, ACLK, the external signal from terminal P0.1, and the signal from the logical .AND. of MCLK and terminal P0.1.

Two counter inputs (load, enable) control the counter operation. The load input controls load operations. A write-access to the counter results in loading the content of the preload register into the counter. The software writes or reads the preload register with all instructions. The preload register acts as a buffer and can be written immediately after the load of the counter is completed. The enable input enables the count operation. When the enable signal is set to high, the counter will count-up each time a positive clock edge is applied to the clock input of the counter.

Serial protocols, like UART protocol, need start-bit edge-detection to determine, at the receiver, the start of a data transmission. When this function is activated, the counter starts counting after start-bit condition is detected. The first signal level is sampled into the RXD input data-latch after completing the first timing interval, which is programmed into the counter. Two latches are used for input and output data (RXD_FF and TXD_FF) are clocked by the counter after the programmed timing interval has elapsed.

uart

The serial communication is realized by using software and the 8-bit timer/counter hardware. The hardware supports the output of the serial data stream, bit-by-bit, with the timing determined by the counter. The software/hardware interface connects the mixed signal controller to external devices, systems, or networks.

timer/port

The timer/port module has two 8-bit counters, an input that triggers one counter, and six digital outputs with 3-state capability. Both counters have an independent clock-selector for selecting an external signal or one of the internal clocks (ACLK or MCLK). One of the counters has an extended control capability to halt, count continuously, or gate the counter by selecting one of two external signals. This gate signal sets the interrupt flag, if an external signal is selected and the gate stops the counter.

Both timers can be read from and written to by software. The two 8-bit counters can be cascaded to a 16-bit counter. A common interrupt vector is implemented. The interrupt flag can be set from three events in the 8-bit counter mode (gate signal, overflow from the counters) or from two events in the 16-bit counter mode (gate signal, overflow from the MSB of the cascaded counter).

absolute maximum ratings

Voltage applied at V_{CC} to V_{SS} . . . . . –0.3 V to + 6.0 V
Voltage applied to any pin (referenced to V_{SS}) . . . . . –0.3 V to V_{CC} + 0.3 V
Diode current at any device terminal . . . . . ± 2 mA
Storage Temperature, T_{stg} (unprogrammed device) . . . . . –55°C to 150°C
Storage Temperature, T_{stg} (programmed device) . . . . . –40°C to 85°C

operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (MSP430C323)		2.5		5.5	V
Supply voltage, V_{CC} (MSP430P/E325)		2.7		5.5	V
Supply Voltage, V_{SS}		0.0	0.0	0.0	V
Operating free-air temperature range, T_A	TMS430C32x, TMS430P32x	–40		85	°C
	PMS430E32x		25		
XTAL frequency, $f_{(XTAL)}$			32 768		Hz
Processor frequency (signal MCLK) $f_{(system)}$	V_{CC} = 3 V	DC		2.2	MHz
	V_{CC} = 5 V	DC		3.3	

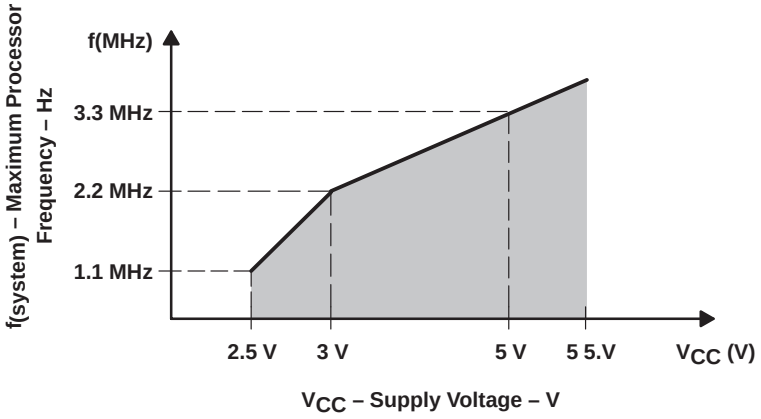


Figure 1. Frequency vs. Supply Voltage

electrical characteristics over recommended operating free-air temperature range temperature (unless otherwise noted)

supply current into $AV_{CC}+DV_{CC}$ excluding external current, f_{system} = 1 MHz

PARAMETER			TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active Mode, A/D conversion in power-down	C323	T_A = –40°C ..+85°C,	V_{CC} = 3 V		400	500	µA
			T_A = –40°C ..+85°C,	V_{CC} = 5 V		800	900	
		P325	T_A = –40°C ..+85°C,	V_{CC} = 3 V		3000	5000	
			T_A = –40°C ..+85°C,	V_{CC} = 5 V		10000	12000	
$I_{(CPUOff)}$	Low power mode, (LPM1)	C323	T_A = –40°C ..+85°C,	V_{CC} = 3 V		50	70	µA
			T_A = –40°C ..+85°C,	V_{CC} = 5 V		100	130	
		P325	T_A = –40°C ..+85°C,	V_{CC} = 3 V		70	110	
			T_A = –40°C ..+85°C,	V_{CC} = 5 V		150	200	
$I_{(LPM2)}$	Low power mode, (LPM2)		T_A = –40°C ..+85°C,	V_{CC} = 3 V		6	12	µA
			T_A = –40°C ..+85°C,	V_{CC} = 5 V		15	25	
$I_{(LPM3)}$	Low power mode, (LPM3)		T_A = –40°C	V_{CC} = 3 V		1.5	2.4	µA
			T_A = 25°C			1.3	2.0	
			T_A = 85°C			1.6	2.8	
			T_A = –40°C	V_{CC} = 5 V		5.2	7.0	
			T_A = 25°C			4.2	6.5	
			T_A = 85°C			4.0	7.0	
$I_{(LPM4)}$	Low power mode, (LPM4)		T_A = –40°C	V_{CC} = 3 V/5 V		0.1	0.8	µA
			T_A = 25°C			0.1	0.8	
			T_A = 85°C			0.4	1.3	

NOTE: All inputs are tied to 0V or V_{CC}. Outputs do not source or sink any current. The current consumption in LPM2, LPM3 and LPM4 are measured with active Basic Timer (ACLK selected) and LCD Module ($f_{(LCD)}$=1024Hz, 4MUX).

schmitt-trigger inputs Port 0, P0.x Timer/Port, CIN, TP 0.5

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3 V	1.2		2.1	V
		V_{CC} = 5 V	2.3		3.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 3 V	0.5		1.35	
		V_{CC} = 5 V	1.4		2.3	
$V_I–V_O$	Input-output voltage differential, (hysteresis)	V_{CC} = 3 V	0.3		1.0	
		V_{CC} = 5 V	0.6		1.4	

standard inputs TCK, TMS,TDI, Ax, RST/NMI

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{IL}	Low-level input voltage	V_{CC} = 3 V/5 V	V_{SS}		V_{SS}+0.8	V
V_{IH}	High-level input voltage		0.7V_{CC}		V_{CC}	

outputs Port 0, P0.x, Timer/port, TP 0.0..5, Sxx/Oxx, XBUF, (see Note 3)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = – 1.2 mA,	V_{CC} = 3 V	V_{CC}–0.4		V_{CC}	V
		$I_{(OHmax)}$ = – 1.5 mA,	V_{CC} = 5 V	V_{CC}–0.4		V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = + 1.2 mA,	V_{CC} = 3 V	V_{SS}		V_{SS}+0.4	
		$I_{(OLmax)}$ = + 1.5 mA,	V_{CC} = 5 V	V_{SS}		V_{SS}+0.4	

NOTE 3: The maximum total current for all outputs combined should not exceed ±9.6 mA to hold the maximum voltage drop specified.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

leakage current (see Note 4)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{lkg(LTP)}$	Leakage current , timer/port	Timer/Port: $V_{(TP0.x,CIN)}$ (see Note 5)	V_{CC} = 3 V/5 V			±50	nA
$I_{lkg(LP0x)}$	Leakage current , port 0	Port 0: $V_{(P0.x)}$ (see Note 6)	V_{CC} = 3/5 V			±50	nA
$I_{lkg(LS20)}$	Leakage current , S20	$V_{(S20)} = V_{SS}$ ... V_{CC}	V_{CC} = 3/5 V			±50	nA
$I_{lkg(LAx)}$	Leakage current , ADC	ADC: Ax, x= 0 .. 5, (see Note 7)	V_{CC} = 3/5 V			±30	nA
$I_{lkg(LR/N)}$	Leakage current , RST/NMI	RST/NMI	V_{CC} = 3/5 V			±50	nA

NOTES: 4. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
5. All Timer/Port pins TP0.0 to TP0.5 are Hi-Z. Pins CIN and TP.0 to TP0.5 are connected together during leakage current measurement. In the leakage measurement the input CIN is included. The input voltage is V_{SS} or V_{CC}.
6. The port pin must be selected for input and there must be no optional pull–up or pull–down resistor.
7. The input voltage is $V_{(IN)} = V_{SS}$ to V_{CC} , the current source is off, AEN.x bit is normally reset to stop throughput current flowing from V_{CC} to V_{SS} terminal.

optional resistors (see Note 8)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$R_{(opt1)}$	Resistors, individually programmable with ROM code, all port pins, values applicable for pull-down and pull-up	V_{CC} = 3 V/5 V	1.2	2.4	4.8	kΩ
$R_{(opt2)}$		V_{CC} = 3 V/5 V	1.8	3.6	7.2	kΩ
$R_{(opt3)}$		V_{CC} = 3 V/5 V	3.6	7.3	14.6	kΩ
$R_{(opt4)}$		V_{CC} = 3 V/5 V	5.5	11	22	kΩ
$R_{(opt5)}$		V_{CC} = 3 V/5 V	11	22	44	kΩ
$R_{(opt6)}$		V_{CC} = 3 V/5 V	22	44	88	kΩ
$R_{(opt7)}$		V_{CC} = 3 V/5 V	33	66	132	kΩ
$R_{(opt8)}$		V_{CC} = 3 V/5 V	55	110	220	kΩ
$R_{(opt9)}$		V_{CC} = 3 V/5 V	77	154	310	kΩ
$R_{(opt10)}$		V_{CC} = 3 V/5 V	100	200	400	kΩ

NOTE 8: Optional resistors $R_{(optx)}$ for pull-down or pull-up are not programmed in standard OTP/EPROM devices P/E 325.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

LCD

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$V_{O(HLCD)}$	Output 1 (HLCD)	$I_{(HLCD)}$ <= 10 nA,	V_{CC} = 3 V/5 V	V_{CC}–0.125		V_{CC}	V
$V_{O(LLCD)}$	Output 0 (LLCD)	$I_{(LLCD)}$ <= 10 nA,		V_{SS}		V_{SS}+0.125	
$I_{I(R03)}$	Input leakage	R03 = V_{SS}, No load at all seg and com pins	V_{CC} = 3 V/5 V			±20	nA
$I_{I(R13)}$		R13 = V_{CC} / 3, No load at all seg and com pins					
$I_{I(R23)}$		R23 = 2 V_{CC} / 3, No load at all seg and com pins					
$r_{o(Rx3\ to\ Sxx)}$	Resistance	$I_{(SXX)}$ = – 3 µA,	V_{CC} = 3 V/5 V			50	kΩ

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(comp)}$	Comparator (timer/port)	CPON = 1	V_{CC} = 3 V		250	350	µA
			V_{CC} = 5 V		450	600	µA
$V_{ref(comp)}$		CPON = 1	V_{CC} = 3 V/5 V	0.23×V_{CC}	0.25×V_{CC}	0.26×V_{CC}	
$V_{hys(comp)}$		CPON = 1	V_{CC} = 3 V		5	37	mV
			V_{CC} = 5 V		10	42	
$t_{(POR\_Delay)}$	POR		V_{CC} = 3 V/5 V		150	250	µs
$V_{(POR)}$				1.3		1.9	V
$V_{(min)}$				0		0.4	
$f_{(NOM)}$	DCO	NDC_0 = 20h, T_A = 25°C	V_{CC} = 3 V/5 V		1		MHz

wake–up LPM3

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$t_{(LPM3)}$	Delay time	f = 1 MHz	V_{CC} = 3 V			6	µs
			V_{CC} = 5 V				
		f = 2 MHz	V_{CC} = 3 V			6	
			V_{CC} = 5 V				
		f = 3 MHz	V_{CC} = 5 V			6	

ADC supply current ($f_{(ADCLK)}$ = 1.0 MHz)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$I_{(ADC)}$	ADC current	SV_{CC} on, current source off, V_{CC} = 3 V		200	400	µA
$I_{(ADC)}$		SV_{CC} on, current source off, V_{CC} = 5 V		300	740	µA

SV_{CC} (switched AV_{CC})

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$V_{(SVCC)}$		SV_{CC} on, $I_{(SVCC)}$ = –8 mA, V_{CC} = 2.5 V	V_{CC}–0.2 V		V_{CC}	V
$I_{(SVCC)}$		SV_{CC} off, SV_{CC} = 0 V, V_{CC} = 5 V			±0.1	µA
$Z_{(SVCC)}$	Input impedance	SV_{CC} off, V_{CC} = 3 V/5 V	40		100	kΩ

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

current source

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$V_{(Rext)}$	Voltage, (Rext)	$V_{(Rext)} = V_{(SVCC)} - V_{(RI)}$, $I_{(RI)}$ = 6 mA,	V_{CC} = 3 V/5 V,	0.246 × $V_{(SVCC)}$	0.249 × $V_{(SVCC)}$	0.252 × $V_{(SVCC)}$	V
$R_{(ext)}$	External resistor		V_{CC} = 3 V/5 V	95		1600	Ω
ΔI_S	Load compliance	VA0..A3 = 0 .. 0.4 × $V_{(SVCC)}$, $I_S = V_{(Rext)}/R_{(ext)}$ = 1 mA	V_{CC} = 3 V,	–1		1	µA
		VA0..A3 = 0 .. 0.4 × $V_{(SVCC)}$, $I_S = V_{(Rext)}/R_{(ext)}$ = 6 mA	V_{CC} = 3 V,	–3.2		3.2	µA
		VA0..A3 = 0 .. 0.5 × $V_{(SVCC)}$ $I_S = V_{(Rext)}/R_{(ext)}$= 1 mA	V_{CC} = 5 V,	–1.5		1.5	µA
		VA0..A3 = 0 .. 0.5 × $V_{(SVCC)}$ $I_S = V_{(Rext)}/R_{(ext)}$= 6 mA	V_{CC} = 5 V,	–3.2		3.2	µA
dN/dT†	Temperature stability	$V_{(Rext)}/R_{(ext)}$= 6mA, Range A	V_{CC} = 3 V/5 V,		0.008		LSB/°C
		Range B			0.015		
$dN/dV_{(SVCC)}$†	$V_{(SVCC)}$rejection ratio	Range A, B, $V_{(Rext)}/R_{(ext)}$ = 1 mA, SV_{CC} ± 10%	V_{CC} = 3 V/5 V,			1.25	LSB/V

† Non JEDEC symbol

A/D converter ($f_{(ADCLK)}$ = 1.0 MHz)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
	Resolution				12 + 2		bits
$f_{(con)}$	Conversion frequency	$f_{(con)} = f_{(ADCLK)}$ 12–bit conversion	V_{CC} = 3 V/5 V	0.1		1.5	MHz
		12+2-bit conversion		0.14		1.5	
$f_{(concyc)}$	Conversion cycles	$f_{(ADCLK)} = f_{(MCLK)}/N$ 12-bit conversion	V_{CC} = 3 V/5 V		96		cycles of ADCLK
		12+2-bit conversion			132		
Conversion offset 12 bit analog input to digital value (see Note 10)		Range A	V_{CC} = 3 V/ 5 V	–1.2	–0.49	0.24	% FSR_A (see Note 11)
		Range B	V_{CC} = 3 V/ 5 V	–1.7	–0.6	0.49	% FSR_B (see Note 11)
		Range C	V_{CC} = 3 V/ 5 V	–1.8	–0.6	0.6	% FSR_C (see Note 11)
		Range D	V_{CC} = 3 V/ 5 V	–1.7	0.6	0.49	% FSR_D (see Note 11)
Conversion offset 14 bit analog input to digital value (see Note 10)		Range ABCD	V_{CC} = 3 V/ 5 V	–0.27	–0.06	0.13	%FSR_{ABCD} (see Note 11)
Slope 12 bit			V_{CC} = 3 V/ 5 V	0.9925	1	1.0075	
Slope 14 bit			V_{CC} = 3 V/ 5 V	0.9982	1	1.0018	

NOTES: 9. AD-range limited to $0xxx_{16}$–$0xxxx_{16}$ by the comparator offset and Network offset.
10. Offset referred to full scale 12/14 bit
11. FSRx: full scale range, separate for the four 12-bit ranges and the 14-bit (12+2) range.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

A/D converter ($f_{(ADCLK)}$ = 1.0MHz)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
LSB Voltage			V_{CC} = 3 V/5 V		$0.000061 \times V_{SVCC}$		V
INL_1	Integral nonlinearity, See Note 12	0 ≤ DDV ≤ 127,	V_{CC} = 3 V/5 V	–2		2	LSB
INL_2		128 ≤ DDV ≤ 255,	V_{CC} = 3 V/5 V	–3		3	LSB
INL_3		256 ≤ DDV ≤ 2047,	V_{CC} = 3 V/5 V	–7		7	LSB
INL_4		2048 ≤ DDV ≤ 4095,	V_{CC} = 3 V/5 V	–10		10	LSB
DNL	Differential nonlinearity, See Note 13		V_{CC} = 3 V/5 V	–1		1	LSB
$C_{(IN)}$	Input capacitance		V_{CC} = 3 V/5 V		40	45	pF
$R_{(SIN)}$	Serial input resistance		V_{CC} = 3 V/5 V		2		kΩ

NOTES: 12. DDV is short form of Delta Digital Value. The DDV is a span of conversion results. It is assumed that the conversion is of 12 bit not 12+2 bit.
13. DNL is valid for all 12-bit ranges and the 14-(12+2)-bit range.

TYPICAL CHARACTERISTICS

DIGITAL CONTROLLED OSCILLATOR FREQUENCY vs TEMPERATURE

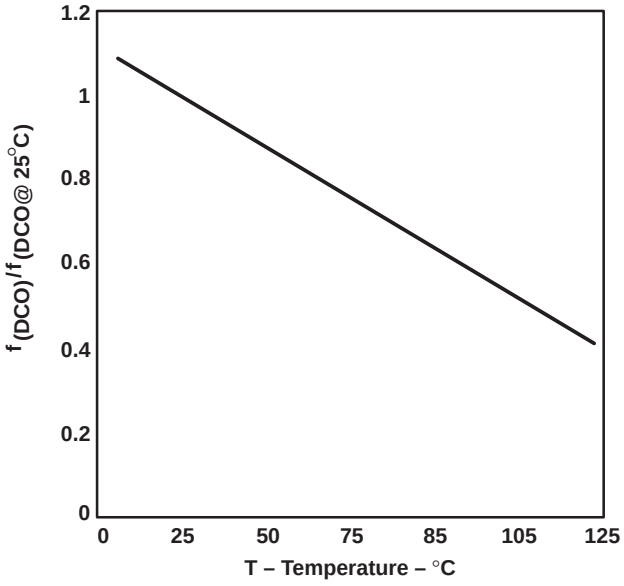


Figure 2

DIGITAL CONTROLLED OSCILLATOR FREQUENCY vs SUPPLY VOLTAGE

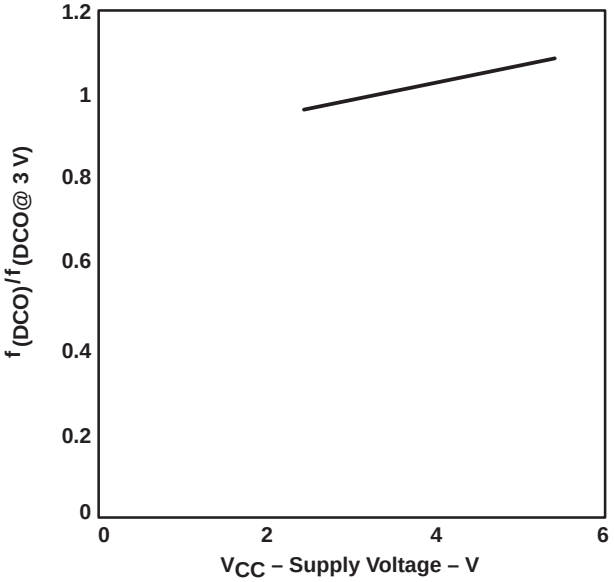
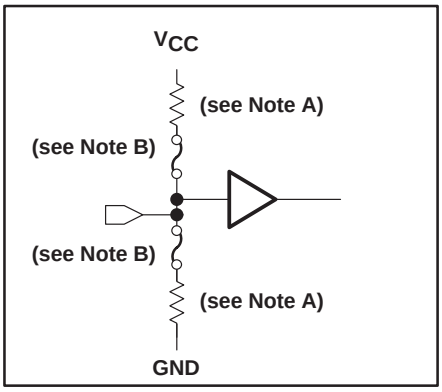
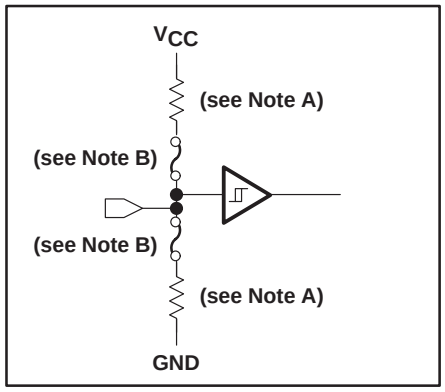


Figure 3

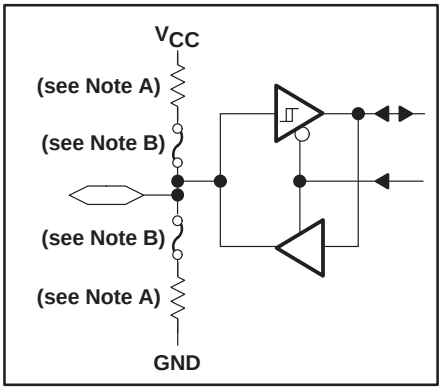
APPLICATION INFORMATION



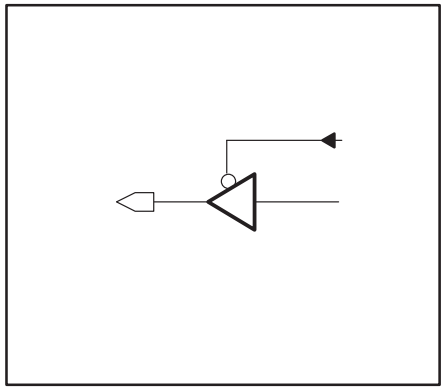
CMOS INPUT (RST/NMI)



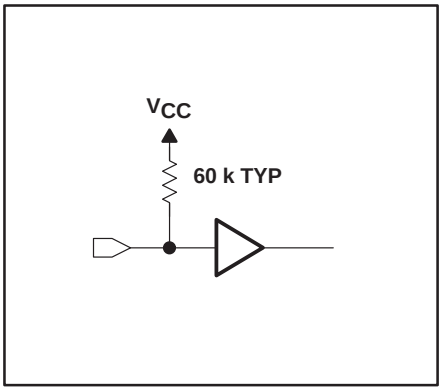
CMOS SCHMITT-TRIGGER INPUT (CIN)



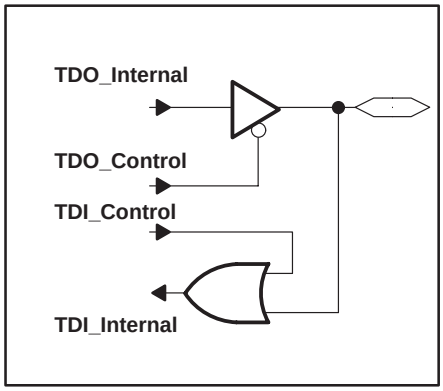
I/O WITH SCHMITT-TRIGGER INPUT (P0.x, TP5)



CMOS 3-STATE OUTPUT
(TP0–4, S2–18, S22, S23, S26, XBUF)



MSP430C32x: TMS, TCK, TDI
MSP430P/E32x: TMS, TCK



MSP430C32x: TDO/TDI
MSP430P/E32x: TDO/TDI

NOTES: A. Optional selection of pull-up or pull-down resistors with ROM (masked) versions. Anti-parallel diodes are connected between AV_{SS} and DV_{SS}.
B. Fuses for the optional pull-up and pull-down resistors can only be programmed at the factory.

APPLICATION INFORMATION

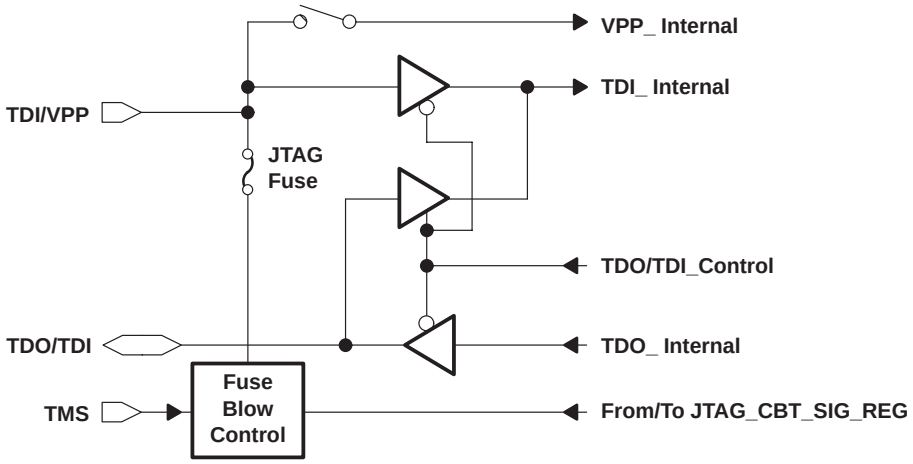


Figure 4. MSP430P325/E325: TDI/VPP, TDO/TDI

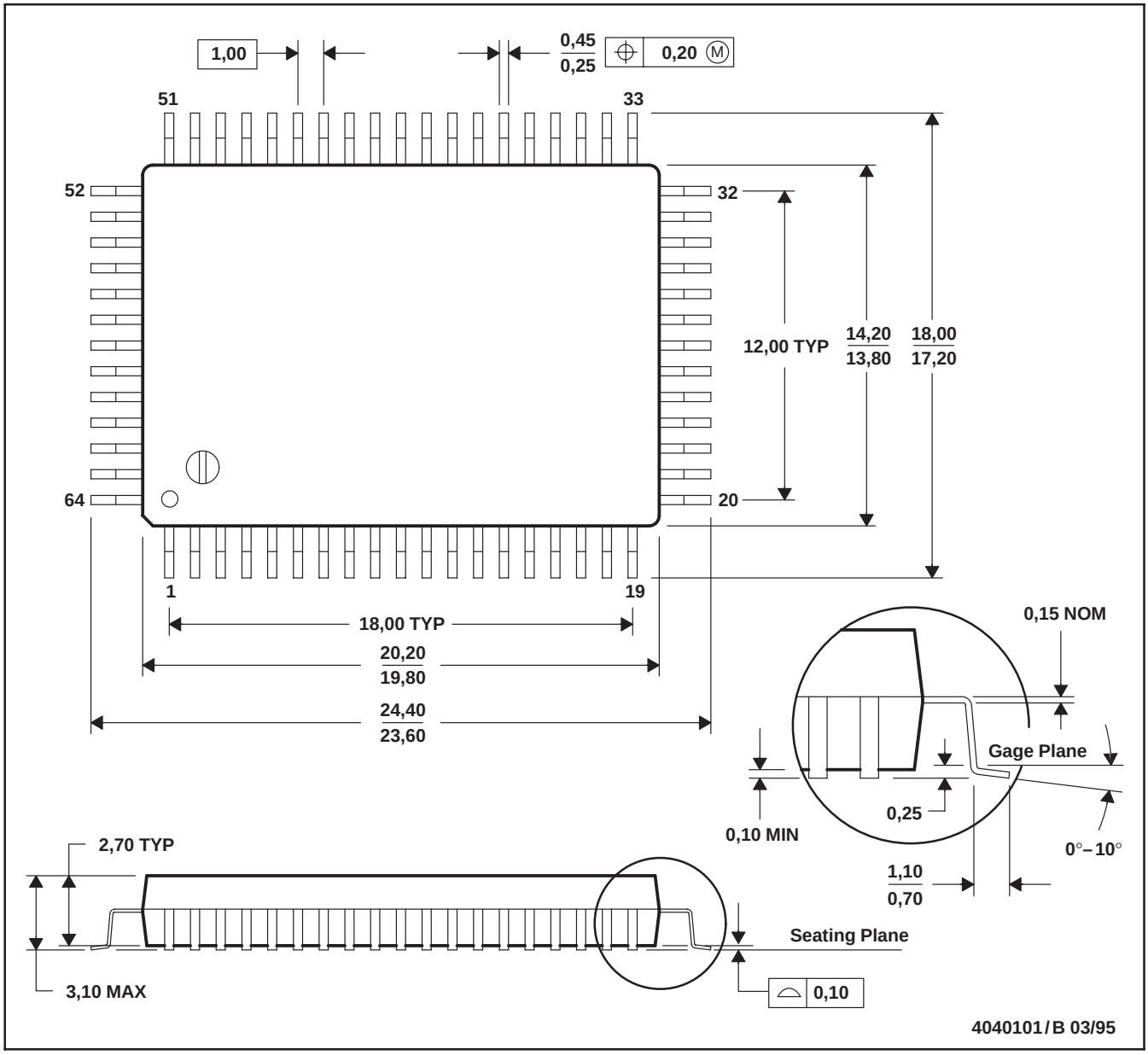
NOTES: A. During programming activity and when blowing the JTAG enable fuse, the TDI/VPP terminal is used to apply the correct voltage source. The TDO/TDI terminal is used to apply the test input data for JTAG circuitry.

B. The TDI/VPP terminal of the ’P325 and ’E325 does not have an internal pull-up resistor. An external pull-down resistor is recommended to avoid a floating node which could increase the current consumption of the device.

C. The TDO/TDI terminal is in a high-impedance state after POR. The ’P325 and ’E325 needs a pull-up or a pull-down resistor to avoid floating a node which could increase the current consumption of the device.

MECHANICAL DATA

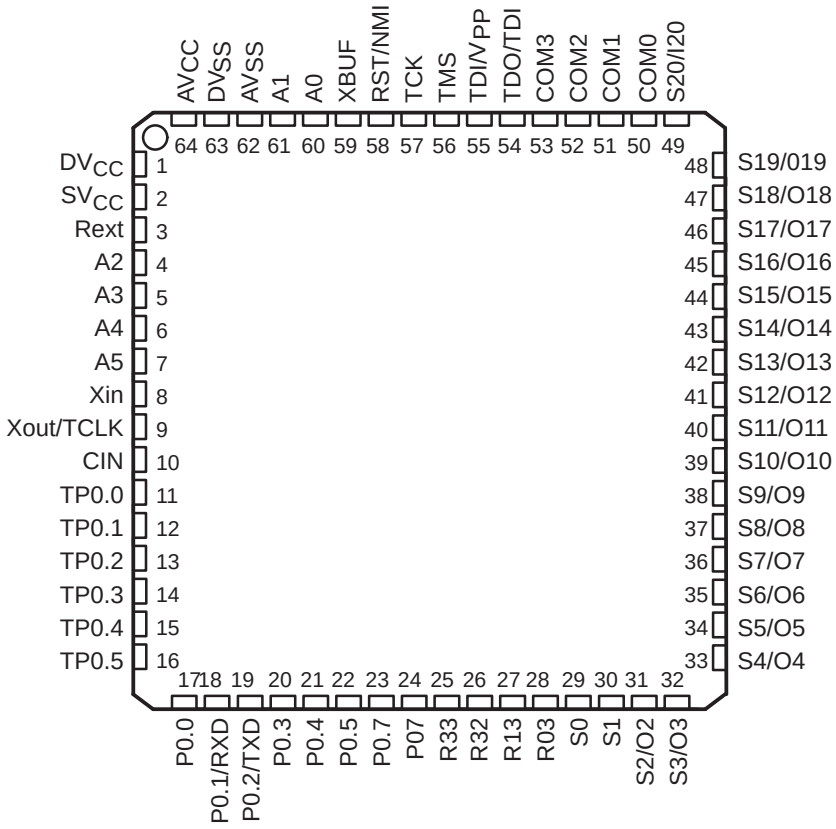
PG (R-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

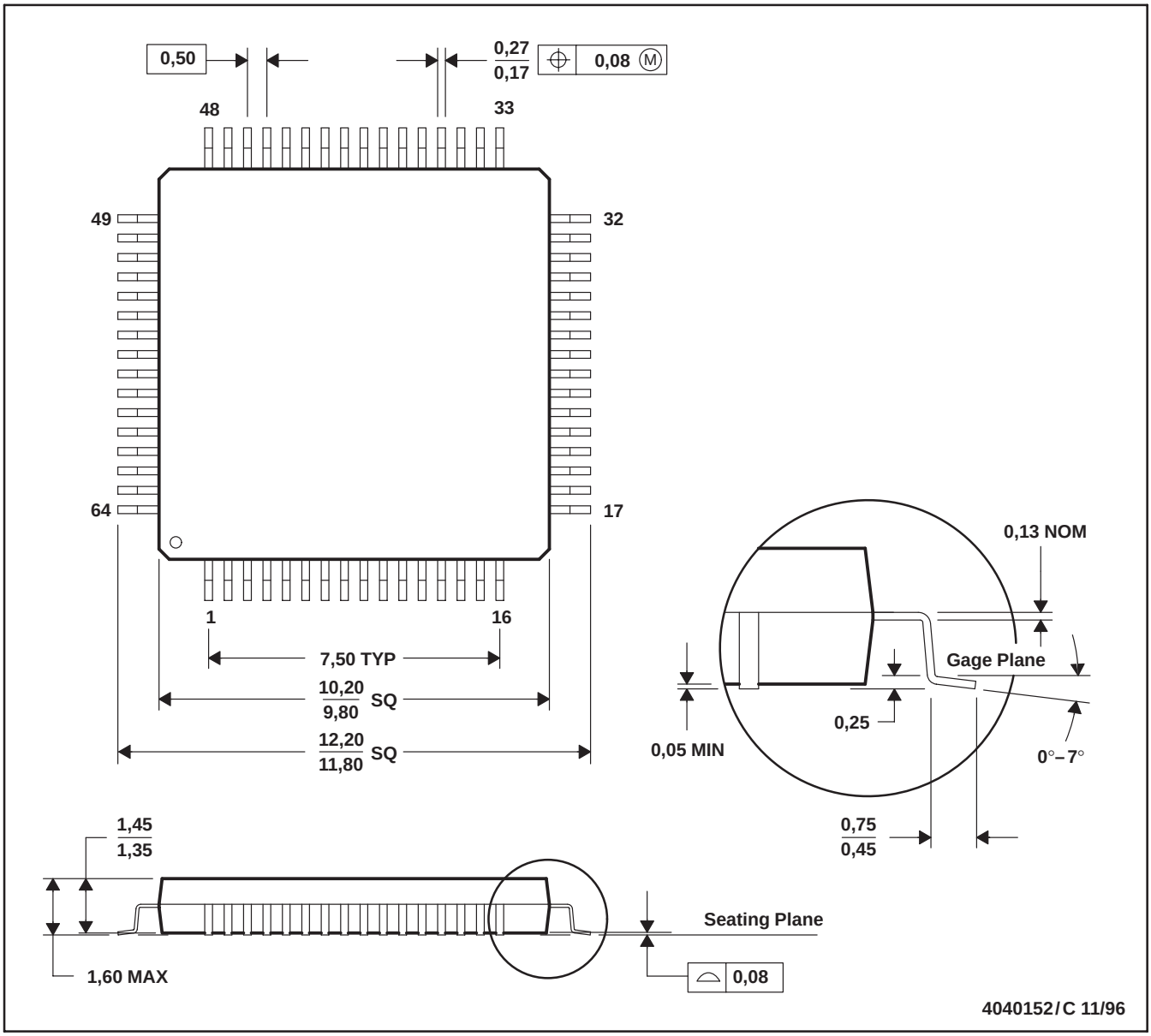
pinning MSP43C323, MSP430C325, MSP430P325 (PM package)

PM PACKAGE
(TOP VIEW)



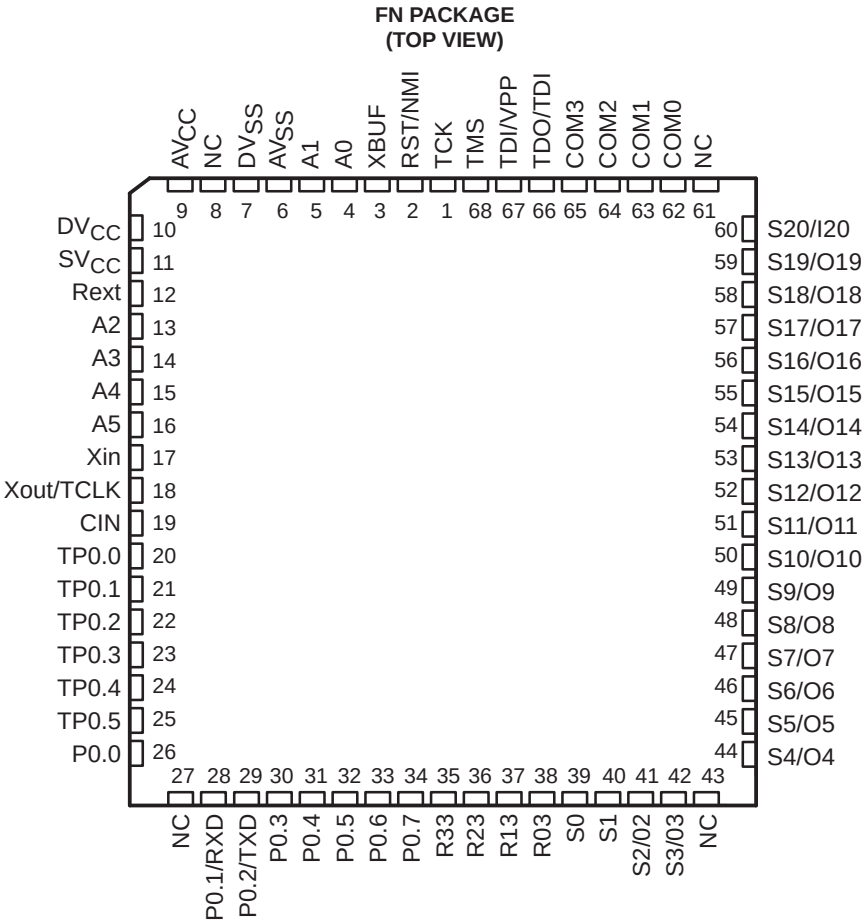
MECHANICAL DATA

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

pinning MSP43C323, MSP430C325, MSP430P325 (FN package)

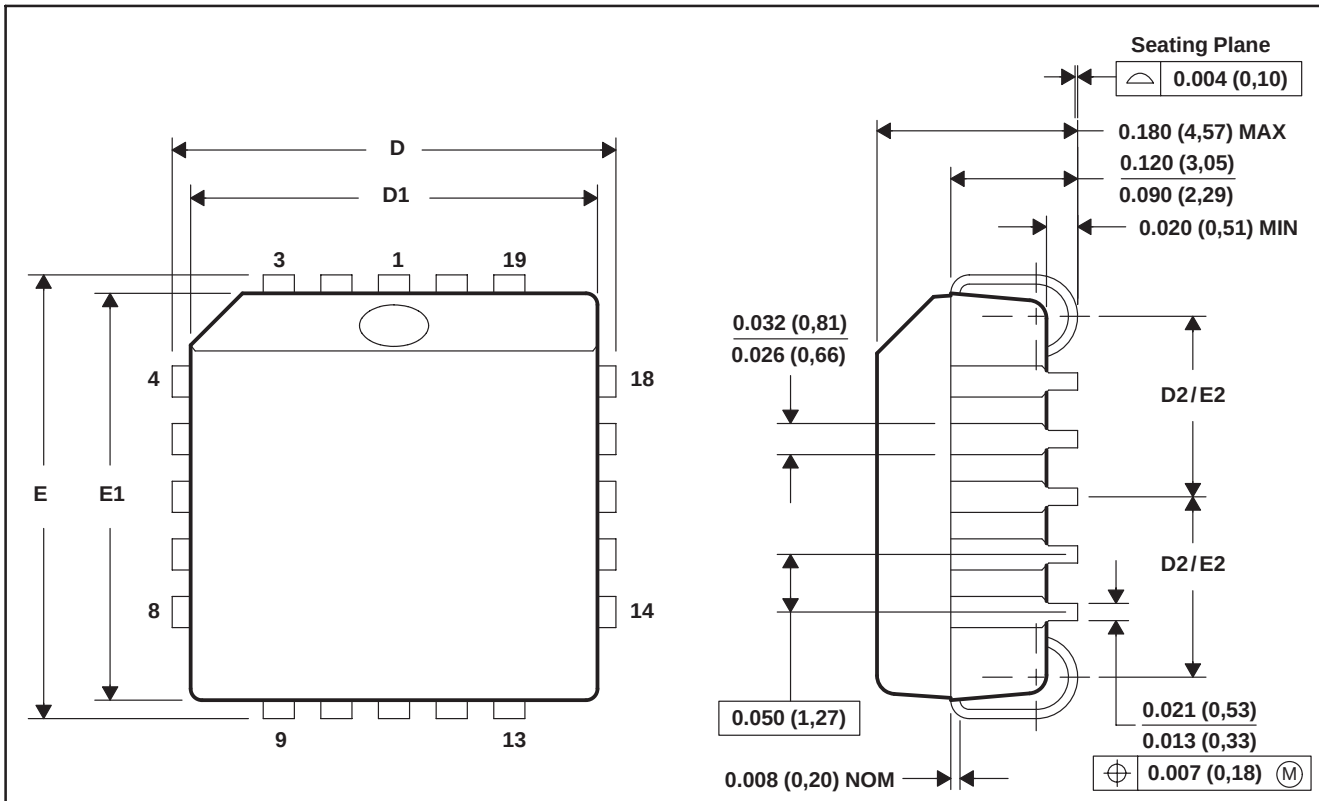


NC – No internal connection

MECHANICAL DATA

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



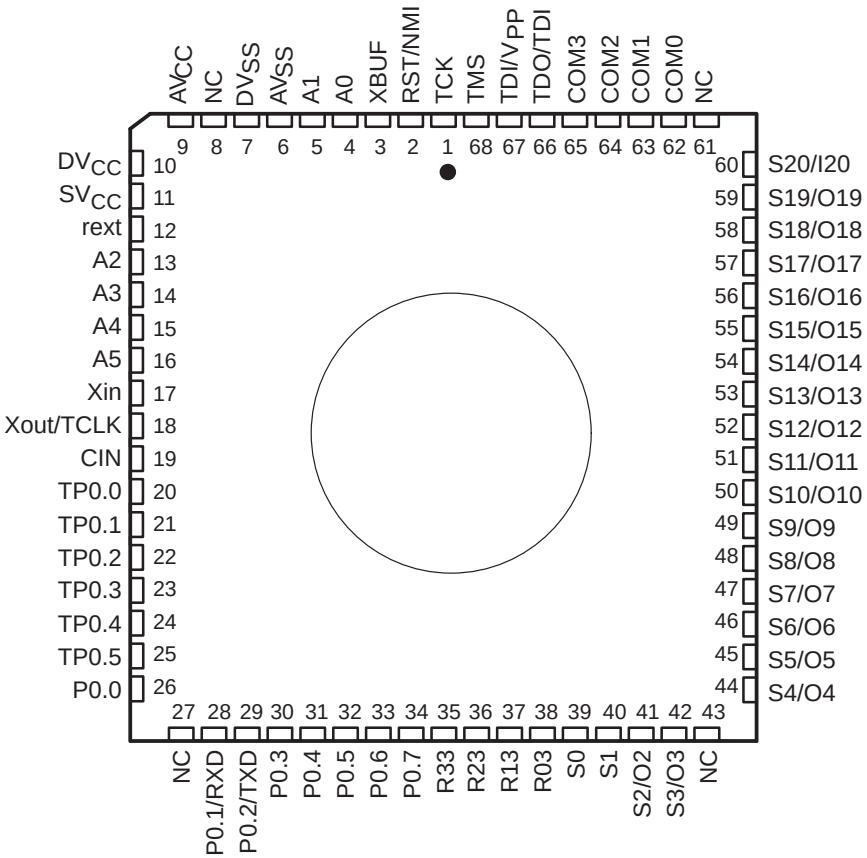
NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

pinning PMS430E325 (FZ package)

FZ PACKAGE
(TOP VIEW)

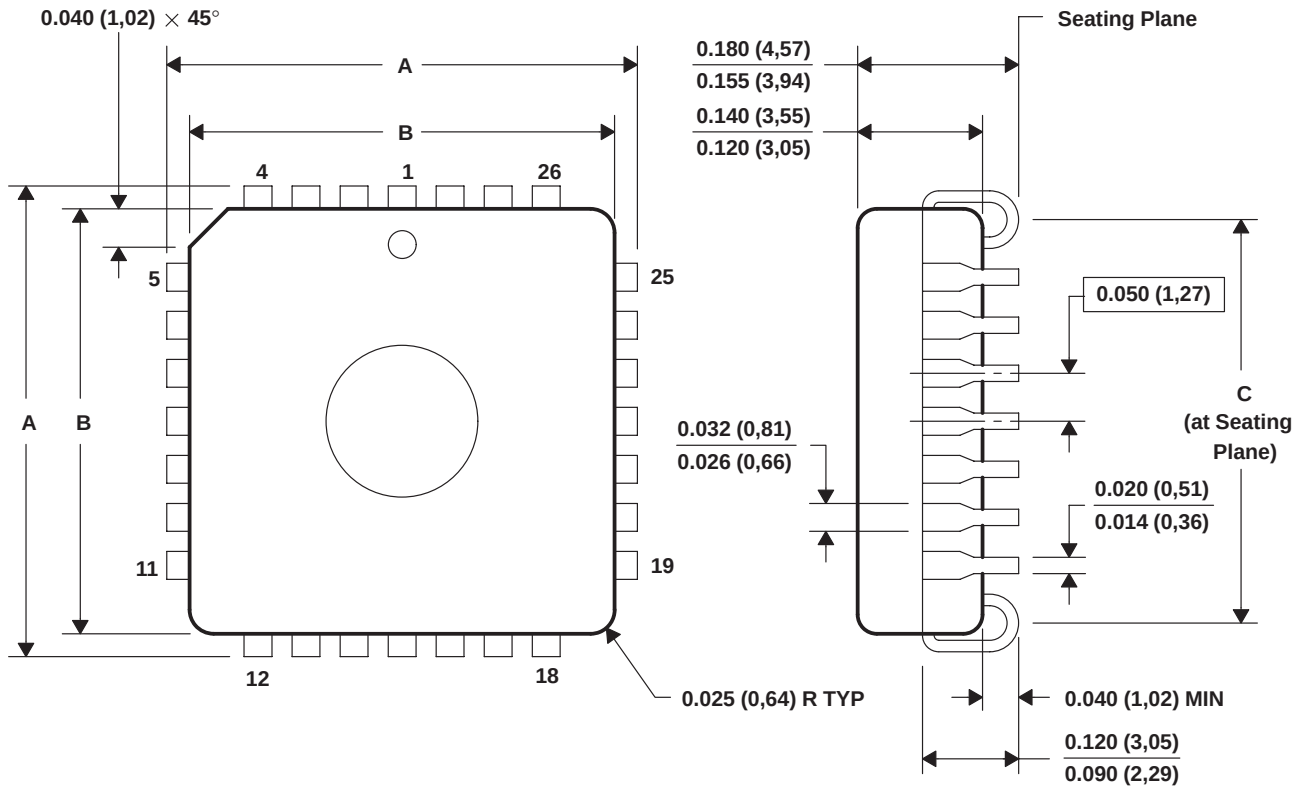


NC – No internal connection

MECHANICAL DATA

FZ (S-CQCC-J)** **J-LEADED CERAMIC CHIP CARRIER**

28 LEAD SHOWN



JEDEC OUTLINE	NO. OF PINS**	A		B		C	
		MIN	MAX	MIN	MAX	MIN	MAX
MO-087AA	28	0.485 (12,32)	0.495 (12,57)	0.430 (10,92)	0.455 (11,56)	0.410 (10,41)	0.430 (10,92)
MO-087AB	44	0.685 (17,40)	0.695 (17,65)	0.630 (16,00)	0.655 (16,64)	0.610 (15,49)	0.630 (16,00)
MO-087AC	52	0.785 (19,94)	0.795 (20,19)	0.730 (18,54)	0.765 (19,43)	0.680 (17,28)	0.740 (18,79)
MO-087AD	68	0.985 (25,02)	0.995 (25,27)	0.930 (23,62)	0.955 (24,26)	0.910 (23,11)	0.930 (23,62)

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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.

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