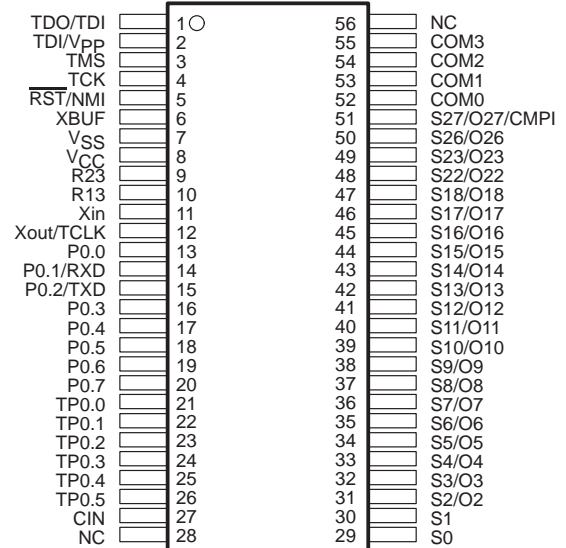
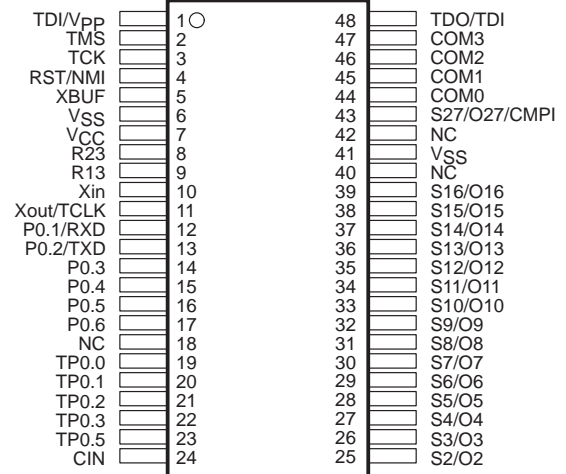


- Low Supply Voltage Range 2.5 V – 5.5 V
- Ultra-Low Power Consumption
- Low Operation Current, 400 μ A at 1 MHz, 3 V
- Five Power Saving Modes: (Standby Mode: 1.3 μ A, Off Mode: 0.1 μ A)
- Wakeup From Standby Mode in 6 μ s Maximum
- 16-Bit RISC Architecture, 300 ns Instruction Cycle Time
- Single Common 32 kHz Crystal, Internal System Clock up to 3.3 MHz
- Integrated LCD Driver for Up to 64 or 92 Segments
- Slope A/D Converter With External Components
- Serial Onboard Programming
- Program Code Protection by Security Fuse
- Family Members Include:
 - MSP430C311S: 2k Byte ROM, 128 Byte RAM
 - MSP430C312: 4k Byte ROM, 256 Byte RAM
 - MSP430C313: 8k Byte ROM, 256 Byte RAM
 - MSP430C314: 12k Byte ROM, 512 Byte RAM
 - MSP430C315: 16k Byte ROM, 512 Byte RAM
 - MSP430P313: 8k Byte OTP, 256 Byte RAM
 - MSP430P315: 16k Byte OTP, 512 Byte RAM
 - MSP430P315S: 16k Byte OTP, 512 Byte RAM
- EPROM Version Available for Prototyping : PMS430E313FZ, PMS430E315FZ
- Available in: 56-Pin Plastic Small-Outline Package (SSOP), 48-Pin SSOP (MSP430C311S, MSP430P315S), 68-Pin J-Leaded Ceramic Chip Carrier (JLCC) Package (EPROM Only)

**DL PACKAGE
(56-PIN TOP VIEW)**



**DL PACKAGE
(48-PIN TOP VIEW)**



NC – No internal connection

description

The Texas Instruments MSP430 series is a ultra low-power microcontroller family consisting of several devices that feature different sets of modules targeted to various applications. The microcontroller is designed to be battery operated for an extended application lifetime. With 16-bit RISC architecture, 16 bit integrated registers on the CPU, and the constant generator, the MSP430 achieves maximum code efficiency. The digitally-controlled oscillator, together with the frequency-locked-loop (FLL), provides a fast wakeup from a low-power mode to active mode in less than 6 μ s.

Typical applications include sensor systems that capture analog signals, converting them to digital values, and then processes the data and displays them or transmits them to a host system. The Timer/Port module provides dual- and single-slope A/D conversion capability for resistive sensors.

MSP430x31x MIXED SIGNAL MICROCONTROLLERS

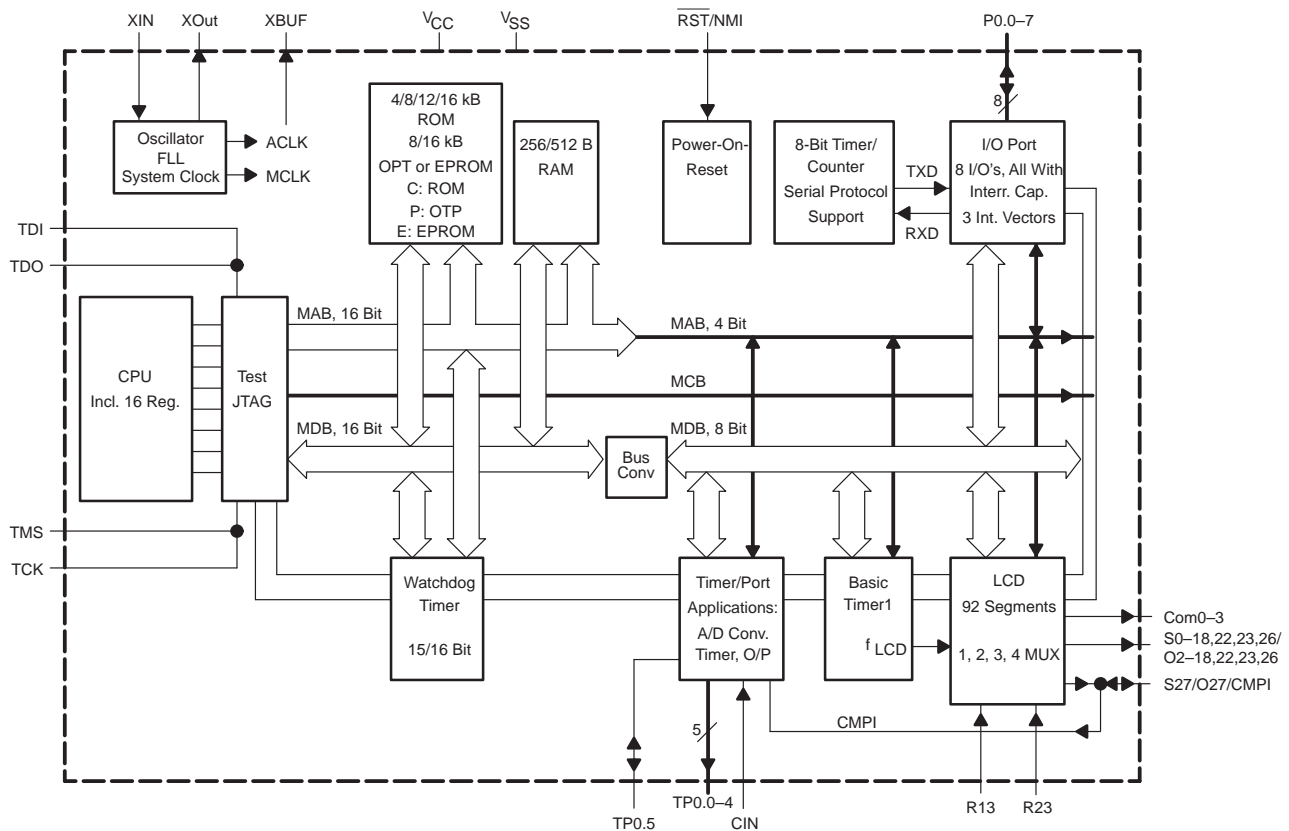
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AVAILABLE OPTIONS

T _A	PACKAGED DEVICES		
	SSOP 48-Pin (DL)	SSOP 56-Pin (DL)	JLCC 68-Pin (FZ)
-40°C to 85°C	MSP430C311SIDL MSP430P315SIDL	MSP430C312IDL MSP430C313IDL MSP430C314IDL MSP430C315IDL MSP430P313IDL MSP430P315IDL	
25°C	—	—	PMS430E313FZ PMS430E315FZ

functional block diagram

MSP430C312,313,314,315 and MSP430P313,315 and PMS430E313,315



Terminal Functions

MSP430C112, MSP430C313, MSP430C314, MSP430C315, MSP430P313, MSP430P315

56-pin SSOP package

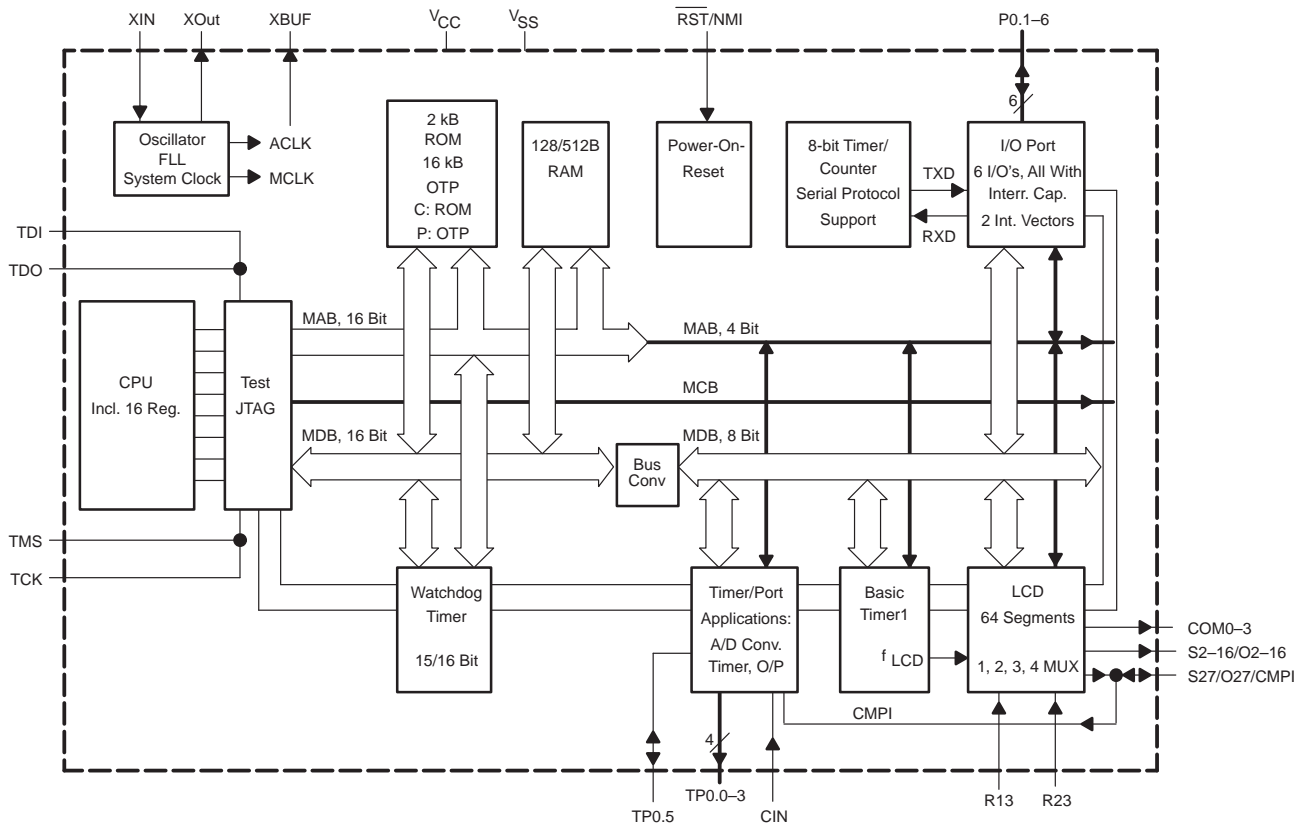
TERMINAL NAME	NO.	I/O	DESCRIPTION
CIN	27	I	Counter enable. CIN input enables counter (TPCNT1) (Timer/Port).
COM0 – COM3	52–55	O	Common output pins. COM0 – COM3 are used for LCD back planes.
P0.0	13	I/O	General-purpose digital I/O pin
P0.1/RXD	14	I/O	General-purpose digital I/O pin, receive data input port – 8-bit (Timer/Counter)
P0.2/TXD	15	I/O	General-purpose digital I/O pin, transmit data output port – 8-bit (Timer/Counter)
P0.3 – P0.7	16–20	I/O	Five general-purpose digital I/O pins, bit 3–7
R23	9	I	Input of second positive analog LCD level (V2) (LCD)
R13	10	I	Input of third positive analog LCD level (V3 of V4) (LCD)
RST/NMI	5	I	Reset input or nonmaskable interrupt input
S0	29	O	Segment line S0 (LCD)
S1	30	O	Segment line S1 (LCD)
S2/O2 – S5/O5	31–34	O	Segment lines (S2 to S5) or digital output port O2 to O5, group 1 (LCD)
S6/O6 – S9/O9	35–38	O	Segment lines (S6 to S9) or digital output port O6 to O9, group 2 (LCD)
S10/O10 – S13/O13	39–42	O	Segment lines (S10 to S13) or digital output port O10 to O13, group 3 (LCD)
S14/O14 – S17/O17	43–46	O	Segment lines (S14 to S17) or digital output port O14 to O17, group 4 (LCD)
S18/O18	47	O	Segment line (S18) or digital output port O18, group 5 (LCD)
S22/O22 – S23/O23	48,49	O	Segment lines (S22 to S23) or digital output port O22 to O23, group 6 (LCD)
S26/O26	50	O	Segment line (S26) or digital output port O26, group 7 (LCD)
S27/O27/CMPI	51	I/O	Segment line (S27) or digital output port O27, can be used as a comparator input port CMPI (Timer/Port)
TCK	4	I	Test clock. TCK is a clock input terminal for device programming and test.
TDI/VPP	2	I	Test data input port. TDI/VPP is used as a data input terminal or an input for programming voltage.
TDO/TDI	1	I/O	Test data output port. TDO/TDI is used as a data output terminal or as a data input during programming.
TMS	3	I	Test mode select. TMS is an input terminal for device programming and test.
TP0.0	21	O	General-purpose 3-state digital output port, bit 0 (Timer/Port)
TP0.1	22	O	General-purpose 3-state digital output port, bit 1 (Timer/Port)
TP0.2	23	O	General-purpose 3-state digital output port, bit 2 (Timer/Port)
TP0.3	24	O	General-purpose 3-state digital output port, bit 3 (Timer/Port)
TP0.4	25	O	General-purpose 3-state digital output port, bit 4 (Timer/Port)
TP0.5	26	I/O	General-purpose 3-state digital I/O pin, bit 5 (Timer/Port)
V _{CC}	8		Supply voltage
V _{SS}	7		Ground reference
XBUF	6	O	Clock signal output of system clock (MCLK) or crystal clock (ACLK)
Xin	11	I	Input terminal of crystal oscillator
Xout/TCLK	12	I/O	Output terminal of crystal oscillator or test clock input

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functional block diagram

MSP430C311S and MSP430P315S



Terminal Functions

MSP430C311S, MSP430P315S

48-pin SSOP package

TERMINAL NAME	NO.	I/O	DESCRIPTION
CIN	24	I	Counter enable. CIN input enables counter (TPCNT1) (Timer/Port).
COM0 – COM3	44–47	O	Common output pins, COM0 – COM3 are used for LCD back planes.
P0.1/RXD	12	I/O	General-purpose digital I/O pin, receive data input port – 8-bit (Timer/Counter)
P0.2/TXD	13	I/O	General-purpose digital I/O pin, transmit data output port – 8-bit (Timer/Counter)
P0.3	14	I/O	General-purpose digital I/O pins, bit 3
P0.4	15	I/O	General-purpose digital I/O pins, bit 4
P0.5	16	I/O	General-purpose digital I/O pins, bit 5
P0.6	17	I/O	General-purpose digital I/O pins, bit 6
R23	8	I	Input of second positive analog LCD level (V2) (LCD)
R13	9	I	Input of third positive analog LCD level (V3 of V4) (LCD)
RST/NMI	4	I	Reset input or nonmaskable interrupt input
S2/O2 – S5/O5	25–28	O	Segment lines (S2 to S5) or digital output port O2 to O5, group 1 (LCD)
S6/O6 – S9/O9	29–32	O	Segment lines (S6 to S9) or digital output port O6 to O9, group 2 (LCD)
S10/O10 – S13/O13	33–36	O	Segment lines (S10 to S13) or digital output port O10 to O13, group 3 (LCD)
S14/O14 – S16/O16	37–39	O	Segment lines (S14 to S17) or digital output port O14 to O17, group 4 (LCD)
S27/O27/CMPI	43	I/O	Segment line (S27) or digital output port O27, can be used as a comparator input port CMPI (Timer/Port)
TCK	3	I	Test clock. TCK is a clock input terminal for device programming and test.
TDI/VPP	1	I	Test data input port. TDI/VPP is used as a data input terminal or an input for programming voltage.
TDO/TDI	48	I/O	Test data output port. TDO/TDI is used as a data output terminal or as a data input during programming.
TMS	2	I	Test mode select. TMS is an input terminal for device programming and test.
TP0.0	19	O	General-purpose 3-state digital output port, bit 0 (Timer/Port)
TP0.1	20	O	General-purpose 3-state digital output port, bit 1 (Timer/Port)
TP0.2	21	O	General-purpose 3-state digital output port, bit 2 (Timer/Port)
TP0.3	22	O	General-purpose 3-state digital output port, bit 3 (Timer/Port)
TP0.5	23	I/O	General-purpose 3-state digital I/O pin, bit 5 (Timer/Port)
V _{CC}	7		Supply voltage
VSS	6, 41		Ground references
XBUF	5	O	Clock signal output of system clock (MCLK) or crystal clock (ACLK)
Xin	10	I	Input terminal of crystal oscillator
Xout/TCLK	11	I/O	Output terminal of crystal oscillator or test clock input

MSP430x31x MIXED SIGNAL MICROCONTROLLERS

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short-form description

processing unit

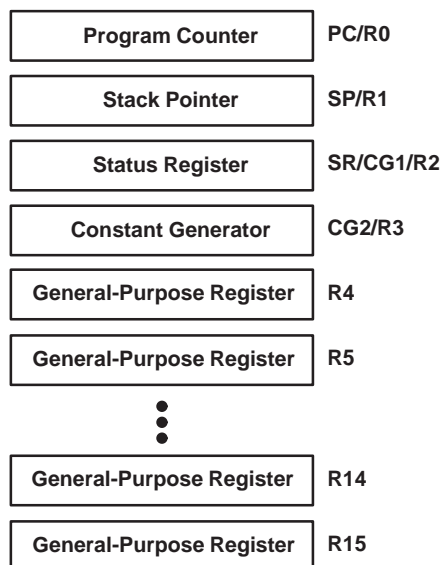
The processing unit is based on a consistent, and orthogonal designed CPU and instruction set. This design structure results in a RISC-like architecture, highly transparent to the application development and is distinguished due to ease of programming. All operations other than program-flow instructions are consequently performed as register operations in conjunction with seven addressing modes for source and four modes for destination operand.

CPU

Sixteen registers located inside the CPU provide reduced instruction execution time. This reduces a register-register operation execution time to one cycle of the processor frequency.

Four registers are reserved for special use as a program counter, a stack pointer, a status register, and a constant generator. The remaining ones are available as general-purpose registers.

Peripherals connected to the CPU using a data address and control bus can be handled easily with all instructions for memory manipulation.



instruction set

The instructions set for this register-register architecture provides a powerful and easy-to-use assembly language. The instruction set consists of 52 instructions with three formats and seven addressing modes. Table 1 provides a summation and example of the three types of instruction formats; the addressing modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4, R5	R4 + R5 → R5
Single operands, destination only	e.g. CALL R8	PC → (TOS), R8 → PC
Relative jump, un-/conditional	e.g. JNE	Jump-on equal bit = 0

Each instruction that operates on word and byte data is identified by the suffix B.

Examples:	Instructions for word operation	Instructions for byte operation
	MOV EDE,TONI	MOV.B EDE,TONI
	ADD #235h,&MEM	ADD.B #35h,&MEM
	PUSH R5	PUSH.B R5
	SWPB R5	—



Table 2. Address Mode Descriptions

ADDRESS MODE	s	d	SYNTAX	EXAMPLE	OPERATION
Register	√	√	MOV Rs, Rd	MOV R10, R11	R10 → R11
Indexed	√	√	MOV X(Rn), Y(Rm)	MOV 2(R5), 6(R6)	M(2 + R5) → M(6 + R6)
Symbolic (PC relative)	√	√	MOV EDE, TONI		M(EDE) → M(TONI)
Absolute	√	√	MOV &MEM, &TCDAT		M(MEM) → M(TCDAT)
Indirect	√		MOV @Rn, Y(Rm)	MOV @R10, Tab(R6)	M(R10) → M(Tab + R6)
Indirect autoincrement	√		MOV @Rn+, RM	MOV @R10+, R11	M(R10) → R11, R10 + 2 → R10
Immediate	√		MOV #X, TONI	MOV #45, TONI	#45 → M(TONI)

NOTE: s = source d = destination

Computed branches (BR) and subroutine calls (CALL) instructions use the same addressing modes as the other instructions. These addressing modes provide *indirect* addressing, ideally suited for computed branches and calls. The full use of this programming capability permits a program structure different from conventional 8- and 16-bit controllers. For example, numerous routines can easily be designed to deal with pointers and stacks instead of using Flag type programs for flow control.

operation modes and interrupts

The MSP430 operating modes support various advanced requirements for ultra-low power and ultra-low energy consumption. This is achieved by the intelligent management of the operations during the different module operation modes and CPU states. The requirements are fully supported during interrupt event handling. An interrupt event awakens the system from each of the various operating modes and returns with the RETI instruction to the mode that was selected before the interrupt event. The clocks used are ACLK and MCLK. ACLK is the crystal frequency and MCLK, a multiple of ACLK, is used as the system clock.

The software can configure five operating modes:

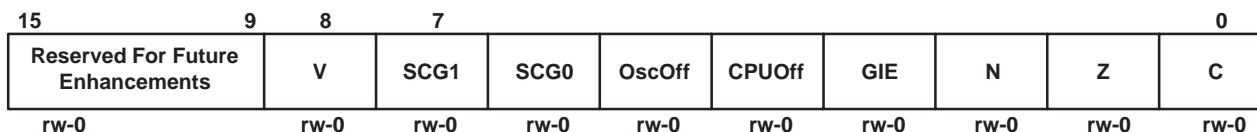
- Active mode (AM). The CPU is enabled with different combinations of active peripheral modules.
- Low power mode 0 (LPM0). The CPU is disabled, peripheral operation continues, ACLK and MCLK signals are active, and loop control for MCLK is active.
- Low power mode 1 (LPM1). The CPU is disabled, peripheral operation continues, ACLK and MCLK signals are active, and loop control for MCLK is inactive.
- Low power mode 2 (LPM2). The CPU is disabled, peripheral operation continues, ACLK signal is active, and MCLK and loop control for MCLK are inactive.
- Low power mode 3 (LPM3). The CPU is disabled, peripheral operation continues, ACLK signal is active, MCLK and loop control for MCLK are inactive, and the dc generator for the digital controlled oscillator (DCO) (→MCLK generator) is switched off.
- Low power mode 4 (LPM4). The CPU is disabled, peripheral operation continues, ACLK signal is inactive (crystal oscillator stopped), MCLK and loop control for MCLK are inactive, and the dc generator for the DCO is switched off.

The special function registers (SFR) include module-enable bits that stop or enable the operation of the specific peripheral module. All registers of the peripherals may be accessed if the operational function is stopped or enabled. However, some peripheral current-saving functions are accessed through the state of local register bits. An example is the enable/disable of the analog voltage generator in the LCD peripheral, which is turned on or off using one register bit.

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The most general bits that influence current consumption and support fast turn-on from low power operating modes are located in the status register (SR). Four of these bits control the CPU and the system clock generator: SCG1, SCG0, OscOff, and CPUOff.



interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the ROM with an address range of 0FFFFh-0FFE0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up, external reset, watchdog	RSTI, WDI (see Note1)	Reset	0FFFEh	15, highest
NMI, oscillator fault	NMIIFG, OFIFG (see Note 1)	Non-maskable, (Non)-maskable	0FFFCh	14
Dedicated I/O P0.0	P0.0IFG	Maskable	0FFFAh	13
Dedicated I/O P0.1 or 8-bit Timer/counter	P0.1IFG	Maskable	0FFF8h	12
			0FFF6h	11
Watchdog timer	WDTIFG	Maskable	0FFF4h	10
			0FFF2h	9
			0FFF0h	8
			0FFEEh	7
			0FFEC	6
Timer/port	See Note 2	Maskable	0FFEAh	5
			0FFE8h	4
			0FFE6h	3
			0FFE4h	2
Basic timer 1	BTIFG	Maskable	0FFE2h	1
I/O Port 0.2–7	P0.27IFG (see Note 1)	Maskable	0FFE0h	0, lowest

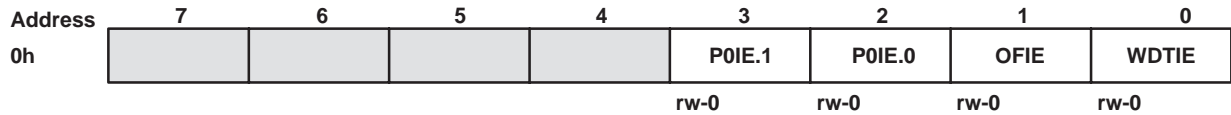
- NOTES: 1. Multiple source flags
2. Timer/port interrupt flags are located in the timer/port registers



special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits that are not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

interrupt enable 1 and 2

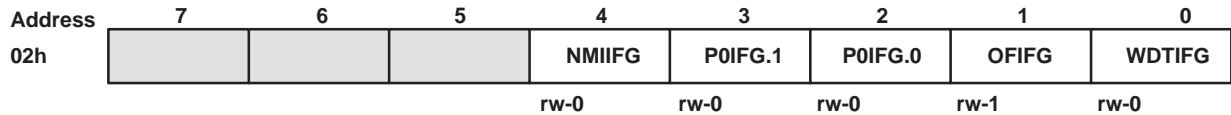


- WDTIE: Watchdog timer enable signal
- OFIE: Oscillator fault enable signal
- P0IE.0: Dedicated I/O P0.0
- P0IE.1: P0.1 or 8-bit timer/counter, RXD

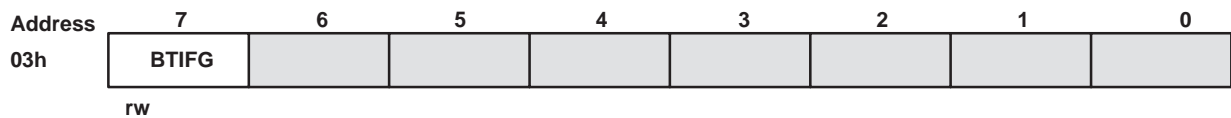


- TPIE: Timer/port enable signal
- BTIE: Basic timer enable signal

interrupt flag register 1 and 2



- WDTIFG: Set on overflow or security key violation
OR
Reset on V_{CC} power-on or reset condition at RST/NMI-pin
- OFIFG: Flag set on oscillator fault
- P0.0IFG: Dedicated I/O P0.0
- P0.1IFG: P0.1 or 8-bit Timer/Counter, RXD
- NMIIFG: Signal at RST/NMI-pin

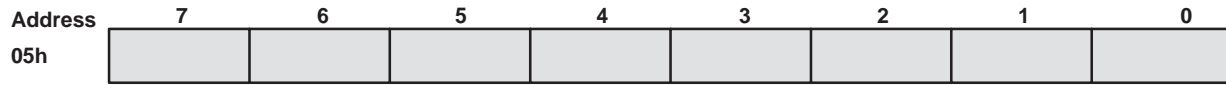
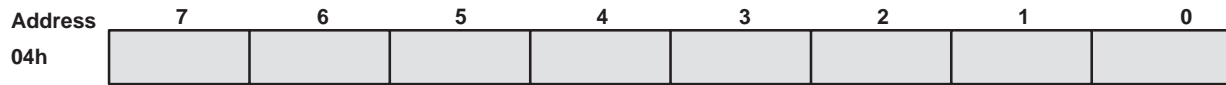


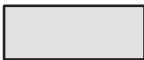
- BTIFG: Basic timer flag

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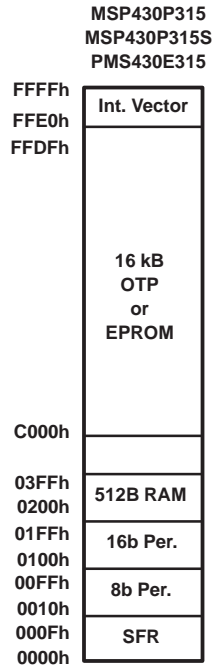
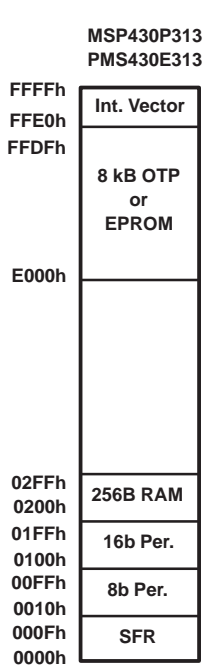
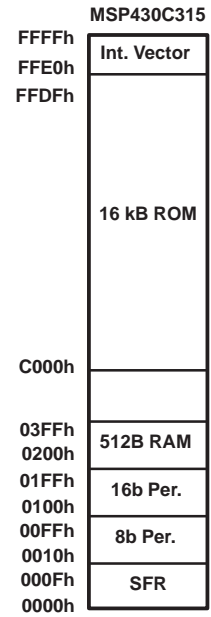
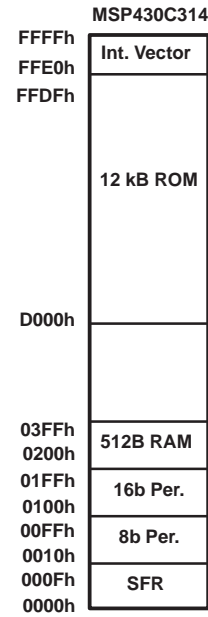
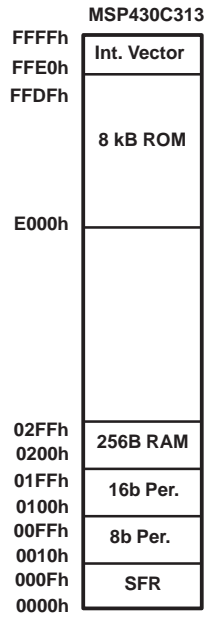
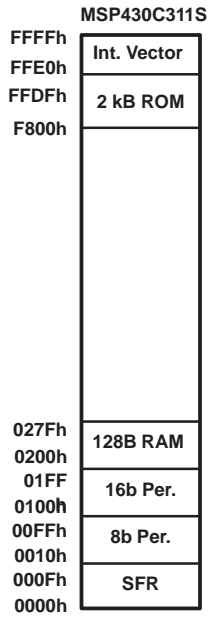
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module enable register 1 and 2



Legend **rw:** Bit can be read and written.
 rw-0: Bit can be read and written. It is reset by PUC
  SFR bit is not present in device.

memory organization



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peripherals

Peripherals connected to the CPU through a data, address, and control busses can be handled easily with instructions for memory manipulation.

oscillator and system clock

Two clocks are used in the system, the system (master) clock (MCLK) and the auxiliary clock (ACLK). The MCLK is a multiple of the ACLK. The ACLK runs with the crystal oscillator frequency. The special design of the oscillator supports the feature of low current consumption and the use of a 32 768 Hz crystal. The crystal is connected across two terminals without any other external components being required.

The oscillator starts after applying VCC, due to a reset of the control bit (OscOff) in the status register (SR). It can be stopped by setting the OscOff bit to a 1. The enabled clock signals ACLK, ACLK/2, ACLK/4, OR MCLK are accessible for use by external devices at output terminal XBUF.

The controller system clock has to operate with different requirements according to the application and system conditions. Requirements include:

- High frequency in order to react quickly to system hardware requests or events
- Low frequency in order to minimize current consumption, EMI, etc.
- Stable frequency for timer applications e.g. real-time clock (RTC)
- Enable start-stop operation with a minimum of delay.

These requirements cannot all be met with fast frequency high-Q crystals or with RC-type low-Q oscillators. The compromise selected for the MSP430 uses a low-crystal frequency, which is multiplied to achieve the desired nominal operating range:

$$f_{(\text{system})} = (N+1) \times f_{(\text{crystal})}$$

The crystal frequency multiplication is achieved with a frequency locked loop (FLL) technique. The factor N is recommended to be 32. The FLL technique, in combination with a digital controlled oscillator (DCO), provides immediate start-up capability together with long-term crystal stability. The frequency variation of the DCO with the FLL inactive is typically 330 ppm, which means that with a cycle time of 1 μ s, the maximum possible variation is 0.33 ns. For more precise timing, the FLL can be used. This forces longer cycle times if the previous cycle time was shorter than the selected one. This switching of cycle times makes it possible to meet the chosen system frequency over a long period of time.

The start-up operation of the system clock depends on the previous machine state. During a power-up clear (PUC), the DCO is reset to its lowest possible frequency. The control logic starts operation immediately after removal of the PUC condition. Correct operation of the FLL control logic requires the presence of a stable crystal oscillator.



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digital I/O

There is one eight-bit I/O port, Port0, that is implemented (MSP430C311S and MSP430P315S have six bits available on external pins). Six control registers give maximum flexibility of digital input/output to the application:

- All individual I/O bits are programmable independently.
- Any combination of input, output, and interrupt conditions is possible.
- Interrupt processing of external events is fully implemented for all eight bits of port P0.
- Provides read/write access to all registers with all instructions

The six registers are:

- | | | |
|-------------------------|--------|--|
| • Input register | 8 bits | contains information at the pins |
| • Output register | 8 bits | contains output information |
| • Direction register | 8 bits | controls direction |
| • Interrupt flags | 6 bits | indicates if interrupt(s) are pending |
| • Interrupt edge select | 8 bits | contains input signal change necessary for interrupt |
| • Interrupt enable | 6 bits | contains interrupt enable bits |

All these registers contain eight bits except for the interrupt flag register and the interrupt enable register. The two least significant bits (LSBs) of the interrupt flag and interrupt enable registers are located in the special functions register (SFR). Three interrupt vectors are implemented, one for Port0.0, one for Port0.1, and one commonly used for any interrupt event on Port0.2, to Port0.7. The Port0.1 and Port0.2 pin function is shared with the 8-bit timer/counter.

LCD drive

Liquid crystal displays (LCDs) for static, 2-, 3-, and 4-MUX operations can be driven directly. The controller LCD logic operation is defined by software using memory-bit manipulation. LCD memory is part of the LCD module and not part of the data memory. Eight mode and control bits define the operation and current consumption of the LCD drive. The information for the individual digits can be easily obtained using table programming techniques combined with the correct addressing mode. The segment information is stored in LCD memory using instructions for memory manipulation.

The drive capability is mainly defined by the external resistor divider that supports the analog levels for 2-, 3-, and 4-MUX operation. Groups of the LCD segment lines can be selected for digital output signals. The MSP430x31x has four common signals and 23 segment lines. The MSP430C311S and MSP430P315S have four common lines and 16 segment lines.

Timer/Port

The timer/port module has two 8-bit counters, an input that triggers one counter, and six digital outputs in the MSP430x31x (MSP430C311S, MSP430C315S have five digital outputs available on external pins) with 3-state capability. Both counters have an independent clock-selector for selecting an external signal or one of the internal clocks (ACLK or MCLK). One of the counters has an extended control capability to halt, count continuously, or gate the counter by selecting one of two external signals. This gate signal sets the interrupt flag, if an external signal is selected and the gate stops the counter.

Both timers can be read from and written to by software. The two 8-bit counters can be cascaded to a 16-bit counter. A common interrupt vector is implemented. The interrupt flag can be set from three events in the 8-bit counter mode (gate signal, overflow from the counters) or from two events in the 16-bit counter mode (gate signal, overflow from the MSB of the cascaded counter).

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slope A/D conversion

Slope A/D conversion is accomplished with the timer/port module using external resistor(s) for reference (R_{ref}), external resistor(s) to the measured (R_{meas}), and an external capacitor. The external components are driven by software in such a way that the internal counter measures the time that is needed to charge or discharge the capacitor. The reference resistor's (R_{ref}) charge or discharge time is represented by N_{ref} counts. The unknown resistors (R_{meas}) charge or discharge time is represented by N_{meas} counts. The unknown resistor's value (R_{meas}) is the value of R_{ref} multiplied by the relative number of counts (N_{meas}/N_{ref}). This value determines resistive sensor values that correspond to the physical data, for example temperature, when an NTC or PTC resistor is used.

Basic Timer1

The basic timer1 (BT1) divides the frequency of MCLK or ACLK, as selected with the SSEL bit, to provide low frequency control signals. This is done within the system by one central divider, the basic timer1, to support low current applications. The BTCTL control register contains the flags which controls or selects the different operational functions. When the supply voltage is applied or when a reset of the device (\overline{RST}/NMI pin), a watchdog overflow, or a watchdog security key violation occurs, all bits in the register hold undefined or unchanged status. The user software usually configures the operational conditions on the BT1 during initialization.

The Basic Timer1 has two 8 bit timers which can be cascaded to a 16 bit timer. Both timers can be read and written by software. Two bits in the SFR address range handle the system control interaction according to the function implemented in the Basic Timer1. These two bits are the Basic Timer Interrupt Flag (BTIFG) and the Basic Timer Interrupt Enable (BTIE) bit.

Watchdog Timer

The primary function of the Watchdog Timer (WDT) module is to perform a controlled system restart after a software upset has occurred. If the selected time interval expires, a system reset is generated. If this watchdog function is not needed in an application, the module can work as an interval timer, which generates an interrupt after the selected time interval.

The Watchdog Timer counter (WDCNT) is a 15/16-bit upcounter which is not directly accessible by software. The WDCNT is controlled using the Watchdog Timer control register (WDTCTL), which is an 8-bit read/write register. Writing to WDTCTL, in both operating modes (watchdog or timer) is only possible by using the correct password in the high-byte. The low-byte stores data written to the WDTCTL. The high-byte password is 05Ah. If any value other than 05Ah is written to the high-byte of the WDTCTL, a system reset PUC is generated. When the password is read its value is 069h, that minimizes accidental write operations to the WDTCTL register. A read-access to WDTCTL is only possible by writing 05Ah as the password in the high-byte of the WDTCTL. This avoids an accidental write-access on the WDTCTL. Additional to the Watchdog Timer control bits, two bits included in the WDTCTL which configure the NMI pin.



8-bit Timer/Counter

The 8-bit interval timer supports three major functions for the application:

- Serial communication or data exchange
- Pulse counting or pulse accumulation
- Timer

The 8-bit timer/counter peripheral includes the following major blocks: an 8-bit up-counter with preload register, an 8-bit control register, an input clock selector, an edge detection (e.g. start bit detection for asynchronous protocols), and an input and output data latch, triggered by the carry-out-signal from the 8-bit counter.

The 8-bit counter counts up with an input clock which is selected by two control bits from the control register. The four possible clock sources are MCLK, ACLK, the external signal from terminal P0.1, and the signal from the logical .AND. of MCLK and terminal P0.1.

Two counter inputs (load, enable) control the counter operation. The load input controls load operations. A write-access to the counter results in loading the content of the preload register into the counter. The software writes or reads the preload register with all instructions. The preload register acts as a buffer and can be written immediately after the load of the counter is completed. The enable input enables the count operation. When the enable signal is set to high, the counter will count up each time a positive clock edge is applied to the clock input of the counter.

Serial protocols, like UART protocol, need start-bit edge-detection to determine, at the receiver, the start of a data transmission. When this function is activated, the counter starts counting after start-bit condition is detected. The first signal level is sampled into the RXD input data-latch after completing the first timing interval, which is programmed into the counter. Two latches used for input and output data (RXD_FF and TXD_FF) are clocked by the counter after the programmed timing interval has elapsed.

UART

The serial communication is realized by using software and the 8-bit timer/counter hardware. The hardware supports the output of the serial data stream, bit-by-bit, with the timing determined by the counter. The software/hardware interface connects the mixed signal controller to external devices, systems, or networks.

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peripheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog/Timer Control	WDTCTL	0120h
PERIPHERALS WITH BYTE ACCESS			
EPROM	EPROM Control	EPCTL	054h
Crystal Buffer	Crystal Buffer Control	CBCTL	053h
System Clock	SCG Frequency Control	SCFQCTL	052h
	SCG Frequency Integrator	SCFI1	051h
	SCG Frequency Integrator	SCFI0	050h
Timer/Port	Timer Port Enable	TPE	04Fh
	Timer Port Data	TPD	04Eh
	Timer Port Counter2	TPCNT2	04Dh
	Timer Port Counter1	TPCNT1	04Ch
	Timer Port Control	TPCTL	04Bh
8-Bit Timer/Counter	8-Bit Timer/Counter Data	TCDAT	044h
	8-Bit Timer/Counter Preload	TCPLD	043h
	8-Bit Timer/Counter Control	TCCTL	042h
Basic Timer1	Basic Timer Counter2	BTCNT2	047h
	Basic Timer Counter1	BTCNT1	046h
	Basic Timer Control	BTCTL	040h
LCD	LCD Memory 15 :	LCDM15	03Fh
	LCD Memory1	LCDM1	031h
	LCD Control & Mode	LCDC	030h
Port P0	Port P0 Interrupt Enable	P0IE	015h
	Port P0 Interrupt Edge Select	P0IES	014h
	Port P0 Interrupt Flag	P0IFG	013h
	Port P0 Direction	P0DIR	012h
	Port P0 Output	P0OUT	011h
	Port P0 Input	P0IN	010h
	Special Function	SFR Interrupt Flag2	IFG2
SFR Interrupt Flag1		IFG1	002h
SFR Interrupt Enable2		IE2	001h
SFR Interrupt Enable1		IE1	000h

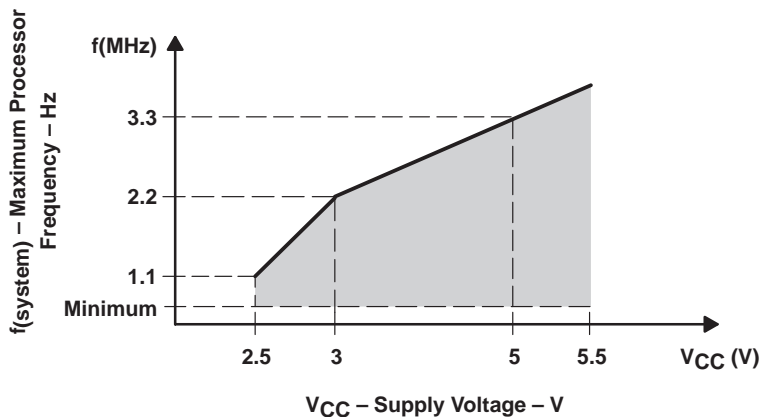


absolute maximum ratings

Voltage applied at V_{CC} to V_{SS}	-0.3 V to +6 V
Voltage applied to any pin (referenced to V_{SS})	-0.3 V to $V_{CC}+0.3$ V
Diode current at any device terminal	± 2 mA
Storage temperature, T_{stg} (unprogrammed device)	-55°C to 150°C
Storage temperature, T_{stg} (programmed device)	-40°C to 85°C

recommended operating conditions

		MIN	NOM	MAX	UNITS
Supply voltage, V_{CC}	MSP430Cxxx	2.5		5.5	V
	MSP430P/E313	2.7		5.5	
	MSP430P/E315	2.7		5.5	
Supply voltage, V_{SS}		0.0		0.0	V
Operating free-air temperature range, T_A	MSP430C31x	-40		85	°C
	MSP430P31x				
	PMS430E31x		25		
XTAL Frequency, f_{XTAL}			32 768		Hz
Processor frequency $f_{(system)}$ (signal MCLK) f_{system}	$V_{CC} = 3$ V	DC		2.2	MHz
	$V_{CC} = 5$ V	DC		3.3	



NOTE: Minimum processor frequency is defined by system clock (see page 21).

Figure 1. Frequency vs. Supply Voltage

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supply current (into V_{CC}) excluding external current ($f_{system} = 1$ MHz)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$ Active mode	C31x	$T_A = -40^{\circ}\text{C} + 85^{\circ}\text{C}$	$V_{CC} = 3\text{ V}$	400	500	μA	
			$V_{CC} = 5\text{ V}$	730	850		
	P313	$T_A = -40^{\circ}\text{C} + 85^{\circ}\text{C}$	$V_{CC} = 3\text{ V}$	2100	2700		
			$V_{CC} = 5\text{ V}$	7000	8600		
	P315(S)	$T_A = -40^{\circ}\text{C} + 85^{\circ}\text{C}$	$V_{CC} = 3\text{ V}$	490	525		
			$V_{CC} = 5\text{ V}$	960	1000		
$I_{(CPUOff)}$ Low power mode, (LPM0,1)	C31x	$T_A = -40^{\circ}\text{C} + 85^{\circ}\text{C}$	$V_{CC} = 3\text{ V}$	50	70	μA	
			$V_{CC} = 5\text{ V}$	100	130		
	P313	$T_A = -40^{\circ}\text{C} + 85^{\circ}\text{C}$	$V_{CC} = 3\text{ V}$	70	85		
			$V_{CC} = 5\text{ V}$	150	170		
	P315(S)	$T_A = -40^{\circ}\text{C} + 85^{\circ}\text{C}$	$V_{CC} = 3\text{ V}$	50	70		
			$V_{CC} = 5\text{ V}$	100	130		
$I_{(LPM2)}$ Low power mode, (LPM2)		$T_A = -40^{\circ}\text{C} + 85^{\circ}\text{C}$	$V_{CC} = 3\text{ V}$	6	12	μA	
			$V_{CC} = 5\text{ V}$	13	25		
$I_{(LPM3)}$ Low power mode, (LPM3)		$T_A = -40^{\circ}\text{C}$	$V_{CC} = 3\text{ V}$	1.5	2.4	μA	
				$T_A = 25^{\circ}\text{C}$	1.3		2
				$T_A = 85^{\circ}\text{C}$	1.6		2.8
		$T_A = -40^{\circ}\text{C}$	$V_{CC} = 5\text{ V}$	5.2	7		
				$T_A = 25^{\circ}\text{C}$	4.2		6
				$T_A = 85^{\circ}\text{C}$	4.8		5.4
$I_{(LPM4)}$ Low power mode, (LPM4)		$T_A = -40^{\circ}\text{C}$	$V_{CC} = 3\text{ V}/5\text{ V}$	0.1	0.8	μA	
				$T_A = 25^{\circ}\text{C}$	0.1		0.8
				$T_A = 85^{\circ}\text{C}$	0.4		1.3

NOTE: All inputs are tied to 0 V or V_{CC} . Outputs do not source or sink any current. The current consumption in LPM2 and LPM3 are measured with active basic timer (ACLK selected) and LCD module. ($f_{LCD} = 1024\text{ Hz}$, 4 mux)

Current consumption of active mode versus system frequency, C versions only

$$I_{AM} = I_{AM}[1\text{ MHz}] \times f_{system} [\text{MHz}]$$

Current consumption of active mode versus supply voltage, C versions only

$$I_{AM} = I_{AM}[3\text{ V}] + 200\ \mu\text{A/V} \times (V_{CC} - 3\text{ V})$$



electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

schmitt-trigger inputs Port 0, Timer/Port, CIN, TP0.5

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3 V	1.2		2.1	V
		V _{CC} = 5 V	2.3		3.4	
V _{IT-}	Negative-going input threshold voltage	V _{CC} = 3 V	0.5		1.35	V
		V _{CC} = 5 V	1.4		2.3	
V _{IT+} – V _{IT-}	Input voltage differential, (hysteresis)	V _{CC} = 3 V	0.3		1.0	V
		V _{CC} = 5 V	0.6		1.4	

standard inputs TCK, TMS, TDI, $\overline{\text{RST}}/\text{NMI}$

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V _{IL}	Low-level input voltage	V _{CC} = 3 V/5 V	V _{SS}		V _{SS} +0.8	V
V _{IH}	High-level input voltage		0.7V _{CC}		V _{CC}	V

outputs Port 0, P0.x, Timer/Port, TP0.0 – 5, LCD: S2/O2 to S26/O26 XBUF:XBUF, JTAG:TDO

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V _{OH}	High-level output voltage	I _(OHmax) = – 1.2 mA, V _{CC} = 3 V, See Note 3	V _{CC} –0.4		V _{CC}	V
		I _(OHmax) = – 3.5 mA, V _{CC} = 3 V, See Note 4	V _{CC} –1		V _{CC}	
		I _(OHmax) = – 1.5 mA, V _{CC} = 5 V, See Note 3	V _{CC} –0.4		V _{CC}	
		I _(OHmax) = – 4.5 mA, V _{CC} = 5 V, See Note 4	V _{CC} –1		V _{CC}	
V _{OL}	Low-level output voltage	I _(OLmax) = 1.2 mA, V _{CC} = 3 V, See Note 3	V _{SS}		V _{SS} +0.4	V
		I _(OLmax) = 3.5 mA, V _{CC} = 3 V, See Note 4	V _{SS}		V _{SS} +1	
		I _(OLmax) = 1.5 mA, V _{CC} = 5 V, See Note 3	V _{SS}		V _{SS} +0.4	
		I _(OLmax) = 4.5 mA, V _{CC} = 5 V, See Note 4	V _{SS}		V _{SS} +1	

- NOTES: 3. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±9.6 mA to hold the maximum voltage drop specified.
 4. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±20 mA to hold the maximum voltage drop specified.

leakage current (see Note 5)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I _{lkg(LTP)}	High-impedance leakage current, Timer/Port	Timer/Port: V _{TP0.x} , V _{CC} = 3 V/5 V, CIN = V _{SS} , V _{CC} , (see Note 6)			±50	nA
I _{lkg(LS27)}	High-impedance leakage current, S27	V _{S27} = V _{SS} to V _{CC} , V _{CC} = 3 V/5 V			±50	nA
I _{lkg(LP0x)}	Leakage current, port 0	Port P0: P0.x, 0 ≤ x ≤ 7, V _{CC} = 3 V/5 V, (see Note 7)			±50	nA

- NOTES: 5. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
 6. All Timer/Port pins TP0.0 to TP0.5 are Hi-Z. Pins CIN and TP.0 to TP0.5 are connected together during leakage current measurement. In the leakage measurement the input CIN is included. The input voltage is V_{SS} or V_{CC}.
 7. The port pin must be selected for input and there must be no optional pull-up or pull-down resistor.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

optional resistors, individually programmable with ROM code, PO.X, (see Note 8)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
R _(opt1)	Resistors, individually programmable with ROM code, all port pins, values applicable for pull down and pull up	V _{CC} = 3 V/5 V	2.1	4.1	6.2	kΩ
R _(opt2)		V _{CC} = 3 V/5 V	3.1	6.2	9.3	kΩ
R _(opt3)		V _{CC} = 3 V/5 V	6	12	18	kΩ
R _(opt4)		V _{CC} = 3 V/5 V	10	19	29	kΩ
R _(opt5)		V _{CC} = 3 V/5 V	19	37	56	kΩ
R _(opt6)		V _{CC} = 3 V/5 V	38	75	113	kΩ
R _(opt7)		V _{CC} = 3 V/5 V	56	112	168	kΩ
R _(opt8)		V _{CC} = 3 V/5 V	94	187	281	kΩ
R _(opt9)		V _{CC} = 3 V/5 V	131	261	392	kΩ
R _(opt10)		V _{CC} = 3 V/5 V	167	337	506	kΩ

NOTE 8: Optional resistors R_{optx} for pull-down or pull-up are not programmed in standard OTP/EPROM devices P/E313 and P/E315(s)

inputs P0.x, CIN, TP.5; output XBUF

	PARAMETER	TEST CONDITIONS	VCC	MIN	NOM	MAX	UNIT
t _(int)	External Interrupt timing	Port P0 External trigger signal for the interrupt flag, (see Notes 9 and 10)	3 V/ 5 V	1.5			cycle
f _(IN)	Input frequency	P0.x, CIN, TP.5	3 V/ 5 V	DC	f _(system)		MHz
t _(H) or t _(L)	High level or low level time		3 V	225			ns
t _(H) or t _(L)			5 V	150			ns
f _(XBUF)	Clock output frequency	XBUF, C _L = 20 pF	3 V/ 5 V		f _(system)		MHz
t _(Xdc)	Duty cycle of clock output frequency	XBUF, C _L = 20 pF f _(MCLK) = 1.1 MHz	3V/ 5V	40%			
		f _(XBUF) = f _(ACLK)	3V/ 5V	35%		60%	
		f _(XBUF) = f _(ACLK/n)	3V/ 5V		50%		65%

NOTES: 9. The external signal sets the interrupt flag every time t_{int} is met. It may be set even with trigger signals shorter than t_{int}. The conditions to set the flag must be met independently from this timing constraint. T_{int} is defined in MCLK cycles.

10. The external interrupt signal cannot exceed the maximum input frequency (f_(in)).

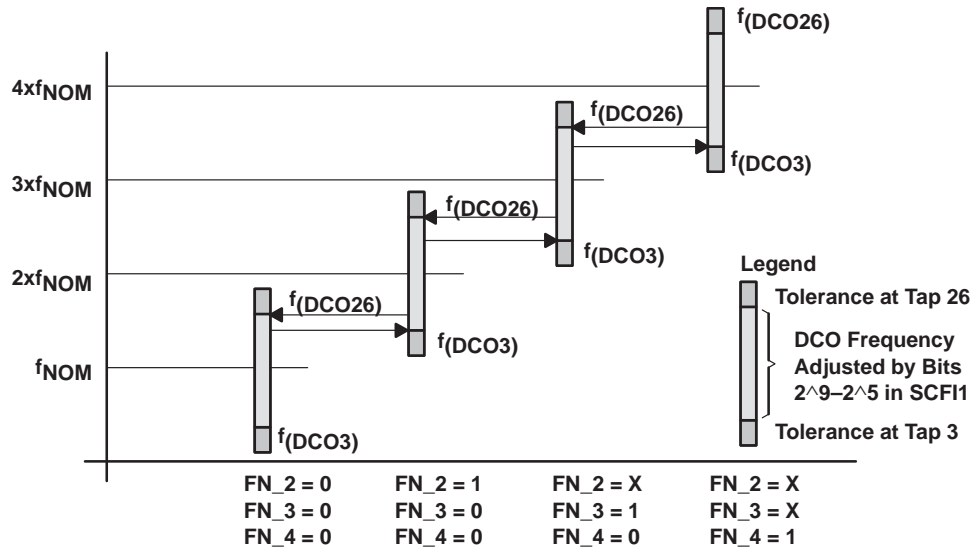
crystal oscillator, Xin, Xout

	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
C _(Xin)	Integrated capacitance at input	V _{CC} = 3 V/5 V		12		pF
C _(Xout)	Integrated capacitance at output	V _{CC} = 3 V/5 V		12		pF
X _{INL}	Input levels at XIN, XOUT	V _{CC} = 3 V/5 V	V _{SS}		0.2×V _{CC}	V
X _{INH}			0.8×V _{CC}		V _{CC}	



electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$f_{(NOM)}$	DCO	$N_{DCO} = 1A0h$ $FN_4=FN_3=FN_2=0$		1		MHz
$f_{(NOM)}$	f_{DCO3}	$N_{DCO} = 00\ 0110\ 0000$ $FN_4=FN_3=FN_2=0$	$V_{CC} = 3\ V$	0.15	0.6	MHz
			$V_{CC} = 5\ V$	0.18	0.62	
	f_{DCO26}	$N_{DCO} = 11\ 0100\ 0000$ $FN_4=FN_3=FN_2=0$	$V_{CC} = 3\ V$	1.25	4.7	
			$V_{CC} = 5\ V$	1.45	5.5	
$2xf_{(NOM)}$	f_{DCO3}	$N_{DCO} = 00\ 0110\ 0000$ $FN_4=FN_3=0, FN_2=1$	$V_{CC} = 3\ V$	0.36	1.05	MHz
			$V_{CC} = 5\ V$	0.39	1.2	
	f_{DC26}	$N_{DCO} = 11\ 0100\ 0000$ $FN_4=FN_3=0, FN_2=1$	$V_{CC} = 3\ V$	2.5	8.1	
			$V_{CC} = 5\ V$	3	9.9	
$3xf_{(NOM)}$	f_{DCO3}	$N_{DCO} = 00\ 0110\ 0000$ $FN_4=0, FN_3=1, FN_2=X$	$V_{CC} = 3\ V$	0.5	1.5	MHz
			$V_{CC} = 5\ V$	0.6	1.8	
	f_{DCO26}	$N_{DCO} = 11\ 0100\ 0000$ $FN_4=0, FN_3=1, FN_2=X$	$V_{CC} = 3\ V$	3.7	11	
			$V_{CC} = 5\ V$	4.5	13.8	
$4xf_{(NOM)}$	f_{DCO3}	$N_{DCO} = 00\ 0110\ 0000$ $FN_4=1, FN_3=FN_2=X$	$V_{CC} = 3\ V$	0.7	1.85	MHz
			$V_{CC} = 5\ V$	0.8	2.4	
	f_{DCO26}	$N_{DCO} = 11\ 0100\ 0000$ $FN_4=1, FN_3=FN_2=X$	$V_{CC} = 3\ V$	4.8	13.3	
			$V_{CC} = 5\ V$	6	17.7	
N_{DCO}		$f_{MCLK} = f_{NOM}$ $FN_4=FN_3=FN_2=0$	$V_{CC} = 3\ V/5\ V$	A0h	1A0h	340h
S		$f_{NDCO+1} = S \times f_{NDCO}$	$V_{CC} = 3\ V/5\ V$	1.07	1.13	



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LCD

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
V ₂₃	Analog voltage	Voltage at R23	V _{CC} = 3 V/5 V	$\frac{(V_{CC}-V_{SS}) \times 2}{3+V_{SS}}$			V
V ₁₃		Voltage at R13	V _{CC} = 3 V/5 V	$\frac{(V_{CC}-V_{SS}) \times 1}{3+V_{SS}}$			V
V _O (HLCD)	Output 1 (HLCD)	I(HLCD) ≤ 10 nA	V _{CC} = 3 V/5 V	V _{CC} -0.125		V _{CC}	V
V _O (LLCD)	Output 0 (LLCD)	I(LLCD) ≤ 10 nA		V _{SS}		V _{SS} +0.125	
I _I (R13)	Input leakage (see Note 11)	R13 = V _{CC} / 3	V _{CC} = 3 V/5 V			±20	nA
I _I (R23)		R23 = 2 V _{CC} / 3					
r _o (R13) to S(XX)	Output (SXX)	I(SXX) = -3 μA, V _{CC} = 3 V/5 V				33	kΩ
r _o (R23) to S(XX)							

NOTE 11: I_I(R_{xx}) is measured with no load on the segment or common LCD I/O pins.

comparator (Timer/Port)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
I _(com)	Comparator (Timer/Port)	CPON = 1	V _{CC} = 3 V		250	350	μA
			V _{CC} = 5 V		450	600	
V _{ref} (com)		CPON = 1, V _{CC} = 3 V/5 V	0.230×V _{CC}	0.25×V _{CC}	0.260×V _{CC}	V	
V _{hys} (com)		CPON = 1	V _{CC} = 3 V		5	37	mV
	V _{CC} = 5 V			10	42		

RAM

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
V _{RAMh}	CPU halted (see Note 12)			1.8			V

NOTE 12: This parameter defines the minimum supply voltage when the data in the program memory RAM remains unchanged. No program execution should happen during this supply voltage condition.

PUC/POR

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
t(POR_Delay)	POR	V _{CC} = 3 V/5 V		150		250	μs
V(POR)				1.3		1.9	V
V(min)				0		0.4	
f(NOM)	DCO	NDC ₀ = 20h, T _A = 25°C	V _{CC} = 3 V/5 V		1		MHz
t _{RESET}	Reset is accepted internally, PUC/POR		V _{CC} = 3 V/5 V	2			μs

wake-up from LPM3

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
t(LPM3)	Delay time	f = 1 MHz	V _{CC} = 3 V			6	μs
			V _{CC} = 5 V				
		f = 2 MHz	V _{CC} = 3 V			6	
			V _{CC} = 5 V				
		f = 3 MHz	V _{CC} = 5 V			6	



electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT	
f _(TCK)	JTAG/Test	TCK frequency	V _{CC} = 3 V	DC	5	MHz	
			V _{CC} = 5 V	DC	10		
R _(TEST)		Pull-up resistors on TMS, TCK, TDI, See Note 13	V _{CC} = 3 V/ 5 V	25	60	90	kΩ
V _(FB)	JTAG/Fuse, See Note 14	Fuse blow voltage, C versions, See Note 15	V _{CC} = 3 V/ 5 V	5.5	6	V	
		Fuse blow voltage, E/P versions, See Note 15	V _{CC} = 3 V/ 5 V	11	12		
I _(FB)		Supply current on TDI/VPP to blow fuse			100	mA	
t _(FB)		Time to blow the fuse			1	ms	
V _(PP)	EPROM (E) and OTP(P) – versions only	Programming Voltage, applied to TDI/VPP	V _{CC} = 3 V/ 5 V	11	11.5	12	V
I _(PP)		Current from programming voltage source	V _{CC} = 3 V/ 5 V			70	mA
t _(pps)		Programming time, single pulse	V _{CC} = 3 V/ 5 V	5			ms
t _(ppf)		Programming time, fast algorithm	V _{CC} = 3 V/ 5 V		100		μs
P _n		Pulses for successful programming	V _{CC} = 3 V/ 5 V	4		100	
t _(erase)		EPROM P– and E–versions only	Erase time wave length 2537 Å at 15 Ws/cm ² (UV lamp of 12 mW/ cm ²)		30		min
	Write/Erase cycles			1000			
	Data retention T _j < 55°C			10		Year	

- NOTES: 13. The TMS and TCK pull up resistors are implemented in all ROM(C), OTP(P), and EPROM(E) versions.
 14. Once the JTAG fuse is blown no further access to the MSP430 JTAG/Test feature is possible.
 15. The voltage supply to blow the JTAG fuse is applied to TDI/VPP pin when fuse blowing is desired.

TYPICAL CHARACTERISTICS

DIGITAL CONTROLLED OSCILLATOR FREQUENCY
vs
TEMPERATURE

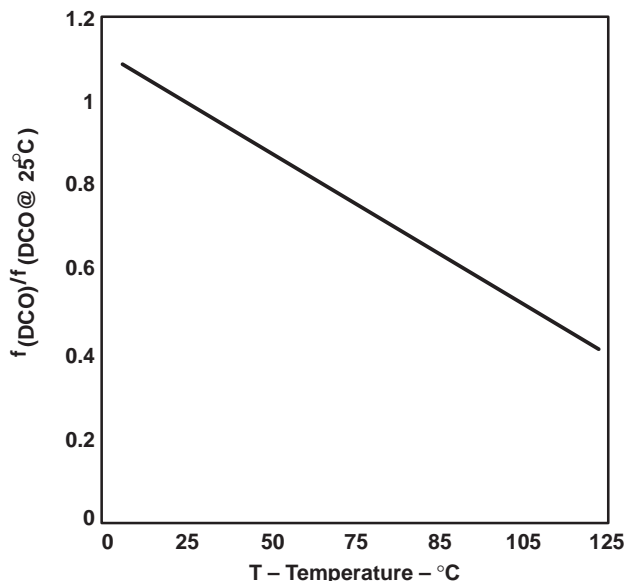


Figure 2

DIGITAL CONTROLLED OSCILLATOR FREQUENCY
vs
SUPPLY VOLTAGE

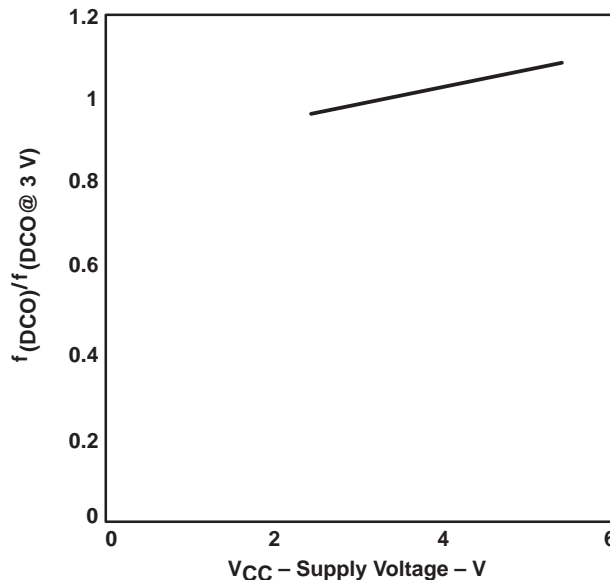
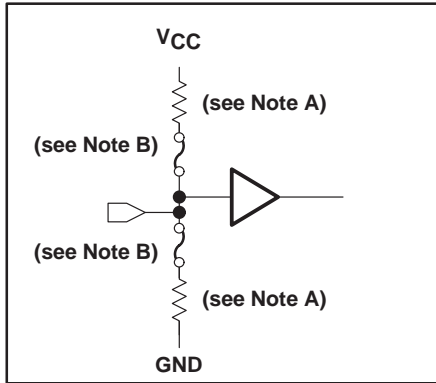
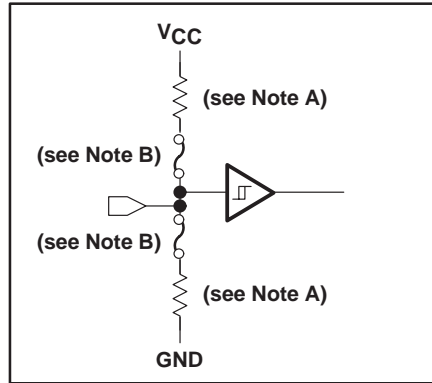


Figure 3

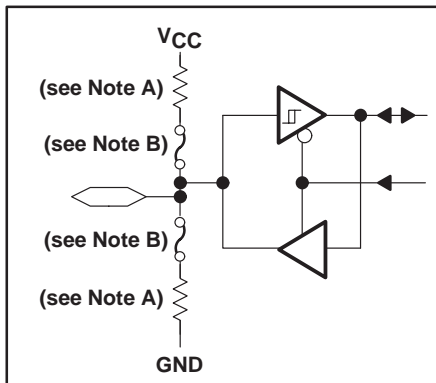
APPLICATION INFORMATION



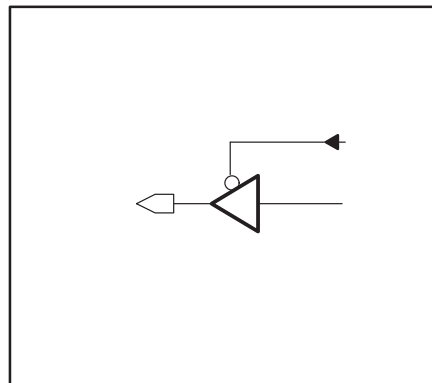
CMOS INPUT ($\overline{\text{RST}}/\text{NMI}$, S27/O27/CMPI)



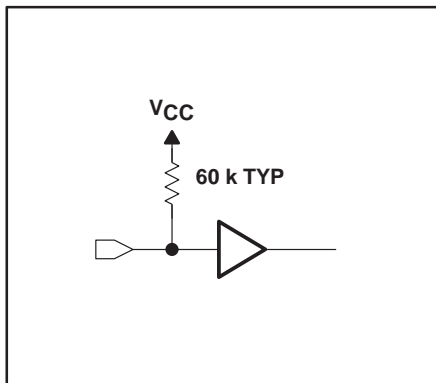
CMOS SCHMITT-TRIGGER INPUT (CIN)



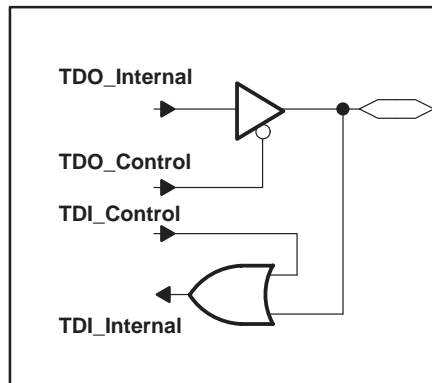
I/O WITH SCHMITT-TRIGGER INPUT (P0.x, TP0.5)



CMOS 3-STATE OUTPUT (TP0.0–4, XBUF)



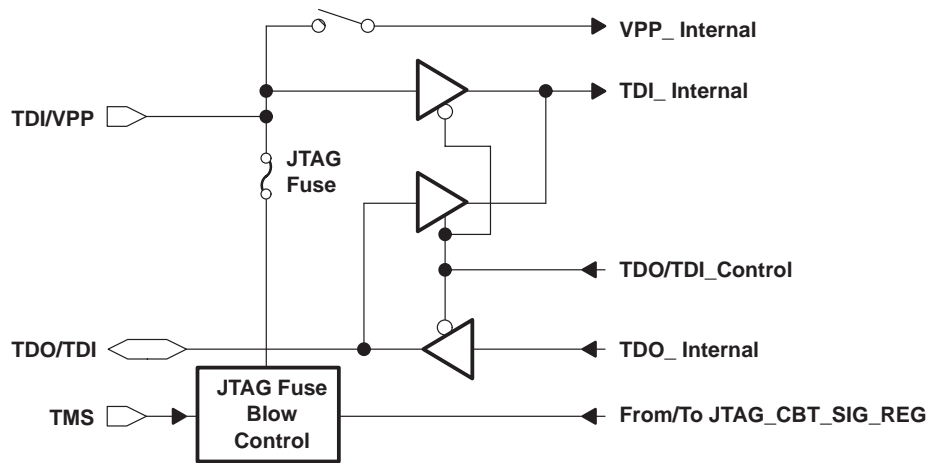
MSP430C31x: TMS, TCK
MSP430P/E31x: TMS, TCK



MSP430C31x: TDO/TDI
MSP430P/E31x: TDO/TDI

NOTES: A. Optional selection of pull up or pull down resistors with ROM (masked) versions.
 B. Fuses for the optional pull up and pull down resistors can only be programmed at the factory.

APPLICATION INFORMATION



- NOTES: A. During programming activity and when blowing the JTAG enable fuse, the TDI/VPP terminal is used to apply the correct voltage source. The TDO/TDI terminal is used to apply the test input data for JTAG circuitry.
- B. The TDI/VPP terminal of the 'P31x and 'E31x does not have an internal pull up resistor. An external pull down resistor is recommended to avoid a floating node which could increase the current consumption of the device.
- C. The TDO/TDI terminal is in a high-impedance state after POR. The 'P31x and 'E31x need a pull up or a pull down resistor to avoid floating a node which could increase the current consumption of the device.

Figure 4. MSP430P313/E313/P315(S)/E315: TDI/VPP, TDO/TDI

MSP430x31x MIXED SIGNAL MICROCONTROLLERS

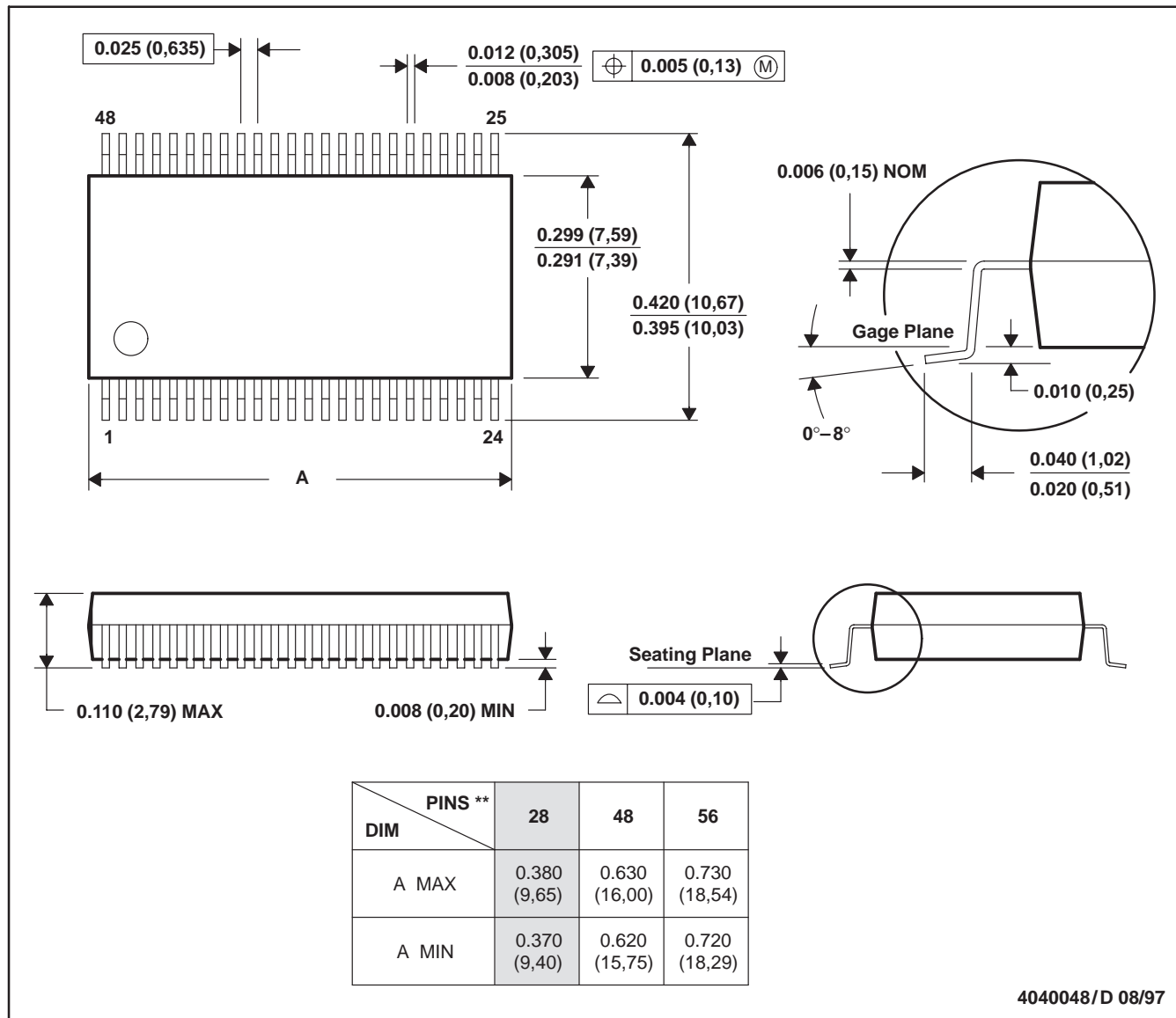
SLAS165B – FEBRUARY 1998 – REVISED NOVEMBER 1998

MECHANICAL DATA

DL (R-PDSO-G**)

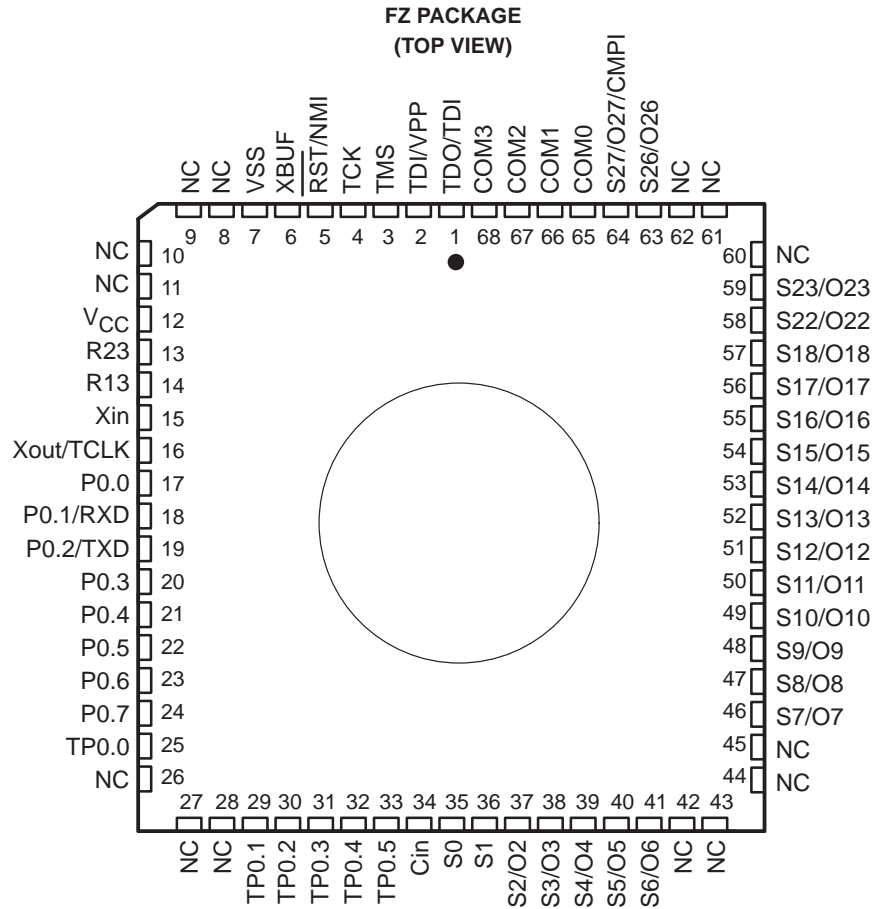
PLASTIC SMALL-OUTLINE PACKAGE

48-PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

pinning PMS430E313, PMS430E315 (FZ package)



MSP430x31x MIXED SIGNAL MICROCONTROLLERS

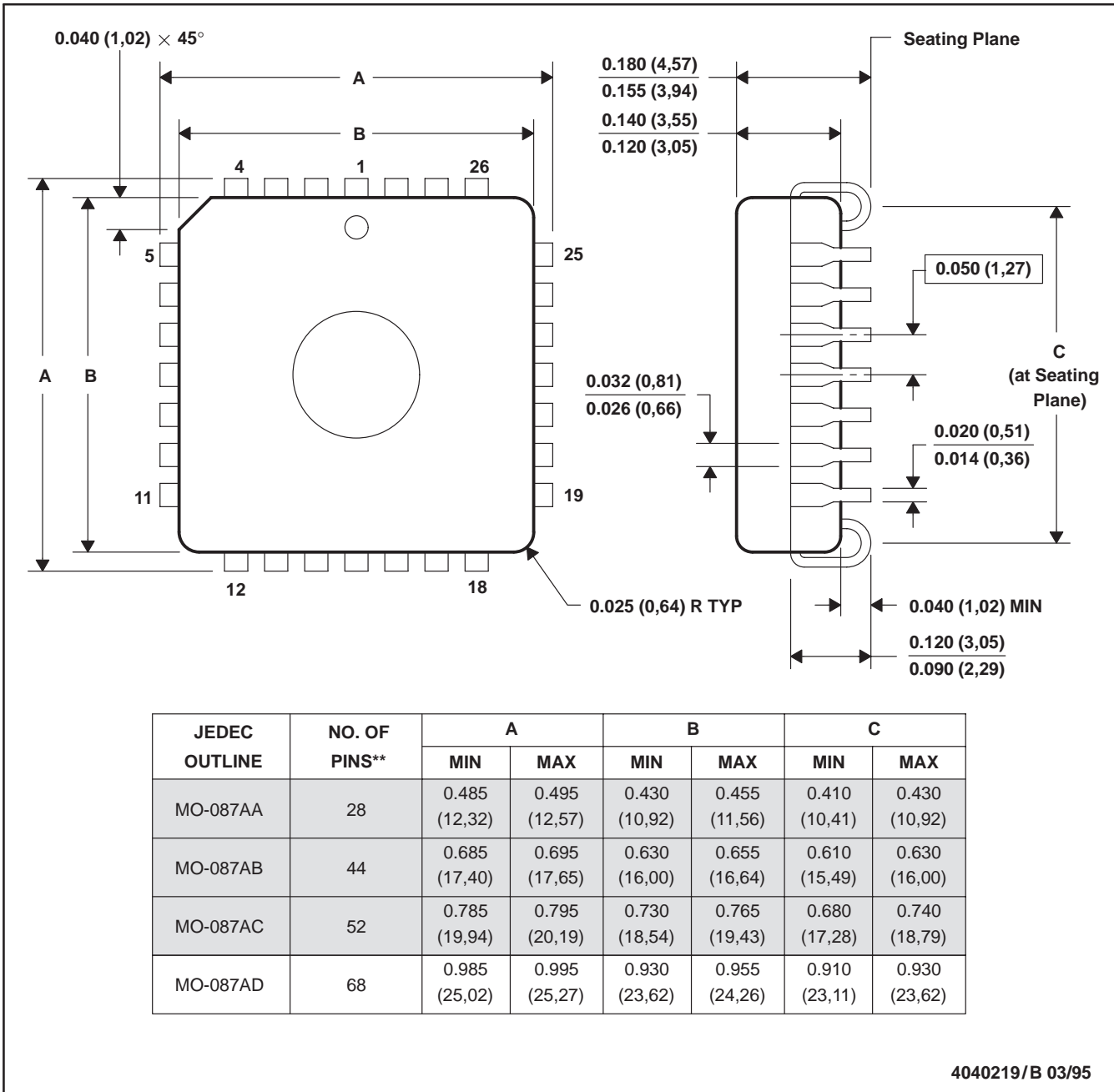
SLAS165B – FEBRUARY 1998 – REVISED NOVEMBER 1998

MECHANICAL DATA

FZ (S-CQCC-J**)

J-LEADED CERAMIC CHIP CARRIER

28 LEAD SHOWN



4040219/B 03/95

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.

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