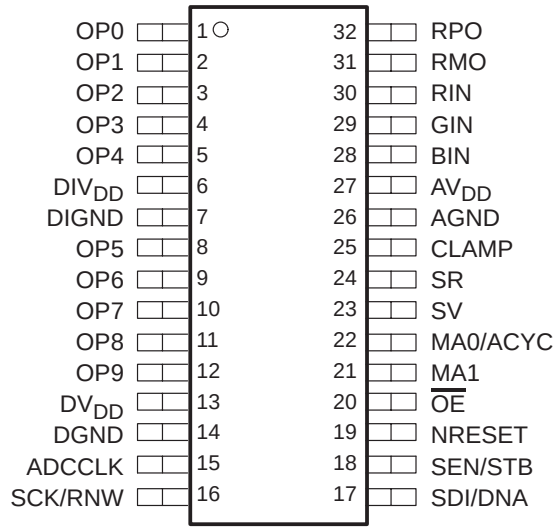
- **Supports Both CIS and CCD Sensors**
- **10-Bit, 4 MSPS, A/D Converter**
- **Differential Nonlinearity Error: ±0.5 LSB Typ**
- **Integral Nonlinearity Error: ±0.6 LSB Typ**
- **8-Bit Offset Correction DAC**
- **PGA With 6-Bit Gain Resolution**
- **Auto-cycling Gain and Offset Control**
- **Single 5-V Supply Operation**
- **Very Low Power: 190 mW Typical**
- **Control by Parallel and Serial Interface**
- **Internal Reference Voltages**
- **32-Pin TSSOP Package**

DA PACKAGE
(TOP VIEW)



description

The TLC8188 is a highly-integrated monolithic analog signal processor/digitizer designed to interface the contact image sensor (CIS) and linear charge-coupled device (CCD) image sensors in scanner applications. The input of the TLC8188 allows direct connection to the CIS and direct ac coupling of the linear CCD. The TLC8188 performs all the analog processing functions necessary to maximize the dynamic range, correct various errors associated with the CIS and the linear CCD sensors, and then digitize the results with an on-chip analog-to-digital converter (ADC). The key components of the TLC8188 include: input clamp circuitry and a correlated double sampler (CDS), a programmable gain amplifier (PGA) with auto-cycling gain control, a programmable offset correction controlled by a digital-to-analog converter (DAC), a 10-bit, 4 MSPS pipeline ADC, a bidirectional parallel bus and a three-wire serial port for easy microprocessor interface, and internal reference voltages.

Designed in advanced CMOS process, the TLC8188 operates from a single 5-V power supply and its digital interface is 3 V compatible. The normal power consumption of the TLC8188 is just 190 mW.

Fully integrated analog processing circuitry, high throughput rate, single supply operation and low cost make the TLC8188 an ideal CIS/linear CCD sensor interfacing solution for imaging applications such as scanners and multifunctional office equipment (printer/scanner/facsimile/copier).

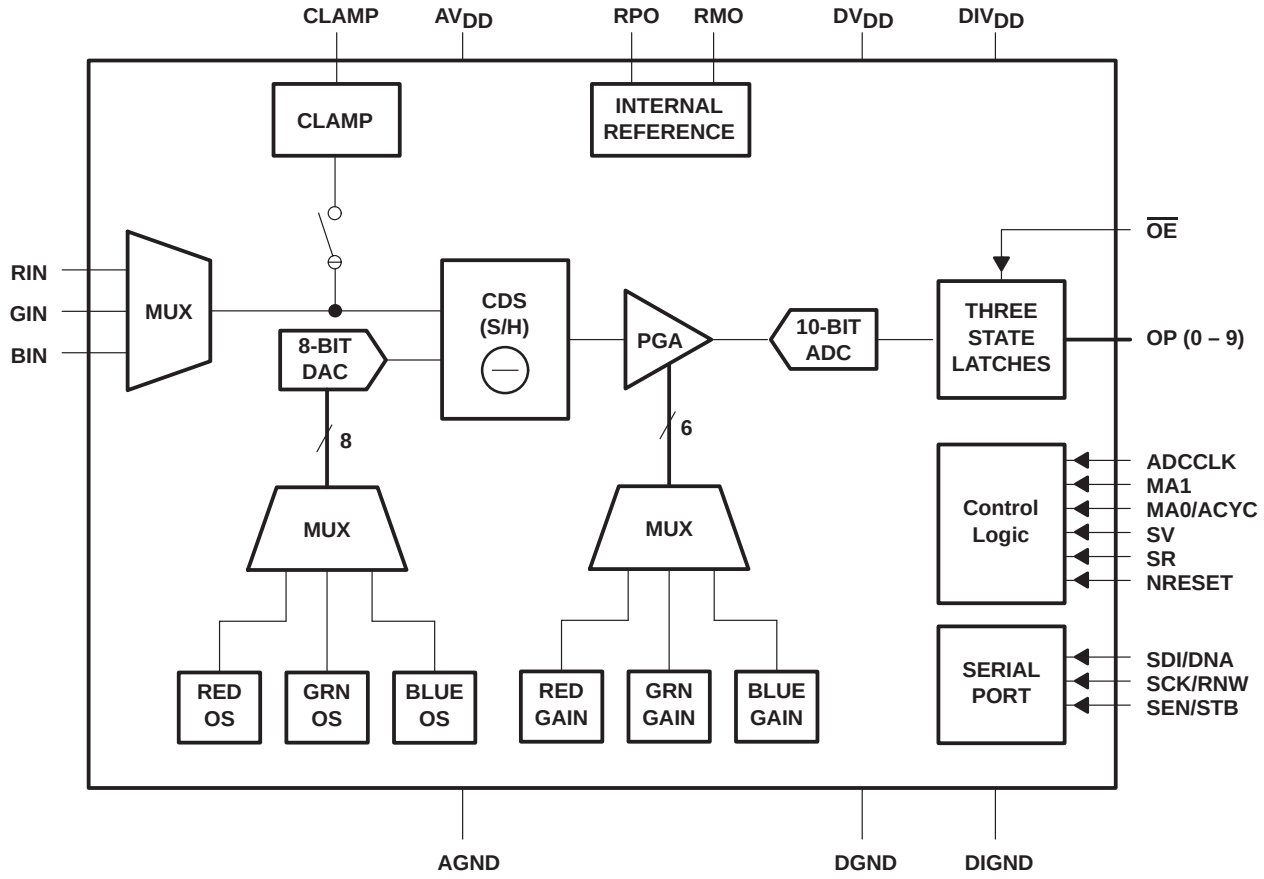
The device is available in a 32-pin TSSOP package and is specified over the 0°C to 70°C operating temperature range.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	SMALL OUTLINE (DA)
0°C to 70°C	TLC8188CDA

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADCCLK	15	I	ADC conversion clock input.
AGND	26		Analog ground
AV_{DD}	27		Analog supply voltage, 5 V
BIN	28	I	Blue channel input
CLAMP	25	I	CCD input clamp signal, active high
DGND	14		Digital ground
DIGND	7		Digital interface circuit ground
DIV_{DD}	6		Digital interface circuit supply voltage, 3 V to 5 V
DV_{DD}	13		Digital supply voltage, 5 V
GIN	29	I	Green channel input
MA1, MA0/ACYC	21, 22	I	MA1 and MA0 select the color to which all internal MUX (input, gain, offset) will point. When in auto-cycling mode, the input mux and internal registers are auto-cycled by the ACYC. The ACYC is a control signal such as a line start pulse that defines the start of a current scanning line.
NRESET	19	I	Power-on reset and Interface mode control. If SEN/STB is 1 when NRESET goes high then the device is in parallel configuration data input mode. If SEN/STB is 0 when NRESET goes high then the device is in serial data input mode.
$\overline{OE}$	20	I	Three-state output enable, active low
OP(0–4)	1 – 5	I/O	Three-state bi-directional data bus, OP0 and OP1 are output only.
OP(5–9)	8 – 12	I/O	Three-state bi-directional data bus.
RIN	30	I	Red channel input
RMO	31	O	Ref– output for external decoupling
RPO	32	O	Ref+ output for external decoupling
SCK/RNW	16	I	Serial interface: serial clock Parallel interface: 1 – OP(9–2) is output bus, 0 – OP(9–2) is input bus
SDI/DNA	17	I	Serial interface: serial interface input data Parallel interface: 1 – data, 0 – address
SEN/STB	18	I	Serial interface: serial data transfer enable, active high. Parallel interface: strobe, active low.
SR	24	I	CCD reset level sample pulse input
SV	23	I	CCD signal level sample pulse input

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.3 V to 6.5 V
Analog input voltage range . . . . . –0.3 V to V_{CC}+0.3 V
Reference input voltage . . . . . V_{CC}+0.3 V
Digital input voltage range . . . . . –0.3 V to V_{CC}+0.3 V
Operating virtual junction temperature range, T_J . . . . . –40°C to 150°C
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

power supplies

	MIN	NOM	MAX	UNIT
Analog supply voltage, AV_{DD}	4.5		5.5	V
Digital supply voltage, DV_{DD}	4.5		5.5	V
Digital interface supply voltage, DIV_{DD}	2.7		5.5	V

digital inputs

		MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	DIV_{DD} = 3 V to 5.5 V	$0.8DIV_{DD}$			V
Low-level input voltage, V_{IL}	DIV_{DD} = 3 V to 5.5 V			$0.2DIV_{DD}$	V
Input ADCCLK frequency				4	MHz
Input SCLK frequency				13.3	MHz

electrical characteristics over recommended operating free-air temperature range, AV_{DD} = DV_{DD} = 5 V, ADCCLK = 4 MHz (unless otherwise noted)

total device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	AV_{DD} operating current			35	40	mA
	DIV_{DD} operating current			1		mA
		5 pF loading, all outputs switching		2		mA
	Device power consumption			190		mW
	Device power consumption, power down mode			7		mW

analog-to-digital converter (ADC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			10		Bits
INL	Integral nonlinearity			±0.6	±2	LSB
DNL	Differential nonlinearity			±0.5	±1	LSB
	No missing codes					
	Full-scale input voltage			4		V_{PP}
	Input capacitance			15		pF
	Conversion rate				4	MHz
	ADC output latency			4		ADCCLK cycles

correlated double sampler (CDS) and programmable gain amplifier (PGA)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	CDS sample rate				4	MHz
	Analog input voltage			4		V
	Input capacitance			5		pF
	PGA gain control resolution			6		Bits
	PGA gain		1		5	V/V
	PGA gain accuracy			±5%		
	PGA output settling time			125		ns
	New gain settling time			125		ns

electrical characteristics over recommended operating free-air temperature range, AV_{DD} = DV_{DD} = 5 V, ADCCLK = 4 MHz (unless otherwise noted) (continued)

digital-to-analog converter (DAC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			8		Bits
INL	Integral nonlinearity			±0.5	±1	LSB
DNL	Differential nonlinearity			±0.3	±1	LSB
	Output settling time	To 1% accuracy			2	µs

reference voltages

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Internal bandgap voltage reference		1.15	1.22	1.28	V
	Temperature coefficient			100		ppm/°C
	Voltage reference noise			0.5		LSB
ADCRef+	ADC positive reference voltage	Externally decoupled	3.35	3.5	3.65	V
ADCRef–	ADC negative reference voltage	Externally decoupled	1.35	1.5	1.65	V
DACRef+	DAC positive reference voltage			2.5		V

input clamp voltages

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Clamp voltage, high	AV_{DD} = 4.5 V to 5.5 V		2.5		V
	Clamp voltage, low	AV_{DD} = 4.5 V to 5.5 V		1.5		V

digital specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic Inputs						
I_{IH}	High-level input current	DIV_{DD} = 5 V	–50		50	µA
I_{IL}	Low-level input current	DIV_{DD} = 5 V	–50		50	µA
C_i	Input capacitance			5		pF
Logic Outputs						
V_{OH}	High-level output voltage	I_{OH} = 50 µA to 0.5 mA	DIV_{DD}–0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 50 µA to 0.5 mA		0.4		V
I_{OZ}	High-impedance-state output current		–10		10	µA
C_O	Output capacitance			20		pF

timing requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Serial Interface						
$t_{w(SCKH)}$	SCK high pulse duration		37.5			ns
$t_{w(SCKL)}$	SCK low pulse duration		37.5			ns
$t_{su(SSU)}$	Data (SDI) to SCK setup time		10			ns
$t_{h(SH)}$	SDI to SCK hold time		10			ns
$t_{su(SCE)}$	SCK to SEN setup time		20			ns
$t_{w(SEN)}$	SEN pulse duration		50			ns
$t_{su(SEC)}$	SEN to SCK setup time		20			ns
Parallel Interface						
$t_{w(STB)}$	Strobe pulse duration		50			ns
$t_{su(D)}$	Data to strobe setup time		10			ns
$t_{h(DH)}$	Data to strobe hold time		10			ns
$t_{su(ADS)}$	Address to srobe setup time		10			ns
$t_{h(ADH)}$	Address to strobe hold time		10			ns
$t_{d(OPZI)}$	RNW low to OP bus 3-state delay time			10		ns
$t_{d(OPZE)}$	RNW high to OP bus 3-state delay time			0		ns
$t_{d(OPDV)}$	RNW high to data valid delay time			10		ns
Output						
t_{dis}	Output disable time			10		ns
t_{en}	Output enable time			10		ns
$t_{d(POW)}$	Delay time to power up			2		ms
$t_{d(PD)}$	Delay time to power down			30		ns
CIS Mode						
$t_{d(LSD)}$	ACYC high to the first valid pixel delay time			1		µs
$t_{w(ACYPW)}$	ACYC pulse duration		25			ns
$t_{w(ACLKH)}$	ADCCLK high pulse duration		125			ns
$t_{w(ACLKL)}$	ADCCLK low pulse duration		125			ns
$t_{su(SMPSU)}$	Sampling setup time		20			ns
$t_{d(OD)}$	ADCCLK to output data delay time			15		ns
CCD Mode						
$t_{d(LSD)}$	ACYC high to the first valid pixel delay time			1		µs
$t_{w(ACLKH)}$	ADCCLK high pulse duration		125			ns
$t_{w(ACLKL)}$	ADCCLK low pulse duration		125			ns
$t_{w(SRW)}$	Sample Reset (SR) pulse duration		40			ns
$t_{w(SVW)}$	Sample Video (SV) pulse duration		40			ns
$t_{d(ACLKSR)}$	ADCCLK low to SR low		60			ns
$t_{d(SRSVN)}$	Delay time SR low to SV high		20			ns
$t_{d(SRSVM)}$	Delay time SV low to SR high		125			ns
$t_{d(OD)}$	ADCCLK to output data delay time			15		ns

PARAMETER MEASUREMENT INFORMATION

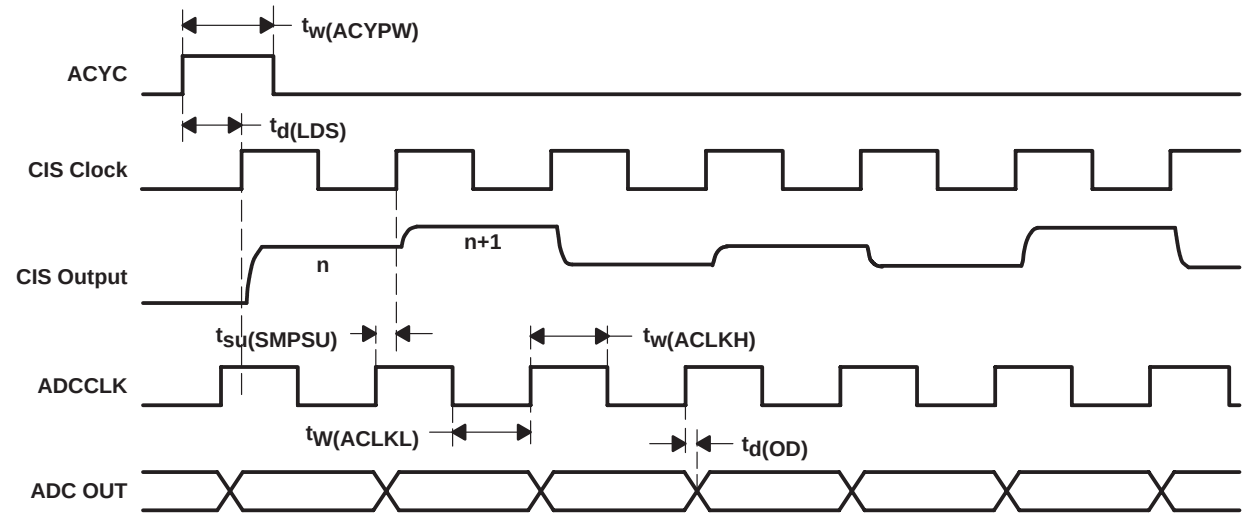


Figure 1. Typical CIS Mode Operation Timing

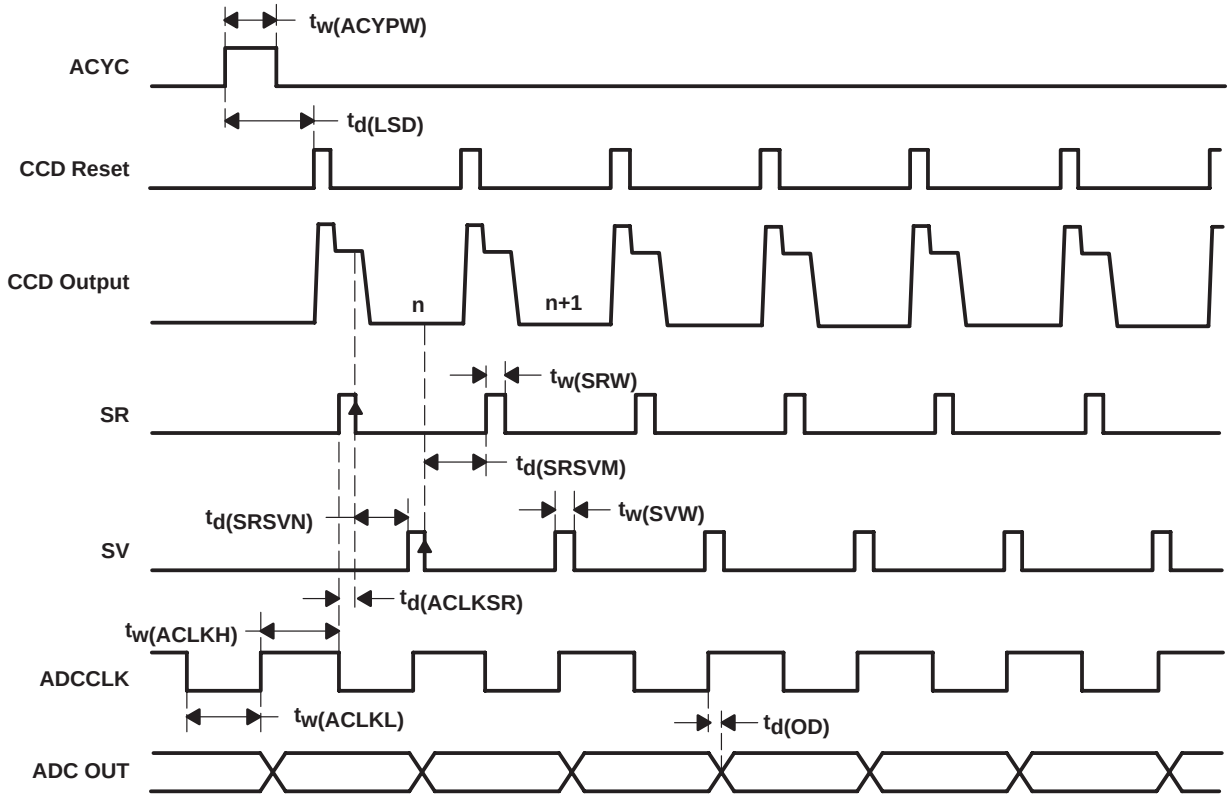


Figure 2. Typical CCD Mode Operation Timing

PARAMETER MEASUREMENT INFORMATION

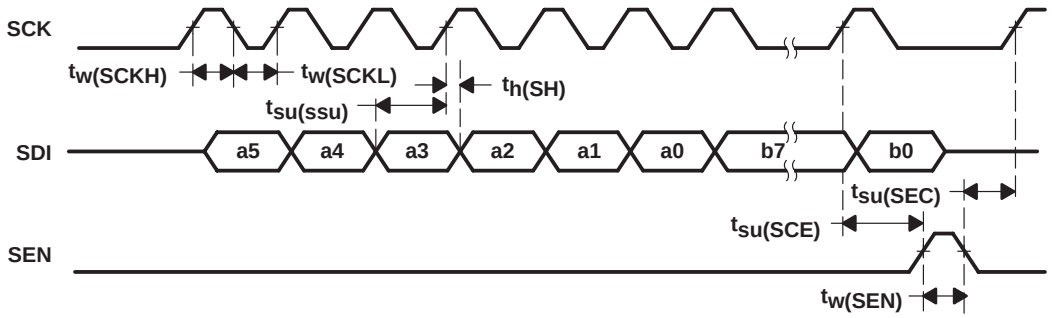


Figure 3. Serial Interface Timing

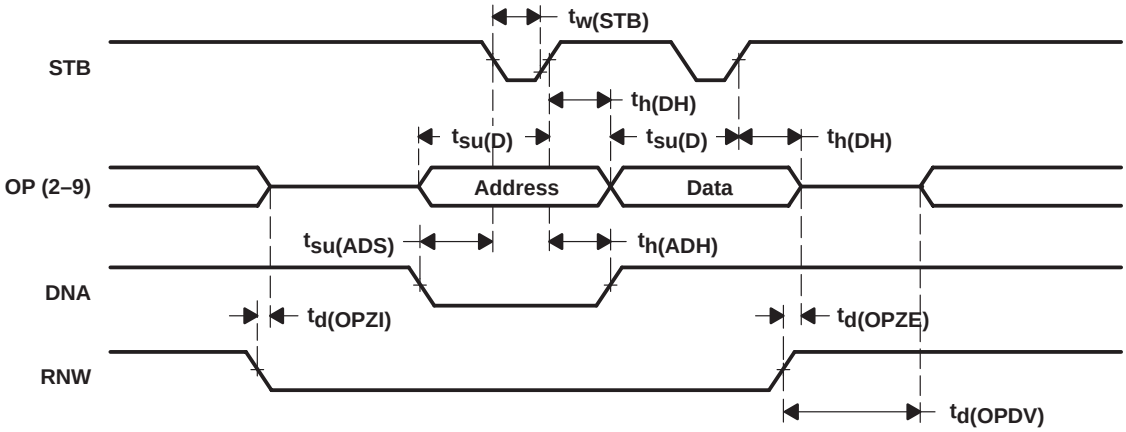


Figure 4. Parallel Interface Timing

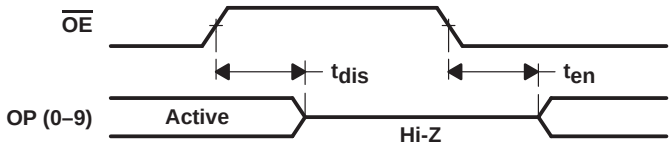


Figure 5. High-Impedance Output Timing

PRINCIPLES OF OPERATION

internal register definition

ADDRESS A5–A0	DESCRIPTION	R/W	DEF. (Hex)	BIT							
				B7	B6	B5	B4	B3	B2	B1	B0
000000	Not Used										
000001	Setup register 1	R/W	01					MUXOP	SM1	SM0	ENBL
000010	Setup register 2	R/W	00		FME	FM1	FM0	INTM1	INTM0	MM1	MM0
000011	Setup register 3	R/W	02							RLC1	RLC0
000100	Software reset	W	00								
000101	Auto-cycle reset	W	00								
000110	Read-only ID	R		0	0	0	0	0	0	0	1
000111	Test register	R/W	00	ST	RR	RA5	RA4	RA3	RA2	RA1	RA0
001000	Reserved										
001001	Reserved										
1000xx	DAC values	R/W	00	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0
1001xx	DAC signs	R/W	00								DSIGN
1010xx	PGA gains	R/W	00			PGA5	PGA4	PGA3	PGA2	PGA1	PGA0

	A1	A0	ADDRESS LSB DECODE	R/W	DEFAULT (HEX)
xx	0	0	Red register	R/W	00
	0	1	Green register	R/W	
	1	0	Blue register	R/W	
	1	1	Red, green, and blue	W	

setup register 1 description

BIT	NAME	DEFAULT	DESCRIPTION
B0	ENBL	1	Standby mode, 0 – standby, 1 – power up
B2,B1	SM1, SM0	00	Sensor mode control: SM1 SM0 0 0 CIS mode – single-ended input (default, RIN pin) 0 1 CIS mode – differential input (RIN, GIN pins) 1 0 CCD mode
B3	MUXOP	0	Eight bit output mode: 0 – ten bit, 1– eight-bit multiplexed

setup register 2 description

BIT	NAME	DEFAULT	DESCRIPTION
B1,B0	MM1, MM0	00	Input MUX and register MUX control: MM1 MM0 0 0 Internal 0 1 External 1 0 Auto-cycling
B3,B2	INTM1, INTM0	00	Register containing color codes used in internal modes
B5,B4	FM1, FM0	00	Register containing color codes used in force mux modes
B6	FME	0	Force mux mode control, 1 – force mux, 0 – no force mux

PRINCIPLES OF OPERATION

color selection mode description

FME	MM1	MM0	NAME	DESCRIPTION
0	0	0	Internal, no force mux	Input mux, offset and gain register selected from internal register bits INTM1, INTM0
0	0	1	External, no force mux	Input mux, offset and gain register selected from external pins MA1, MA0 MA1 MA0 0 0 Red 0 1 Green 1 0 Blue
0	1	0	Auto-cycling, no force mux	Input mux, offset and gain register auto-cycled, R → G → B → R on ACYC pulse.
1	0	0	Internal, force mux	Input mux selected from internal register bits FM1, FM0; offset and gain register selected from internal register bits INTM1, INTM0
1	0	1	External, force mux	Input mux selected from internal register bits FM1, FM0; offset and gain register selected from external pins MA1, MA0
1	1	0	Auto-cycling, force mux	Input mux selected from internal register bits FM1, FM0; offset and gain register auto-cycled, R → G → B → R on ACYC pulse

setup register 3 description

BIT	NAME	DEFAULT	DESCRIPTION
B1, B0	RCL1, RCL0	No default setting	These two bits control the input clamp voltage levels. RCL1 RCL0 0 0 Clamp low, 1.5 V 0 1 Clamp high, 2.5 V

software reset description

BIT	DESCRIPTION
B7–B0	Software reset, reset system to the default settings.

auto-cycle reset description

BIT	DESCRIPTION
B7–B0	In auto-cycling mode this will reset auto-cycling to RED channel, RED gain register, and RED offset register.

read-only I.D. description

BIT	NAME	DEFAULT	DESCRIPTION
B7–B0	ID		Hard-coded device revision identification. This can be read in one of the test modes.

test register description

BIT	NAME	DEFAULT	DESCRIPTION
B5–B0	RA5–RA0	00	These six bits select the internal register to be read out at the output data bus.
B7	ST	0	Self test. 1 – self-test enable, the DAC output is connected to the PGA input. 0 – self-test disable (default)
B6	RR	0	Read internal register value from the output data bus. 1 – read enable, 0 – read disable (default). When the RR bit is set to 1, the content of a register specified by RA5–RA0 can be read from the parallel data bus upper 8 bits, OP(9–2). Both the parallel and serial ports can be used to write any internal registers, but only the parallel port is used to read the registers.

PRINCIPLES OF OPERATION

DAC value registers and DAC sign register format

DSIGN = 0:	DAC coding	CIS mode DAC output	CCD mode DAC output
	0000 0000	0 V (default)	0 V (default)
	1000 0000	1.25 V	250 mV
	1111 1111	2.5 V	500 mV

DSIGN = 1:	DAC coding	CIS mode DAC output	CCD mode DAC output
	0000 0000	Not applicable	0 V (default)
	1000 0000		–250 mV
	1111 1111		–500 mV

PGA output in CCD mode: $V_{O(PGA)}$ = Gain (Vr – Vs) – V_{offset}

Offset correction performed after gain stage.

PGA output in CIS single-ended mode: $V_{O(PGA)}$ = Gain (Vs – V_{offset})

Offset correction performed before gain stage.

PGA output in CIS differential input mode: $V_{O(PGA)}$ = Gain (Signal on RIN – Signal on GIN)

No additional offset cancellation.

gain registers format

PGA coding	PGA gain
000000	1 V/V (default)
111111	5 V/V

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