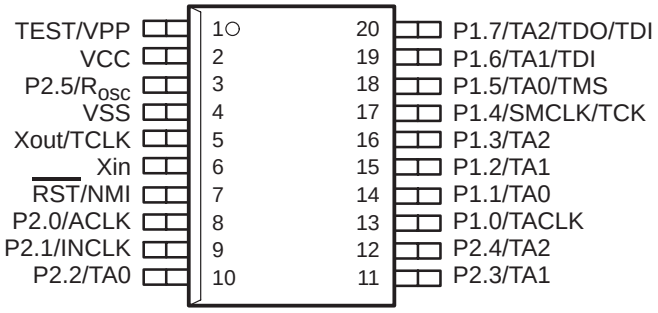
- **Low Supply Voltage Range 2.5 V – 5.5 V**
- **Ultra-Low Power Consumption**
- **Low Operation Current, 350 μA at 1 MHz,3 V**
- **Five Power Saving Modes: (Standby Mode: 1.5 μA, RAM Retention Off Mode: 0.1 μA)**
- **Wakeup From Standby Mode in 6 μs Maximum**
- **16-Bit RISC Architecture, 200 ns Instruction Cycle Time: 5 MIPS**
- **Basic Clock Module Configurations:**
  - **Various Internal Resistors**
  - **Single External Resistor**
  - **32 kHz Crystal**
  - **High Frequency Crystal**
  - **Resonator**
  - **External Clock Source**
- **Single Slope A/D Converter With External Components**
- **16-Bit Timer With 3 Capture/Compare Registers**
- **Serial Onboard Programming**
- **Program Code Protection by Security Fuse**
- **Family Members Include:**
  MSP430C111: 2k Byte ROM,128 Byte RAM†
  MSP430C112: 4k Byte ROM, 256 Byte RAM†
  MSP430P112: 4k Byte OTP, 256 Byte RAM
- **EEPROM Version Available for Prototyping:**
  - **PMS430E112: 4k Byte EROM, 256 Byte RAM**
- **Available in a 20-Pin Plastic Small-Outline Wide Body (SOWB) Package, 20-Pin Ceramic Dual-In-Line (CDIP) Package (EPROM Only)**

DW PACKAGE
(TOP VIEW)



description

The Texas Instruments MSP430 series is an ultra low-power microcontroller family consisting of several devices featuring different sets of modules targeted to various applications. The microcontroller is designed to be battery operated for an extended application lifetime. With 16-bit RISC architecture, 16 bit integrated registers on the CPU, and the constant generator, the MSP430 achieves maximum code efficiency. The digitally-controlled oscillator provides fast wakeup from all low-power modes to active mode in less than 6 μs.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and then process the data and display them or transmit them to a host system. Stand alone RF sensor front-end is another area of application. The I/O port inputs provide single slope A/D conversion capability on resistive sensors. The MSP430x11x series is an ultra low-power mixed signal microcontroller with a built in 16-bit timer and fourteen I/O pins.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

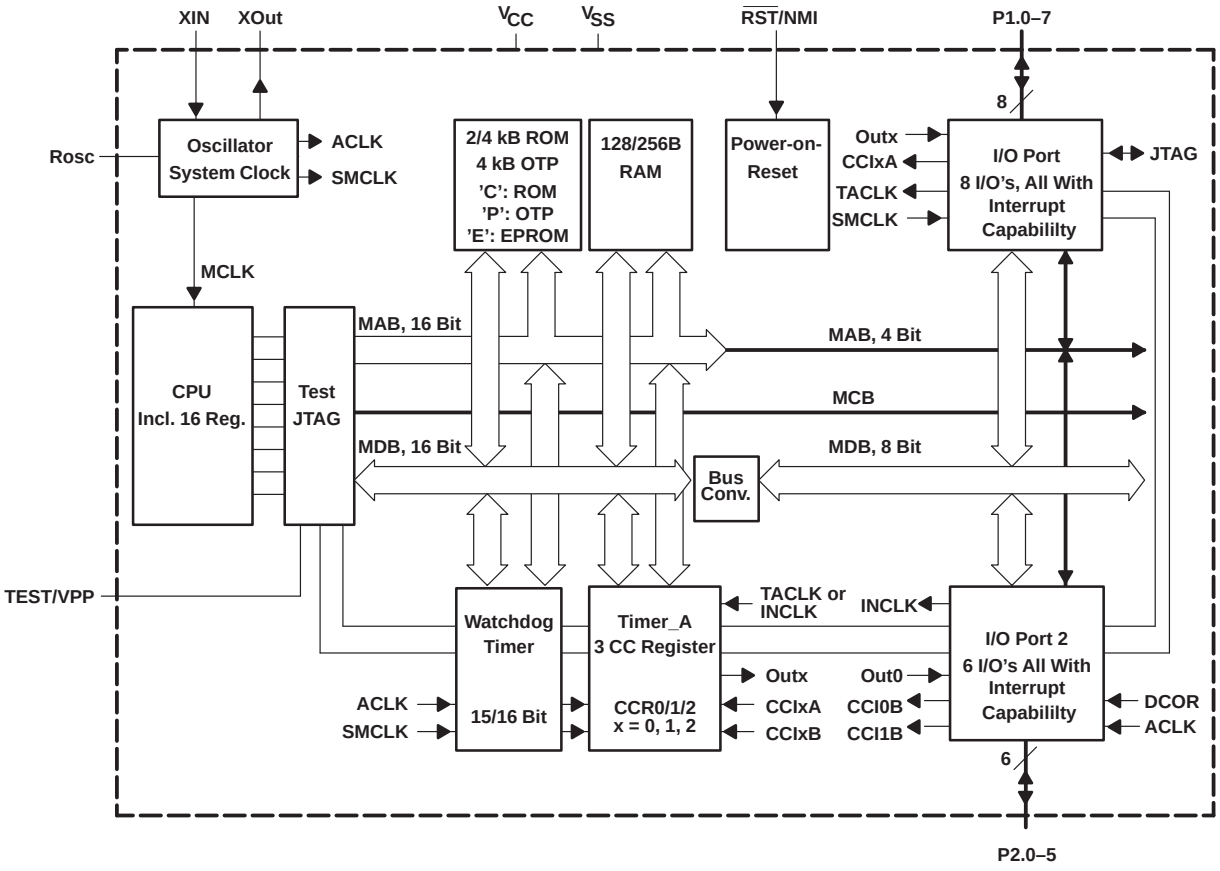
† Advanced Information

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	SOWB 20-Pin (DW)	CDIP 20-Pin (JL)
–40°C to 85°C	MSP430C111IDW† MSP430C112IDW† MSP430P112IDW	
25°C	—	PMS430E112JL

† Advanced Information

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
P1.0/TACLK	13	I/O	General-purpose digital I/O pin/Timer_A, clock signal TACLK input
P1.1/TA0	14	I/O	General-purpose digital I/O pin/Timer_A, Capture: CCI0A input, Compare: Out0 output
P1.2/TA1	15	I/O	General-purpose digital I/O pin/Timer_A, Capture: CCI1A input, Compare: Out1 output
P1.3/TA2	16	I/O	General-purpose digital I/O pin/Timer_A, Capture: CCI2A input, Compare: Out2 output
P1.4/SMCLK/TCK	17	I/O	General-purpose digital I/O pin/SMCLK signal output/Test clock, input terminal for device programming and test
P1.5/TA0/TMS	18	I/O	General-purpose digital I/O pin/Timer_, Compare: Out0 output/Test mode select, input terminal for device programming and test.
P1.6/TA1/TDI	19	I/O	General-purpose digital I/O pin/Timer_A, Compare: Out1 output/Test data input terminal.
P1.7/TA2/TDO/TDI	20	I/O	General-purpose digital I/O pin/Timer_A, Compare: Out2 output/Test data output terminal or data input during programming.
P2.0/ACLK	8	I/O	General-purpose digital I/O pin/ACLK output
P2.1/INCLK	9	I/O	General-purpose digital I/O pin/Timer_A, clock signal at INCLK
P2.2/TA0	10	I/O	General-purpose digital I/O pin/Timer_A, Capture: CCI0B input, Compare: Out0 output
P2.3/TA1	11	I/O	General-purpose digital I/O pin/Timer_A, Capture: CCI1B input, Compare: Out1 output
P2.4/TA2	12	I/O	General-purpose digital I/O pin/Timer_A, Compare: Out2 output
P2.5/R_{OSC}	3	I/O	General-purpose digital I/O pin/Input for external resistor that defines the DCO nominal frequency
$\overline{RST}$/NMI	7	I	Reset or nonmaskable interrupt input
TEST/VPP	1	I	Select of test mode for JTAG pins on Port1/programming voltage input during EPROM programming
VCC	2		Supply voltage
VSS	4		Ground reference
Xin	6	I	Input terminal of crystal oscillator
Xout/TCLK	5	I/O	Output terminal of crystal oscillator or test clock input

short-form description

processing unit

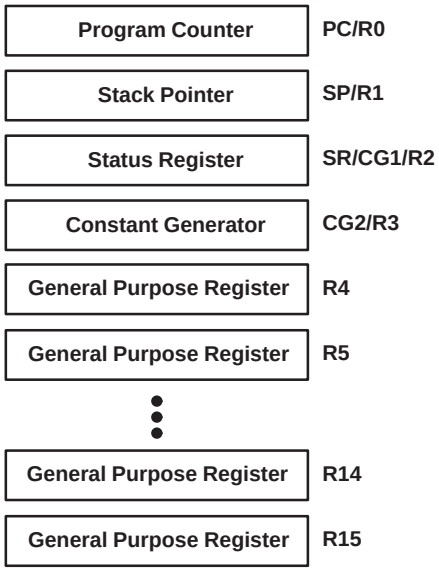
The processing unit is based on a consistent, and orthogonally designed CPU and instruction set. This design structure results in a RISC-like architecture, highly transparent to the application development and distinguished due to ease of programming. All operations other than program-flow instructions are consequently performed as register operations in conjunction with seven addressing modes for source and four modes for destination operands.

CPU

All sixteen registers are located inside the CPU, providing reduced instruction execution time. This reduces a register-register operation execution time to one cycle of the processor.

Four registers are reserved for special use as a program counter, a stack pointer, a status register, and a constant generator. The remaining twelve registers are available as general purpose registers.

Peripherals are connected to the CPU using a data address and control buses and can be handled easily with all instructions for memory manipulation.



instruction set

The instructions set for this register-register architecture provides a powerful and easy-to-use assembly language. The instruction set consists of 52 instructions with three formats and seven addressing modes. Table 1 provides a summation and example of the three types of instruction formats; the addressing modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD	R4, R5	R4 + R5 → R5
Single operands, destination only	e.g. CALL	R8	PC → (TOS), R8 → PC
Relative jump, un-/conditional	e.g. JNE		Jump-on equal bit = 0

Most instructions can operate on both word and byte data. Byte operations are identified by the suffix B.

Examples:	Instructions for word operation		Instructions for byte operation	
	MOV	EDE,TONI	MOV.B	EDE,TONI
	ADD	#235h,&MEM	ADD.B	#35h,&MEM
	PUSH	R5	PUSH.B	R5
	SWPB	R5	—	

Table 2. Address Mode Descriptions

ADDRESS MODE	s	d	SYNTAX	EXAMPLE	OPERATION
Register	√	√	MOV Rs, Rd	MOV R10, R11	R10 → R11
Indexed	√	√	MOV X(Rn), Y(Rm)	MOV 2(R5), 6(R6)	M(2 + R5) → M(6 + R6)
Symbolic (PC relative)	√	√	MOV EDE, TONI		M(EDE) → M(TONI)
Absolute	√	√	MOV &MEM, &TCDAT		M(MEM) → M(TCDAT)
Indirect	√		MOV @Rn, Y(Rm)	MOV @R10, Tab(R6)	M(R10) → M(Tab + R6)
Indirect autoincrement	√		MOV @Rn+, RM	MOV @R10+, R11	M(R10) → R11, R10 + 2 → R10
Immediate	√		MOV #X, TONI	MOV #45, TONI	#45 → M(TONI)

NOTE: s = source d = destination Rs/Rd = source register/destination register Rn = register number

short-form description (continued)

Computed branches (BR) and subroutine calls (CALL) instructions use the same addressing modes as the other instructions. These addressing modes provide *indirect* addressing, ideally suited for computed branches and calls. The full use of this programming capability permits a program structure different from conventional 8- and 16-bit controllers. For example, numerous routines can easily be designed to deal with pointers and stacks instead of using Flag type programs for flow control.

operation modes and interrupts

The MSP430 operating modes support various advanced requirements for ultra-low power and ultra-low energy consumption. This is achieved by the intelligent management of the operations during the different module operation modes and CPU states. The advanced requirements are fully supported during interrupt event handling. An interrupt event awakens the system from each of the various operating modes and returns with the *RETI* instruction to the mode that was selected before the interrupt event. The different requirements of the CPU and modules, which are driven by system cost and current consumption objectives, necessitate the use of different clock signals (see Figure 1):

- Auxiliary Clock ACLK (from LFXTCLK/crystal's frequency), used by the peripheral modules
- Main System Clock MCLK, used by the CPU and system
- Sub-System Clock SMCLK, used by the peripheral modules.

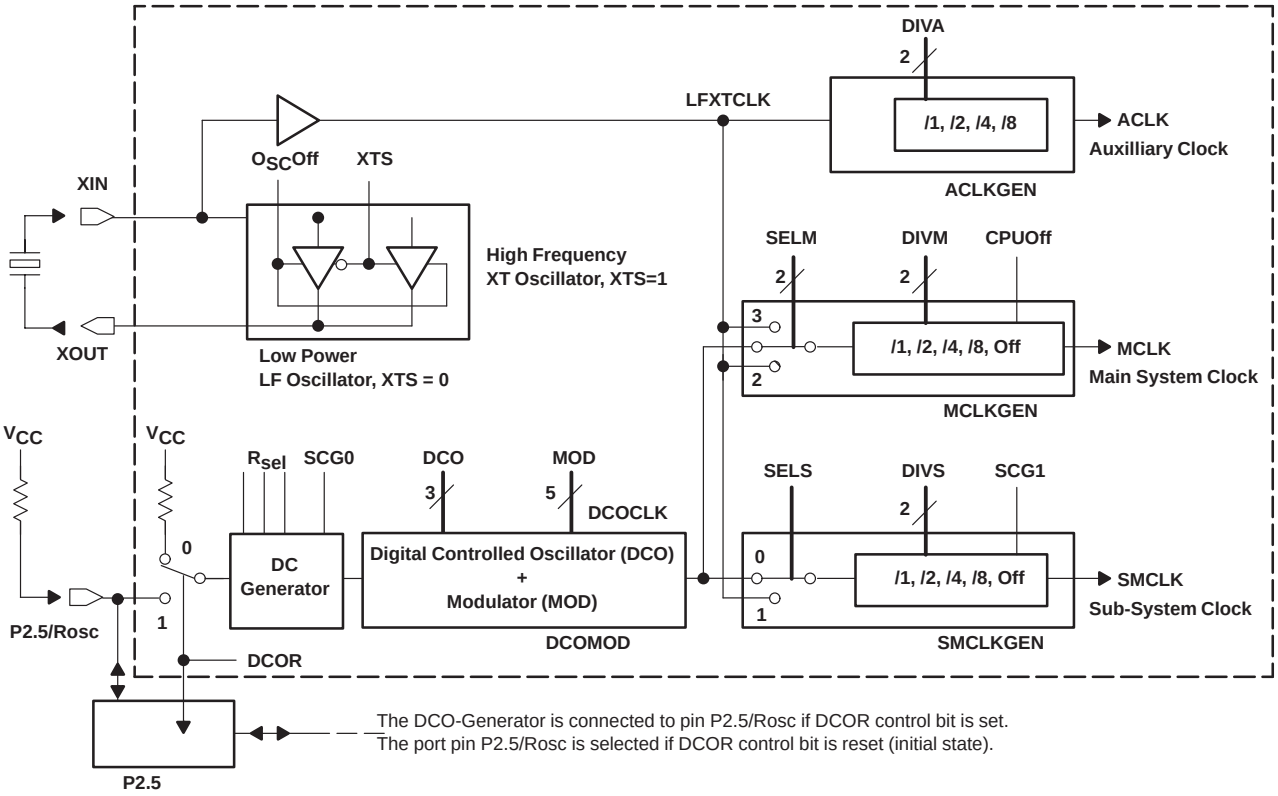


Figure 1. Clock Signals

Two clock sources, LFXTCLK and DCOCLK, can be used to drive the MSP430 system. The LFXTCLK is defined by connecting a low power, low frequency crystal to the oscillator, or by connecting a high frequency crystal to the oscillator, or by applying an external clock source. The high frequency crystal oscillator is used if the control bit XTS is set. The crystal oscillator may be switched off when the LFXTCLK oscillator is not needed for the

present operation mode. The DCOCLK is active and the frequency is selected or adjusted by the software. The DCOCLK is inactive or stopped when it is not used by the CPU or peripheral modules. The dc-generator can be stopped when SCG0 is reset and DCOCLK is not needed. The dc-generator defines the basic DCO frequency and can be defined by one external resistor or it is adjusted in eight steps with the integrated resistors.

NOTE:

The system clock generator always starts with the DCOCLK selected for MCLK (CPU clock) to ensure proper start of program execution. The software then defines the final system clock, via control bit manipulation.

low-power consumption capabilities

The various operating modes are controlled by the software through controlling the operation of the internal clock system. This clock system provides many combinations of hardware and software capabilities to run the application with the lowest power consumption and with optimized system costs:

- Use the internal clock (DCO) generator without any external components.
- Select an external crystal or ceramic resonator for lowest frequency or cost.
- Select and activate the proper clock signals (LFXTCLK and/or DCOCLK) and clock pre-divider function.
- Apply an external clock source.

Four of the control bits that influence the operation of the clock system and support fast turn-on from low power operating modes are located in the status register SR. The four bits that control the CPU and the system clock generator are SCG1, SCG0, OscOff, and CPUOff:

status register R2

15 – 9	8	7	6	5	4	3	2	1	0
Reserved For Future Enhancements	V	SCG1	SCG0	OscOff	CPUOff	GIE	N	Z	C
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

The bits CPUOff, SCG1, SCG0, and OscOff are the most important low-power control bits when the basic function of the system clock generator is established. They are pushed onto the stack whenever an interrupt is accepted and thereby saved so that the previous mode of operation can be retrieved after the interrupt request. During execution of an interrupt handler routine, the bits can be manipulated via indirect access of the data on the stack. That allows the program to resume execution in another power operating mode after the return from interrupt (RETI).

SCG1: The clock signal SMCLK, used for peripherals, is enabled when the bit is reset or disabled if the bit is set.

SCG0: The dc-generator is active when it is reset. The DCO can be deactivated only if the SCG0 bit is set and the DCOCLK signal is not used for MCLK or SMCLK. The current consumed by the dc-generator defines the basic frequency of the DCOCLK. It is a dc current.

NOTE:

When the current is switched off (SCG0=1) the start of the DCOCLK is delayed slightly. The delay is in the µs-range. See device parameters for the specified values.

OscOff: The LFXT crystal oscillator is active when the OscOff bit is reset. The LFXT oscillator can only be deactivated if the OscOff bit is set and it is not used for MCLK or SMCLK. The setup-time to start a crystal oscillation needs consideration when oscillator off option is used. Mask programmable (ROM) devices can disable this feature so that the oscillator can never be switched off by software.

CPUOff: The clock signal MCLK, used for the CPU, is active when the bit is reset or stopped if it is set.

low-power consumption capabilities (continued)

DCOCLK: The clock signal DCOCLK is deactivated if it is not used for MCLK or SMCLK or if the SCG0 bit is set. There are two situations when the SCG0 bit cannot switch off the DCOCLK signal:

1. DCOCLK frequency is used for MCLK (CPUOff=0 and SELM.1=0).
2. DCOCLK frequency is used for SMCLK (SCG1=0 and SELS=0).

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the ROM with an address range of 0FFFFh-0FFE0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up, external reset, watchdog	WDTIFG (see Note1)	Reset	0FFFEh	15, highest
NMI, oscillator fault	NMIIFG, OFIFG (see Note 1)	(non)-maskable, (non)-maskable	0FFFCh	14
			0FFFAh	13
			0FFF8h	12
			0FFF6h	11
Watchdog Timer	WDTIFG	maskable	0FFF4h	10
Timer_A	CCIFG0 (see Note 2)	maskable	0FFF2h	9
Timer_A	CCIFG1, CCIFG2, TAIFG (see Notes 1 and 2)	maskable	0FFF0h	8
			0FFEEh	7
			0FFECh	6
			0FFEAh	5
			0FFE8h	4
I/O Port P2 (eight flags – see Note 3)	P2IFG.0 to P2IFG.7 (see Notes 1 and 2)	maskable	0FFE6h	3
I/O Port P1 (eight flags)	P1IFG.0 to P1IFG.7 (see Notes 1 and 2)	maskable	0FFE4h	2
			0FFE2h	1
			0FFE0h	0, lowest

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module
3. There are eight Port P2 interrupt flags, but only six Port P2 I/O pins (P2.0–5) are implemented on the 11x devices.

special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits that are not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

interrupt enable 1

Address	7	6	5	4	3	2	1	0
0h				NMIIE			OFIE	WDTIE
				rw-0			rw-0	rw-0

WDTIE: Watchdog timer enable signal
OFIE: Oscillator fault enable signal
NMIIE: Non-maskable interrupt enable signal

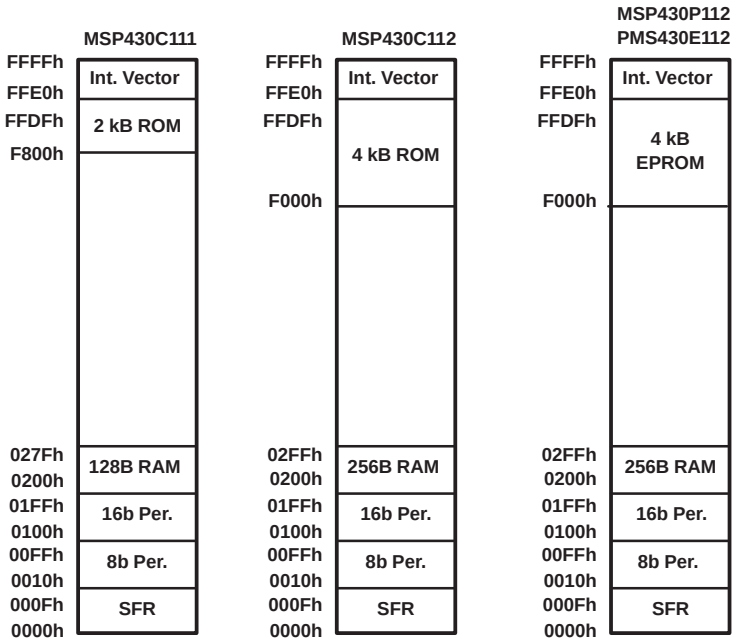
interrupt flag register 1

Address	7	6	5	4	3	2	1	0
02h				NMIIFG			OFIFG	WDTIFG
				rw-0			rw-1	rw-0

WDTIFG: Set on overflow or security key violation
OR
Reset on V_{CC} power-on or reset condition at RST/NMI-pin
OFIFG: Flag set on oscillator fault
NMIIFG: Set via $\overline{RST}$/NMI-pin

Legend		
	rw:	Bit can be read and written.
	rw-0:	Bit can be read and written. It is reset by PUC
		SFR bit is not present in device.

memory organization



peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled easily with instructions for memory manipulation.

digital I/O

There are two eight-bit I/O ports, Port P1 and Port P2 – implemented (11x parts only have six Port P2 I/O signals available on external pins). Both ports, P1 and P2, have seven control registers to give maximum flexibility of digital input/output to the application:

- All individual I/O bits are programmable independently.
- Any combination of input, output, and interrupt conditions are possible.
- Interrupt processing of external events is fully implemented for all eight bits of port P1 and for six bits of Port P2.
- Provides read/write access to all registers with all instructions.

The seven registers are:

- Input register 8 bits at Port P1/P2 contains information at the pins
- Output register 8 bits at Port P1/P2 contains output information
- Direction register 8 bits at Port P1/P2 controls direction
- Interrupt edge select 8 bits at Port P1/P2 input signal change necessary for interrupt
- Interrupt flags 8 bits at Port P1/P2 indicates if interrupt(s) are pending
- Interrupt enable 8 bits at Port P1/P2 contains interrupt enable bits
- Selection (Port or Mod.) 8 bits at Port P1/P2 determines if pin(s) have port or module function

digital I/O (continued)

All these registers contain eight bits. Two interrupt vectors are implemented: one commonly used for any interrupt event on Port P1.0 to Port P1.7, and one commonly used for any interrupt event on Port P2.0 to P2.7.

NOTE:

Six bits of Port P2, P2.0 to P2.5, are available on external pins – but all control and data bits for Port P2 are implemented.

Watchdog Timer

The primary function of the Watchdog Timer (WDT) module is to perform a controlled system restart after a software problem has occurred. If the selected time interval expires, a system reset is generated. If this watchdog function is not needed in an application, the module can work as an interval timer, which generates an interrupt after the selected time interval.

The Watchdog Timer counter (WDTCNT) is a 16-bit up-counter which is not directly accessible by S/W. The WDTCNT is controlled through the watchdog timer control register (WDTCTL), which is a 16-bit read/write register. Writing to WDTCTL is, in both operating modes (watchdog or timer), only possible by using the correct password in the high-byte. The low-byte stores data written to the WDTCTL. The high-byte must be the password 05Ah. If any value other than 05Ah is written to the high-byte of the WDTCTL, a system reset PUC is generated. When the password is read, its value is 069h, that minimizes accidental write operations to the WDTCTL register. In addition to the Watchdog Timer control bits, there are two bits included in the WDTCTL register that configure the NMI pin.

Timer_A (3 capture/compare registers)

The Timer_A module on 11x devices offers one sixteen bit counter and three capture/compare registers. The timer clock source can be selected to come from two external sources TACLK (SSEL=0) or INCLK (SSEL=3), or from two internal sources, the ACLK (SSEL=1) or SMCLK (SSEL=2). The clock source can be divided by one, two, four, or eight. The timer can be fully controlled (in word mode) since it can be halted, read, and written. It can be stopped, run continuously, counted up or up/down, using one compare block to determine the period. The three capture/compare blocks are configured by the application to run in capture or compare mode.

The capture mode is primarily used to measure external or internal events using any combination of positive, negative, or both edges of the signal. Capture mode can be started and stopped by software. Three different external events TA0, TA1, and TA2 can be selected. At capture/compare register CCR2 the ACLK is the capture signal if CCI2B is selected. Software capture is chosen if CCISx=2 or CCISx=3 (see Figure 2).

The compare mode is primarily used to generate timings for the software or application hardware, or to generate pulse-width modulated output signals for various purposes like D/A conversion functions or motor control. An individual output module is assigned to each of the three capture/compare registers. The output modules can run independently of the compare function, or can be triggered in several ways.

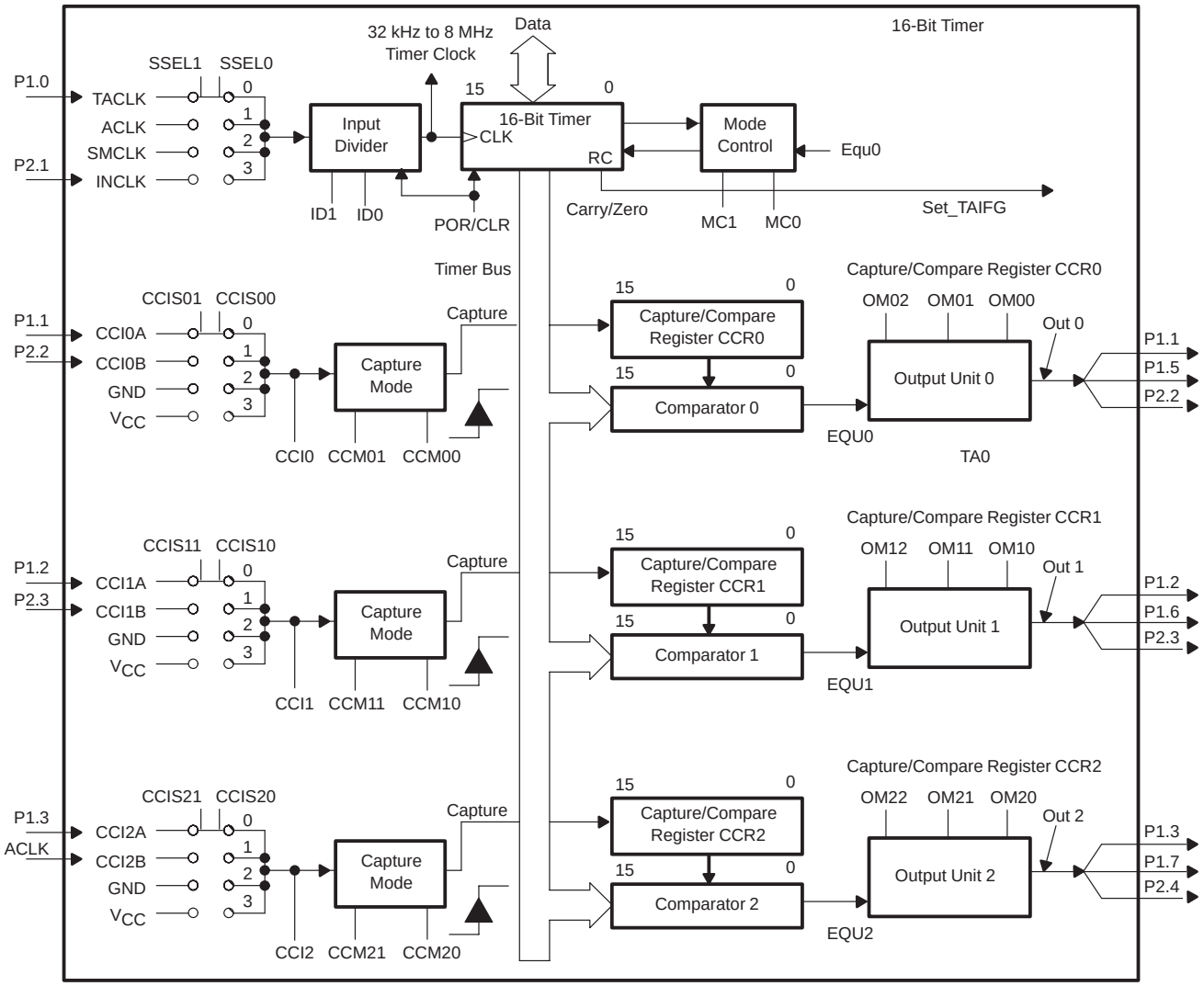


Figure 2. Timer_A, MSP430x11x Configuration

Two interrupt vectors are used by the Timer_A module. One individual vector is assigned to capture/compare block CCR0, and one common interrupt vector is implemented for the timer and the other two capture/compare blocks. The three interrupt events using the same vector are identified by an individual interrupt vector word. The interrupt vector word is used to add an offset to the program counter to continue the interrupt handler software at the corresponding program location. This simplifies the interrupt handler and gives each interrupt event the same overhead of 5 cycles in the interrupt handler.

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog/Timer Control	WDTCTL	0120h
Timer_A	Timer_A Interrupt Vector	TAIV	012Eh
	Timer_A Control	TACTL	0160h
	Cap/Com Control	CCTL0	0162h
	Cap/Com Control	CCTL1	0164h
	Cap/Com Control	CCTL2	0166h
	Reserved		0168h
	Reserved		016Ah
	Reserved		016Ch
	Reserved		016Eh
	Timer_A Register	TAR	0170h
	Cap/Com Register	CCR0	0172h
	Cap/Com Register	CCR1	0174h
	Cap/Com Register	CCR2	0176h
	Reserved		0178h
	Reserved		017Ah
	Reserved		017Ch
	Reserved		017Eh
PERIPHERALS WITH BYTE ACCESS			
System Clock	Basic Clock Sys. Control2	BCSCTL2	058h
	Basic Clock Sys. Control1	BCSCTL1	057h
	DCO Clock Freq. Control	DCOCTL	056h
EPROM	EPROM Control	EPCTL	054h
Port P2	Port P2 Selection	P2SEL	02Eh
	Port P2 Interrupt Enable	P2IE	02Dh
	Port P2 Interrupt Edge Select	P2IES	02Ch
	Port P2 Interrupt Flag	P2IFG	02Bh
	Port P2 Direction	P2DIR	02Ah
	Port P2 Output	P2OUT	029h
	Port P2 Input	P2IN	028h
Port P1	Port P1 Selection	P1SEL	026h
	Port P1 Interrupt Enable	P1IE	025h
	Port P1 Interrupt Edge Select	P1IES	024h
	Port P1 Interrupt Flag	P1IFG	023h
	Port P1 Direction	P1DIR	022h
	Port P1 Output	P1OUT	021h
	Port P1 Input	P1IN	020h
Special Function	SFR Interrupt Flag1	IFG1	002h
	SFR Interrupt Enable1	IE1	000h

absolute maximum ratings

Voltage applied at V_{CC} to V_{SS} . . . . . –0.3 V to 6 V
Voltage applied to any pin (referenced to V_{SS}) . . . . . –0.3 V to V_{CC}+0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature, T_{stg} (unprogrammed device) . . . . . –55°C to 150°C
Storage temperature, T_{stg} (programmed device) . . . . . –40°C to 85°C

recommended operating conditions

		MIN	NOM	MAX	UNITS
Supply voltage, V_{CC}	MSP430C11x	2.5		5.5	V
	MSP430P112	2.7		5.5	
	PMS430E112	2.7		5.5	V
Supply voltage, V_{SS}		0.0		0.0	V
Operating free-air temperature range, T_A	MSP430C11x	–40		85	°C
	MSP430P112				
	PMS430E112		25		
XTAL frequency, $f_{(XTAL)}$,(ACLK signal)			32 768		Hz
Processor frequency $f_{(system)}$ (MCLK signal)	V_{CC} = 3 V	dc		2.73	MHz
	V_{CC} = 5 V	dc		5.35	

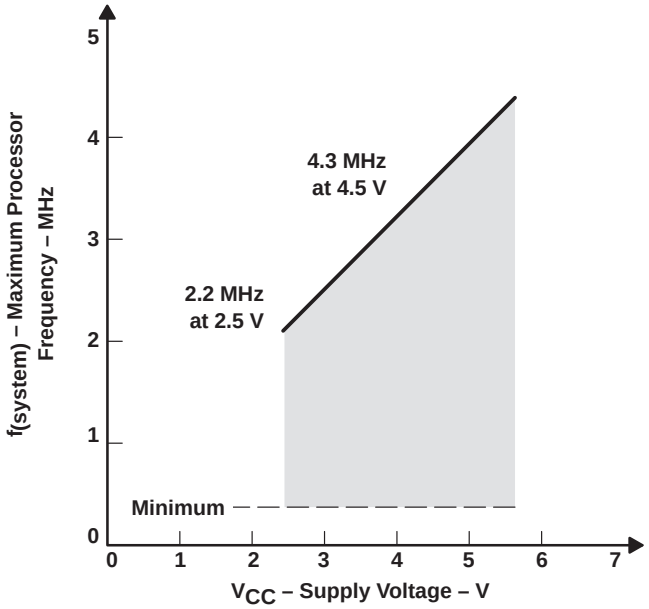


Figure 3. Frequency vs Supply Voltage

NOTE: Minimum processor frequency is defined by system clock.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

supply current (into V_{CC}) excluding external current ($f_{(system)}$ = 1 MHz)

PARAMETER			TEST CONDITIONS			MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active Mode	C11x	T_A = –40°C +85°C, $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz		V_{CC} = 3 V		330	400	µA
					V_{CC} = 5 V		630	700	
			T_A = –40°C +85°C, $f_{(MCLK)} = f_{(SMCLK)} = f_{(ACLK)}$ = 4096 Hz		V_{CC} = 3 V		3.4	4	µA
					V_{CC} = 5 V		7.8	10	
		P112	T_A = –40°C +85°C, $f_{MCLK} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz		V_{CC} = 3 V		400	500	µA
					V_{CC} = 5 V		730	900	
			T_A = –40°C +85°C, $f_{(MCLK)} = f_{(SMCLK)} = f_{(ACLK)}$ = 4096 Hz		V_{CC} = 3 V		3.4	4	µA
					V_{CC} = 5 V		7.8	10	
$I_{(CPUOff)}$	Low power mode, (LPM0)	C11x	T_A = –40°C +85°C, f_{MCLK} = 0 MHz, $f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz		V_{CC} = 3 V		51	60	µA
					V_{CC} = 5 V		120	150	
		P112	T_A = –40°C +85°C, $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz		V_{CC} = 3 V		70	85	
					V_{CC} = 5 V		125	170	
$I_{(LPM2)}$	Low power mode, (LPM2)		T_A = –40°C +85°C, $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 0, Rsel = 3		V_{CC} = 3 V		8	22	µA
					V_{CC} = 5 V		16	35	
$I_{(LPM3)}$	Low power mode, (LPM3)		T_A = –40°C	$f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1	V_{CC} = 3 V		2	2.6	µA
			T_A = 25°C				1.5	2.2	
			T_A = 85°C				1.85	2.2	
			T_A = –40°C	$f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1	V_{CC} = 5 V		6.3	8	
			T_A = 25°C				5.1	7	
			T_A = 85°C				5.1	7	
$I_{(LPM4)}$	Low power mode, (LPM4)		T_A = –40°C	$f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1	V_{CC} = 3 V/ 5 V		0.1	0.8	µA
			T_A = 25°C				0.1	0.8	
			T_A = 85°C				0.4	1	

NOTE: All inputs are tied to V_{SS} or V_{CC}. Outputs do not source or sink any current.

Current consumption of active mode versus system frequency, C versions only

$$I_{AM} = I_{AM[1\ MHz]} \times f_{system}\ [MHz]$$

Current consumption of active mode versus supply voltage, C versions only

$$I_{AM} = I_{AM[3\ V]} + 175\ \mu A/V \times (V_{CC} - 3\ V)$$

schmitt-trigger inputs Port 1 to Port P2; P1.0 to P1.7, P2.0 to P2.5

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3 V	1.2		2.1	V
		V_{CC} = 5 V	2.3		3.4	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 3 V	0.7		1.5	V
		V_{CC} = 5 V	1.4		2.3	
$V_{IT+} - V_{IT-}$	Input voltage differential, (hysteresis)	V_{CC} = 3 V	0.3		1	V
		V_{CC} = 5 V	0.6		1.4	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

standard inputs TCK, TMS, TDI, $\overline{RST}$/NMI

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{IL}	Low-level input voltage	V_{CC} = 3 V/5 V	V_{SS}		V_{SS}+0.8	V
V_{IH}	High-level input voltage		0.7V_{CC}		V_{CC}	V

outputs Port 1 to P2; P1.0 to P1.7, P2.0 to P2.5

PARAMETER		TEST CONDITIONS			MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = – 1.5 mA,	V_{CC} = 3 V/5 V,	See Note 4	V_{CC}–0.4		V_{CC}	V
		$I_{(OHmax)}$ = – 4.5 mA,	V_{CC} = 3 V/5 V,	See Note 5	V_{CC}-0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1.5 mA,	V_{CC} = 3 V/5 V,	See Note 4	V_{SS}		V_{SS}+0.4	V
		$I_{(OLmax)}$ = 4.5 mA,	V_{CC} = 3 V/5 V,	See Note 5	V_{SS}		V_{SS}+0.6	

NOTES: 4. The maximum total current, I_{OH}max and I_{OL}max, or all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
5. The maximum total current, I_{OH}max and I_{OL}max, or all outputs combined, should not exceed ±36 mA to hold the maximum voltage drop specified.

leakage current (see Note 6)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{lkg(LPx.x)}$	High-impendance leakage current	Port P1: P1.x, 0 ≤ × ≤ 7 (see Note 7)	V_{CC} = 3 V/5 V,			±50	nA
		Port P2: P2.x, 0 ≤ × ≤ 5 (see Note 7)	V_{CC} = 3 V/5 V,			±50	

NOTES: 6. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
7. The leakage of the digital port pins is measured individually. The port pin must be selected for input and there must be no optional pull-up or pull-down resistor.

optional resistors, individually programmable with ROM code (see Note 8)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$R_{(opt1)}$	Resistors, individually programmable with ROM code, all port pins, values applicable for pull-down and pull-up	V_{CC} = 3 V/5 V	1.2	2.4	4.8	kΩ
$R_{(opt2)}$		V_{CC} = 3 V/5 V	1.8	3.6	7.2	kΩ
$R_{(opt3)}$		V_{CC} = 3 V/5 V	3.6	7.3	14.6	kΩ
$R_{(opt4)}$		V_{CC} = 3 V/5 V	5.5	11	22	kΩ
$R_{(opt5)}$		V_{CC} = 3 V/5 V	11	22	44	kΩ
$R_{(opt6)}$		V_{CC} = 3 V/5 V	22	44	88	kΩ
$R_{(opt7)}$		V_{CC} = 3 V/5 V	33	66	132	kΩ
$R_{(opt8)}$		V_{CC} = 3 V/5 V	55	110	220	kΩ
$R_{(opt9)}$		V_{CC} = 3 V/5 V	77	154	310	kΩ
$R_{(opt10)}$		V_{CC} = 3 V/5 V	100	200	400	kΩ

NOTE 8: Optional resistors R_{optx} for pull-down or pull-up are not programmed in standard OTP or EPROM devices MSP430P112 or PMS430E112.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

inputs Px.x, TAx

PARAMETER		TEST CONDITIONS	VCC	MIN	NOM	MAX	UNIT
$t_{(int)}$	External Interrupt timing	Port P1, P2: P1.x to P2.x, External trigger signal for the interrupt flag, (see Note 9)	3 V/ 5 V	1.5			cycle
			3 V	540			ns
			5 V	270			
$t_{(cap)}$	Timer_A, capture timing	TA0, TA1, TA2. (see Note 10)	3 V/ 5 V	1.5			cycle
			3 V	540			ns
			5 V	270			

NOTES: 9. The external signal sets the interrupt flag every time the minimum t_{int} cycle and time parameters are met. It may be set even with trigger signals shorter than t_{int}. Both the cycle and timing specifications must be met to ensure the flag is set.

10. The external capture signal triggers the capture event every time when the minimum t_{cap} cycles and time parameters are met. A capture may be triggered with capture signals even shorter than t_{cap}. Both the cycle and timing specifications must be met to ensure a correct capture of the 16-bit timer value and to ensure the flag is set.

internal signals TAx, SMCLK at Timer_A

PARAMETER		TEST CONDITIONS	VCC	MIN	NOM	MAX	UNIT
$f_{(IN)}$	Input frequency	Internal TA0, TA1, TA2, $t_H = t_L$	3 V	dc		10	MHz
			5 V	dc		15	
$f_{(TAint)}$	Timer_A clock frequency	Internally, SMCLK signal applied	3 V/5 V	dc		f_{System}	

outputs P2x, TAx

PARAMETER		TEST CONDITIONS		VCC	MIN	NOM	MAX	UNIT
$f_{(P20)}$	Output frequency	P2.0/ACLK,	C_L = 20 pF	3 V/5 V			1.1	MHz
$f_{(TAx)}$		TA0, TA1, TA2,	C_L = 20 pF	3 V/5 V	dc		f_{System}	
$t_{(Xdc)}$	Duty cycle of O/P frequency	P2.0/ACLK, C_L = 20 pF	f_{P20} = 1.1 MHz	3 V/ 5 V	40%		60%	
			$f_{P20} = f_{XTCLK}$		35%		65%	
			$f_{P20} = f_{XTCLK/n}$			50%		
$t_{(TAdc)}$		TA0, TA1, TA2, Duty cycle = 50%	C_L = 20 pF,	3 V/ 5 V		0	±50	ns

PUC/POR

PARAMETER		TEST CONDITIONS	VCC	MIN	NOM	MAX	UNIT
$t_{(POR-delay)}$	POR		3 V/5 V		150	200	µs
$V_{(POR)}$				1.1		2.4	V
$V_{(min)}$				0		0.4	
$t_{(reset)}$		Reset is accepted internally, PUC/POR	3 V/5 V	2			µs

crystal oscillator, Xin, Xout

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$C_{(Xin)}$	Capacitance at input	V_{CC} = 3 V/5 V		12		pF
$C_{(Xout)}$	Capacitance at output	V_{CC} = 3 V/5 V		12		pF
$V_{I(XINL)}$	Input levels at XIN, XOUT	V_{CC} = 3 V/5 V	V_{SS}		$0.2 \times V_{CC}$	V
$V_{I(XINH)}$			$0.8 \times V_{CC}$		V_{CC}	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

RAM

PARAMETER		MIN	NOM	MAX	UNIT
$V_{(RAMh)}$	CPU halted (see Note 11)	1.8			V

NOTE 11: This parameter defines the minimum supply voltage V_{CC} when the data in the program memory RAM remains unchanged. No program execution should happen during this supply voltage condition.

DCO

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{(DCO03)}$	R_{sel} = 0, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V		0.12		MHz
		V_{CC} = 5 V		0.13		
$f_{(DCO13)}$	R_{sel} = 1, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V		0.19		MHz
		V_{CC} = 5 V		0.21		
$f_{(DCO23)}$	R_{sel} = 2, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V		0.31		MHz
		V_{CC} = 5 V		0.34		
$f_{(DCO33)}$	R_{sel} = 3, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V		0.5		MHz
		V_{CC} = 5 V		0.55		
$f_{(DCO43)}$	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V	0.5	0.8	1.1	MHz
		V_{CC} = 5 V	0.6	0.9	1.2	
$f_{(DCO53)}$	R_{sel} = 5, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V	0.9	1.2	1.55	MHz
		V_{CC} = 5 V	1.1	1.4	1.7	
$f_{(DCO63)}$	R_{sel} = 6, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V	1.7	2	2.3	MHz
		V_{CC} = 5 V	2.1	2.4	2.7	
$f_{(DCO73)}$	R_{sel} = 7, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V	2.8	3.1	3.5	MHz
		V_{CC} = 5 V	3.8	4.2	4.5	
$f_{(DCO47)}$	R_{sel} = 4, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V/5 V	F_{DCO40} x1.8	F_{DCO40} x2.2	F_{DCO40} x2.6	MHz
$S_{(Rsel)}$	$S_R = f_{Rsel+1}/f_{Rsel}$	V_{CC} = 3 V/5 V	1.4	1.65	1.9	ratio
$S_{(DCO)}$	$S_{DCO} = f_{DCO+1}/f_{DCO}$	V_{CC} = 3 V/5 V	1.07	1.12	1.16	
D_t	Temperature drift, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 12)	V_{CC} = 3 V	–0.31	–0.36	–0.40	%/°C
		V_{CC} = 5 V	–0.33	–0.38	–0.43	
D_V	Drift with V_{CC} variation, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 12)	V_{CC} = 3 V to 5 V	0	5	10	%/V

NOTE 12: These parameters are not production tested.

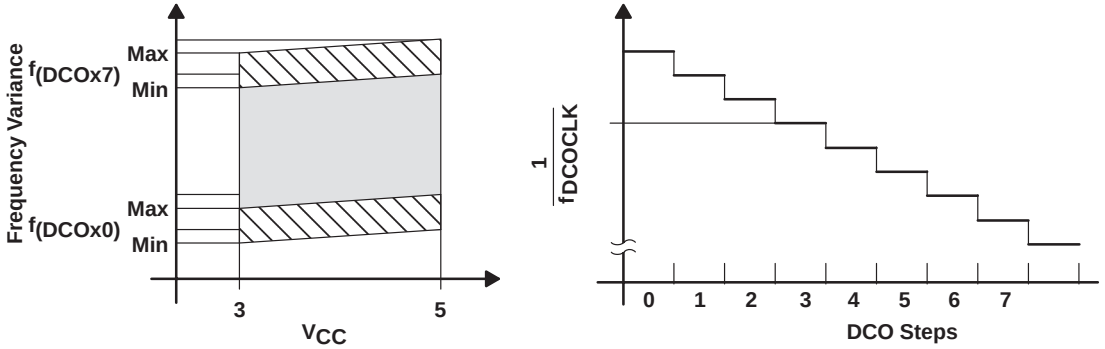


Figure 4. DCO Characteristics

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

principle characteristics of the DCO

- Individual devices have a minimum and maximum operation frequency. The specified parameters for f_{DCOx0} to f_{DCOx7} are valid for all devices.
- The ranges selected by R_{sel4} to R_{sel5}, R_{sel5} to R_{sel6}, and R_{sel6} to R_{sel7} are overlapping.
- The DCO control bits DCO0, DCO1 and DCO2 have a step size as defined in parameter S_{DCO}.
- The modulation control bits MOD0 to MOD4 select how often f_{DCO+1} is used within the period of 32 DCOCLK cycles. f_{DCO} is used for the remaining cycles. The frequency is an average = $f_{DCO} \times (2^{MOD/32})$.

wake-up from lower power modes (LPMx)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$t_{(LPM0)}$/ $t_{(LPM2)}$	Delay time		V_{CC} = 3 V/5 V		100		ns
$t_{(LPM3)}$		R_{Sel} = 4, DCO = 3, MOD = 0	V_{CC} = 3 V/5 V		2.6	6	µs
$t_{(LPM4)}$		R_{Sel} = 4, DCO = 3, MOD = 0	V_{CC} = 3 V/5 V		2.8	6	µs

JTAG/programming

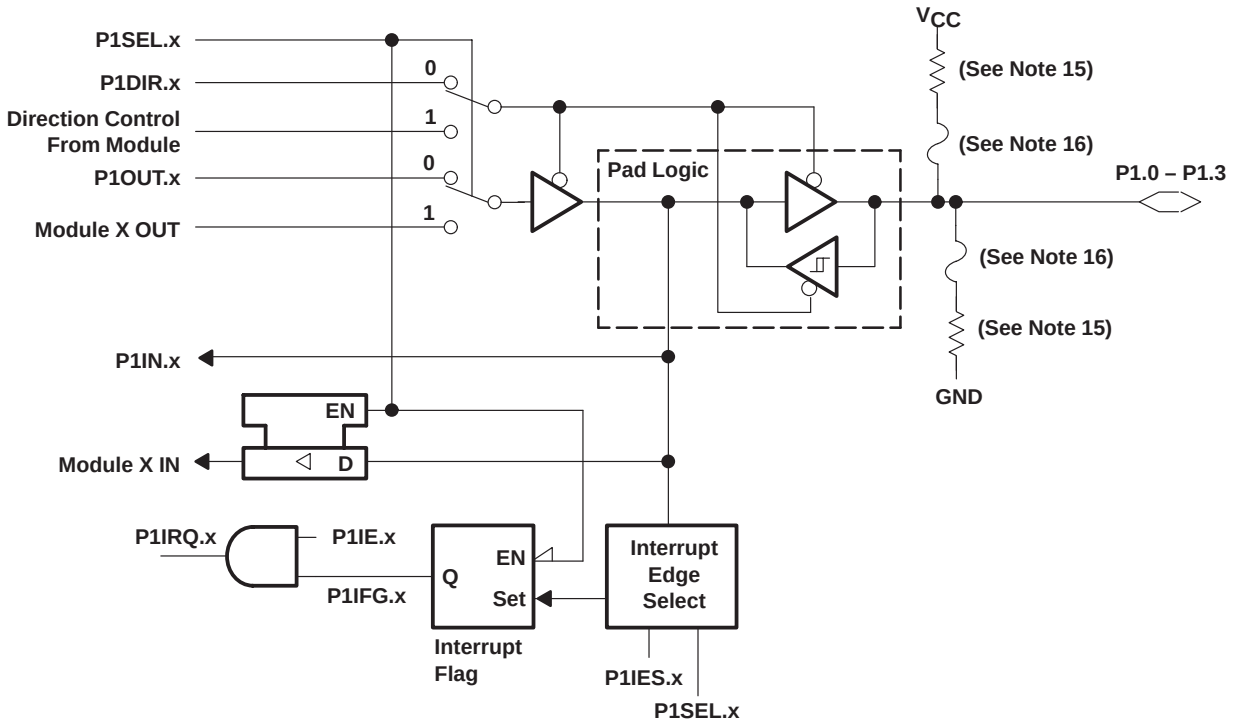
PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{(TCK)}$	JTAG/Test	TCK frequency	V_{CC} = 3 V	dc		5	MHz
			V_{CC} = 5 V	dc		10	
$V_{(FB)}$	JTAG/Fuse (see Note 13)	Fuse blow voltage, C versions (see Note 14)	V_{CC} = 3 V/ 5 V	5.5		6	V
		Fuse blow voltage, E/P versions (see Note 14)	V_{CC} = 3 V/ 5 V	11		12	
$I_{(FB)}$		Supply current on Test/VPP during fuse is blown				100	mA
$t_{(FB)}$		Time to blow the fuse				1	ms
$V_{(PP)}$	EPROM P- and E-versions only	Programming Voltage, applied to Test/VPP	V_{CC} = 3 V/ 5 V	11	11.5	12	V
$I_{(PP)}$		Current from programming voltage source	V_{CC} = 3 V/ 5 V			70	mA
$t_{(pps)}$		Programming time, single pulse	V_{CC} = 3 V/ 5 V	5			ms
$t_{(ppf)}$		Programming time, fast algorithm	V_{CC} = 3 V/ 5 V		100		µs
$P_{(n)}$		Number of pulses for successful programming	V_{CC} = 3 V/ 5 V	4		100	
$t_{(erase)}$		Erase time wave length 2537 Å at 15 Ws/cm^2 (UV lamp of 12 mW/ cm^2)		30			min
		Write/Erase cycles		1000			
		Data retention Tj < 55°C		10			Year

NOTES: 13. Once the JTAG fuse is blown no further access to the MSP430 JTAG/Test feature is possible. The JTAG block is switched to By-Pass mode.
14. The power source to blow the fuse is applied to Test/VPP pin during blowing the fuse.

APPLICATION INFORMATION

input/output schematic

Port P1, P1.0 to P1.3, input/output with Schmitt-trigger



NOTE: x = Bit Identifier, 0 to 3 For Port P1

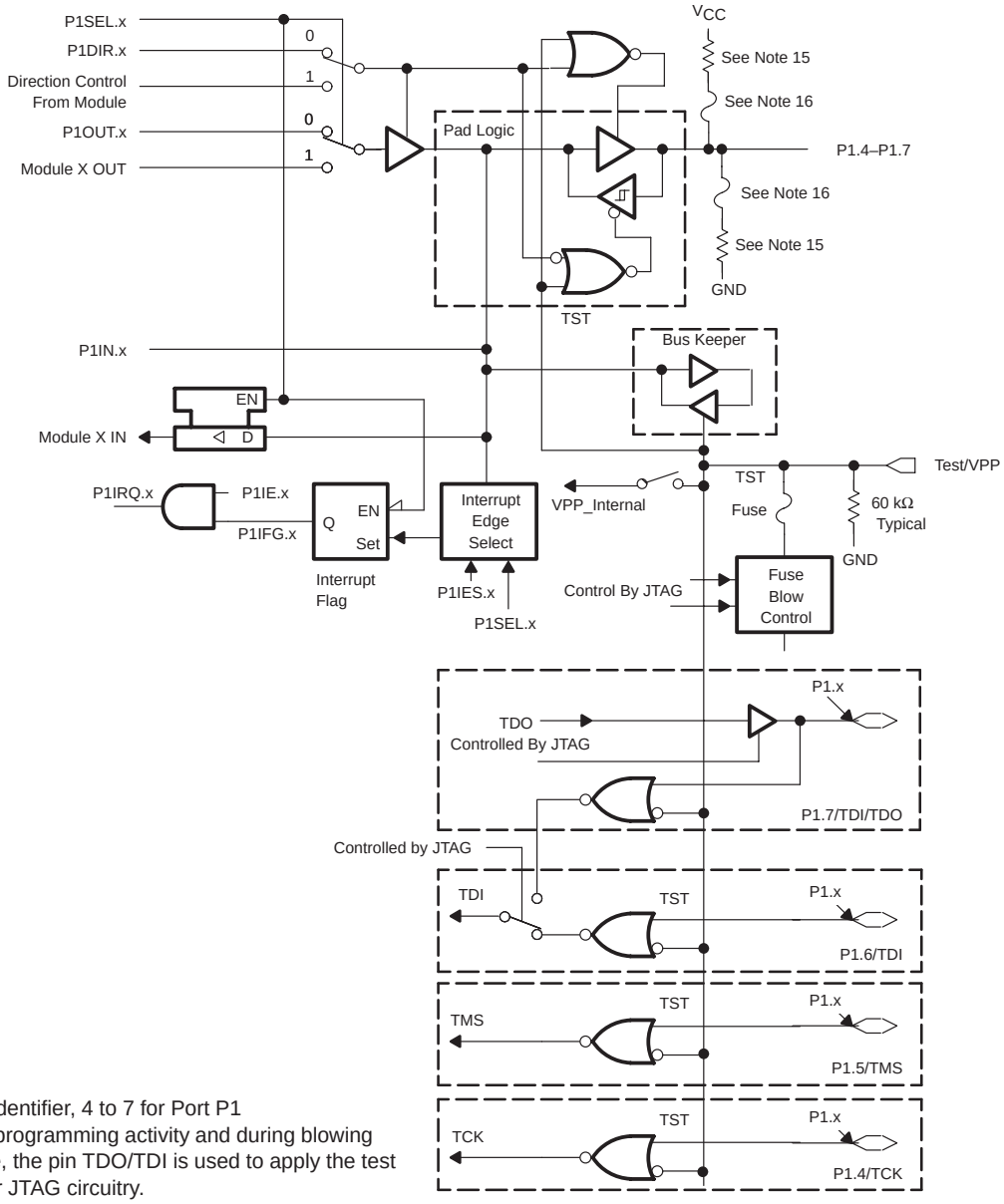
PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.0	P1DIR.0	P1DIR.0	P1OUT.0	VSS	P1IN.0	TACLK†	P1IE.0	P1IFG.0	P1IES.0
P1Sel.1	P1DIR.1	P1DIR.1	P1OUT.1	Out0 signal†	P1IN.1	CCI0A†	P1IE.1	P1IFG.1	P1IES.1
P1Sel.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 signal†	P1IN.2	CCI1A†	P1IE.2	P1IFG.2	P1IES.2
P1Sel.3	P1DIR.3	P1DIR.3	P1OUT.3	Out2 signal†	P1IN.3	CCI2A†	P1IE.3	P1IFG.3	P1IES.3

† Signal from or to Timer_A

NOTES: 15. Optional selection of pull-up or pull-down resistors with ROM (masked) versions.
16. Fuses for optional pull-up and pull-down resistors can only be programmed at the factory.

APPLICATION INFORMATION

Port P1, P1.4 to P1.7, input/output with Schmitt-trigger and in-system access features



NOTE: x = Bit identifier, 4 to 7 for Port P1
During programming activity and during blowing the fuse, the pin TDO/TDI is used to apply the test input for JTAG circuitry.

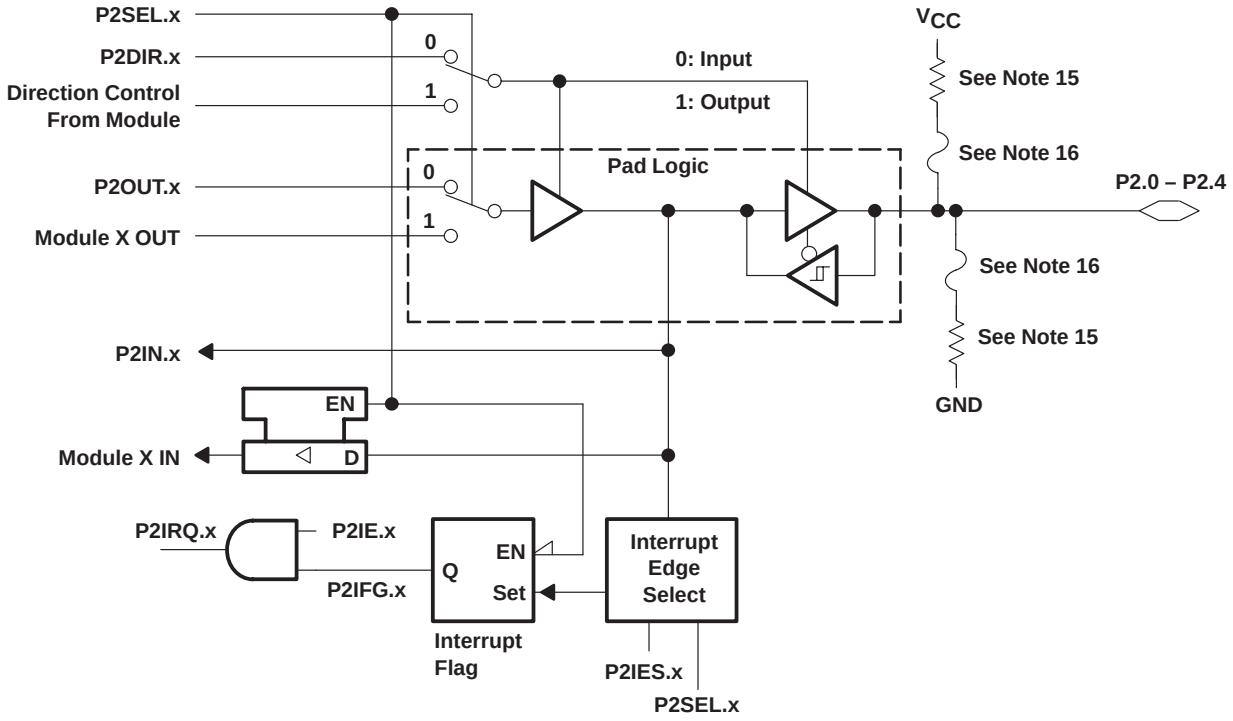
PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.4	P1DIR.4	P1DIR.4	P1OUT.4	SMCLK	P1IN.4	unused	P1IE.4	P1IFG.4	P1IES.4
P1Sel.5	P1DIR.5	P1DIR.5	P1OUT.5	Out0 signal†	P1IN.5	unused	P1IE.5	P1IFG.5	P1IES.5
P1Sel.6	P1DIR.6	P1DIR.6	P1OUT.6	Out1 signal†	P1IN.6	unused	P1IE.6	P1IFG.6	P1IES.6
P1Sel.7	P1DIR.7	P1DIR.7	P1OUT.7	Out2 signal†	P1IN.7	unused	P1IE.7	P1IFG.7	P1IES.7

† Signal from or to Timer_A

NOTES: 15. Optional selection of pull-up or pull-down resistors with ROM (masked) versions.
16. Fuses for optional pull-up and pull-down resistors can only be programmed at the factory.

APPLICATION INFORMATION

Port P2, P2.0 to P2.4, input/output with Schmitt-trigger



NOTE: x = Bit Identifier, 0 to 4 For Port P2

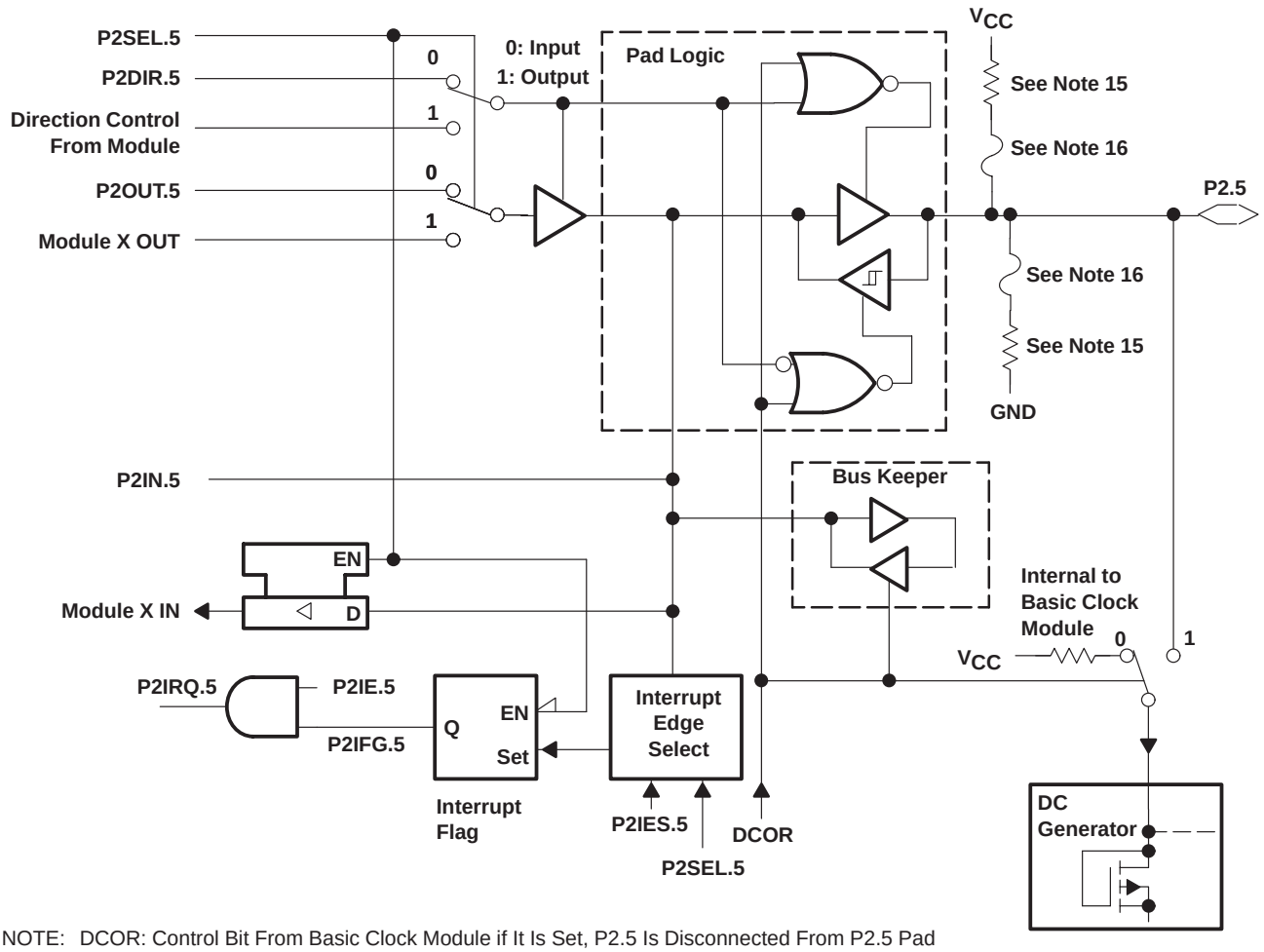
PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	ACLK	P2IN.0	unused	P2IE.0	P2IFG.0	P1IES.0
P2Sel.1	P2DIR.1	P2DIR.1	P2OUT.1	VSS	P2IN.1	INCLK†	P2IE.1	P2IFG.1	P1IES.1
P2Sel.2	P2DIR.2	P2DIR.2	P2OUT.2	Out0 signal†	P2IN.2	CCI0B†	P2IE.2	P2IFG.2	P1IES.2
P2Sel.3	P2DIR.3	P2DIR.3	P2OUT.3	Out1 signal†	P2IN.3	CCI1B†	P2IE.3	P2IFG.3	P1IES.3
P2Sel.4	P2DIR.4	P2DIR.4	P2OUT.4	Out2 signal†	P2IN.4	unused	P2IE.4	P2IFG.4	P1IES.4

† Signal from or to Timer_A

NOTES: 15. Optional selection of pull-up or pull-down resistors with ROM (masked) versions.
16. Fuses for optional pull-up and pull-down resistors can only be programmed at the factory.

APPLICATION INFORMATION

Port P2, P2.5, input/output with Schmitt-trigger and R_{OSC} function for the Basic Clock module



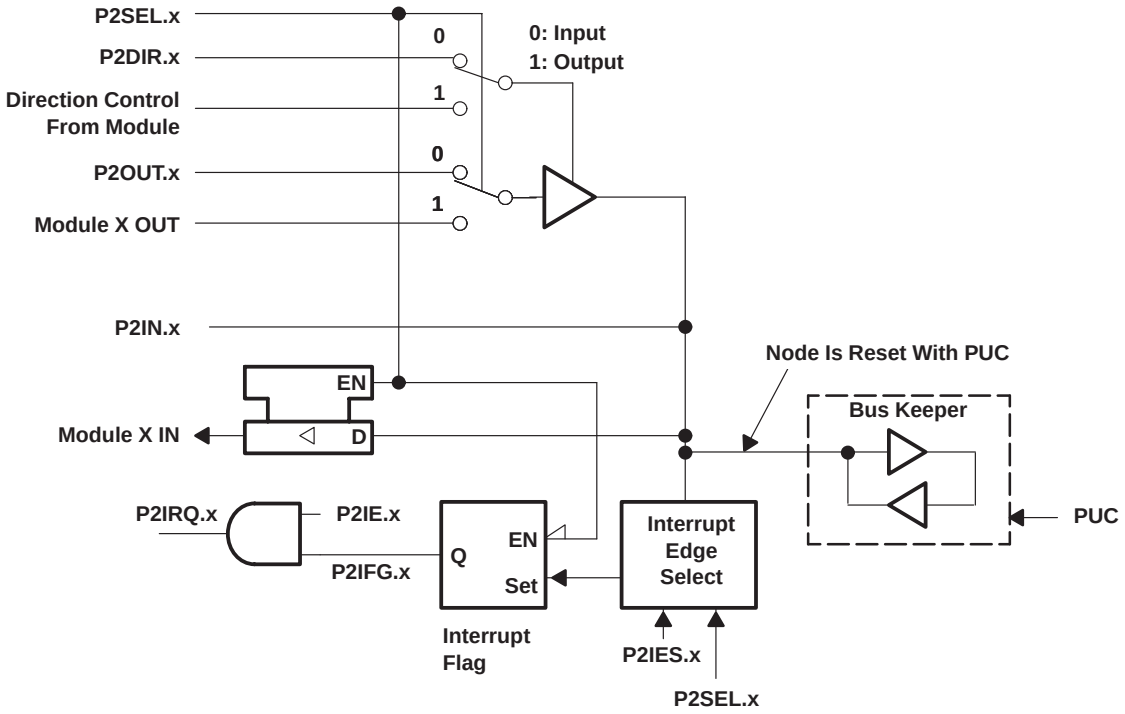
NOTE: DCOR: Control Bit From Basic Clock Module if It Is Set, P2.5 Is Disconnected From P2.5 Pad

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.5	P2DIR.5	P2DIR.5	P2OUT.5	VSS	P2IN.5	unused	P2IE.5	P2IFG.5	P2IES.5

NOTES: 15. Optional selection of pull-up or pull-down resistors with ROM (masked) versions.
16. Fuses for optional pull-up and pull-down resistors can only be programmed at the factory.

APPLICATION INFORMATION

Port P2, un-bonded bits P2.6 and P2.7



NOTE: x = Bit Identifier, 6 to 7 for Port P2 without external pins

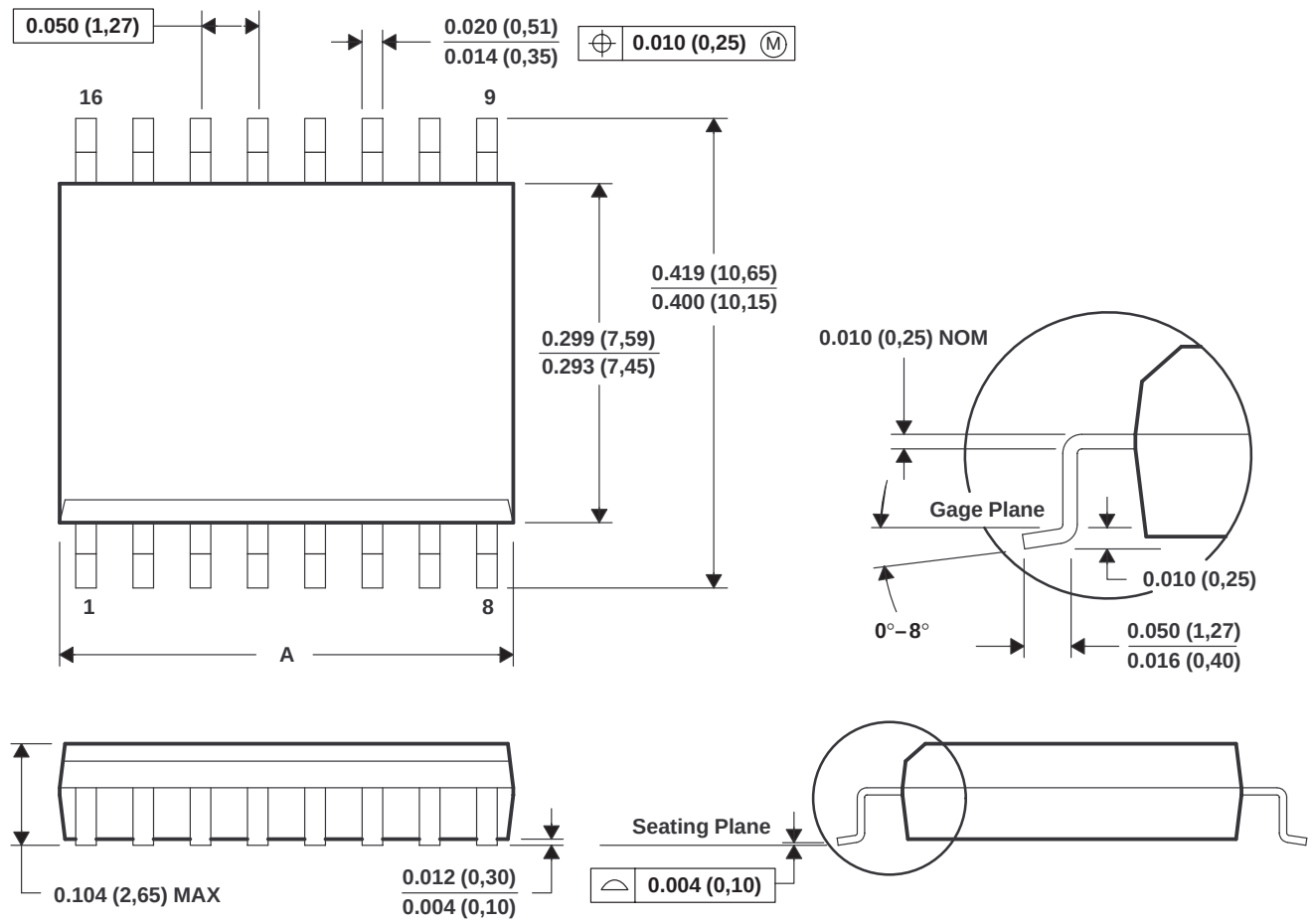
P2Sel.x	P2DIR.x	Dir. Control from module	P2OUT.x	Module X OUT	P2IN.x	Module X IN	P2IE.x	P2IFG.x	P2IES.x
P2Sel.6	P2DIR.6	P2DIR.6	P2OUT.6	VSS	P2IN.6	unused	P2IE.6	P2IFG.6	P2IES.6
P2Sel.7	P2DIR.7	P2DIR.7	P2OUT.7	VSS	P2IN.7	unused	P2IE.7	P2IFG.7	P2IES.7

NOTE: A good use of the unbonded bits 6 and 7 of port P2 is to use the interrupt flags. The interrupt flags can not be influenced from any signal other than from software. They work then as soft interrupt.

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN



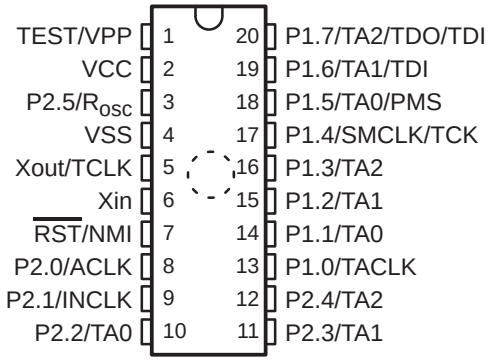
DIM \ PINS **	16	20	24
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)

4040000/D 02/98

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

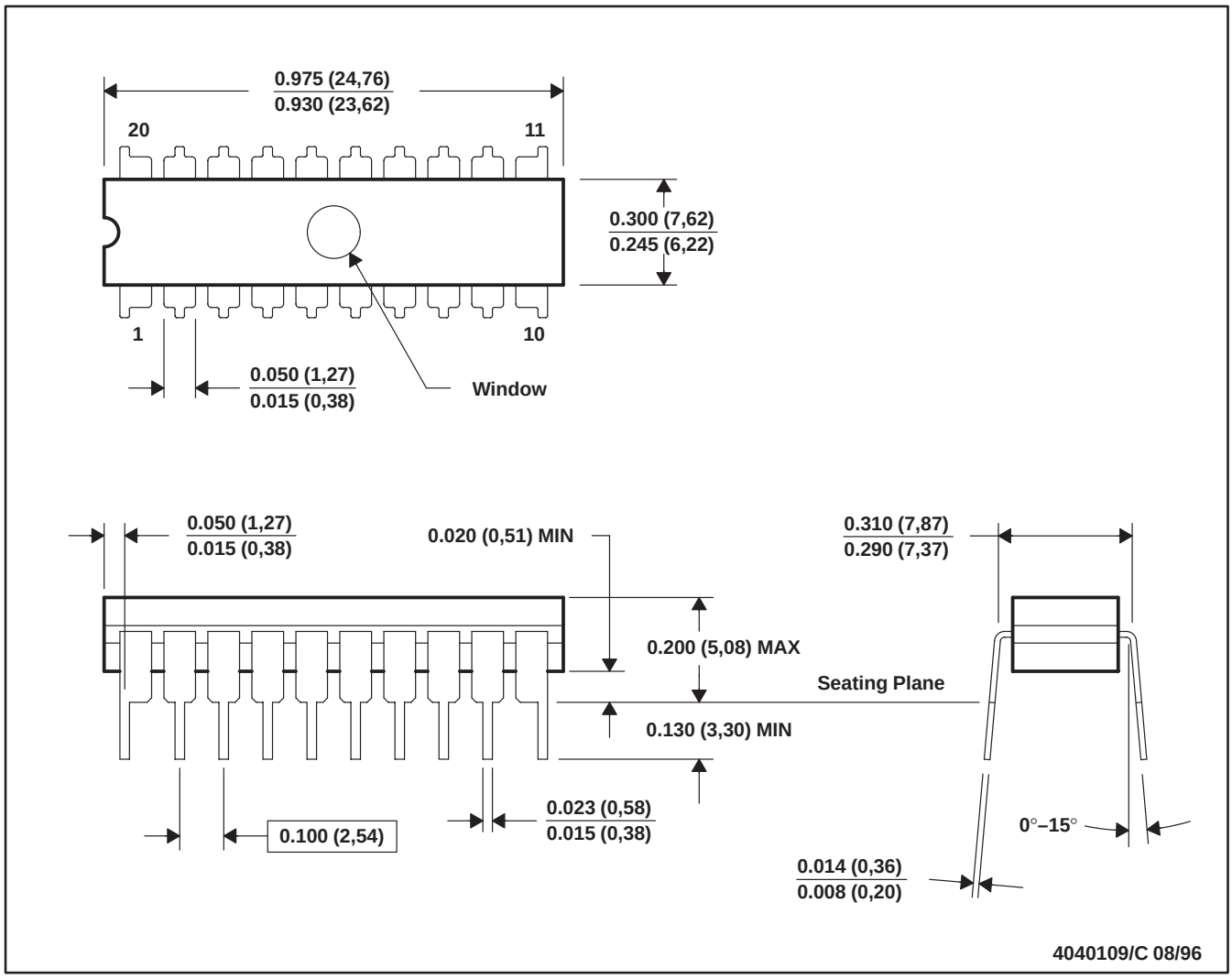
PMS430E112 pin out

JL PACKAGE
(TOP VIEW)



MECHANICAL DATA

JL (R-GDIP-T20) **CERAMIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
E. Falls within MIL-STD-1835 GDIP1-T20

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