TLC320AD535
Data Manual

Dual Channel Voice/Data Codec

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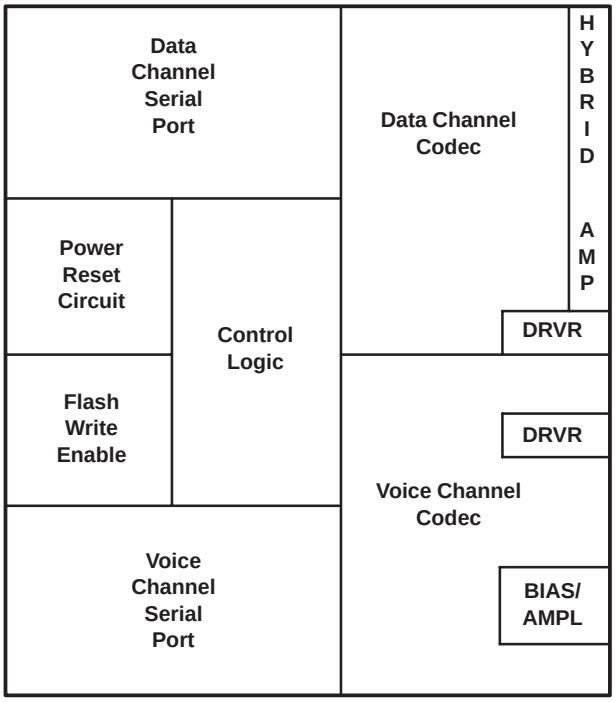
1 Introduction

The TLC320AD535 dual channel voice/data codec is a mixed-signal broadband connectivity device. The TLC320AD535 is comprised of a two channel codec and analog hybrid circuitry with two independent serial ports for communication with the host processor and external resistors and capacitors for setting gain and filter poles. The device also contains microphone bias and amplification, audio mixing capabilities in the voice channel, programmable gain control, and two speaker drivers. The device operates with a 5-V analog and a 5-V digital power supply as well as a 5-V monitor power supply. It is available in a single 64-pin PM (QFP) package.

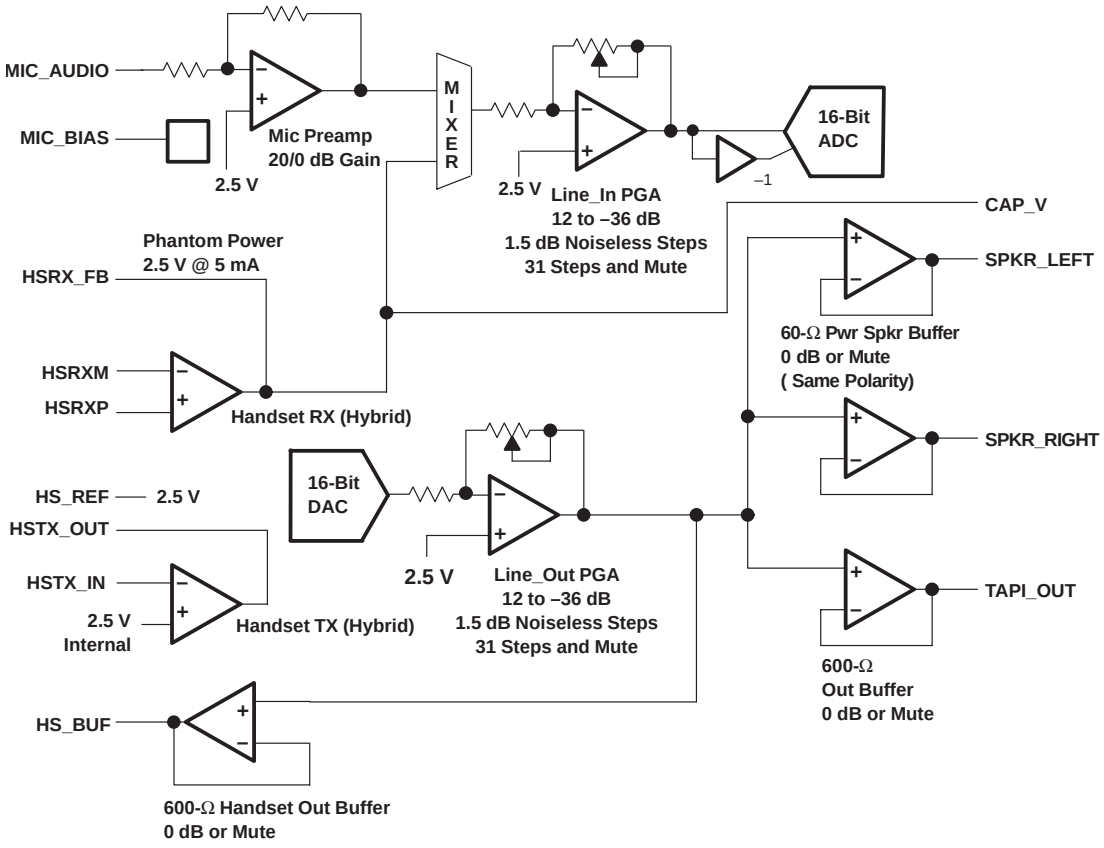
1.1 Features

- 5-V Analog, Digital, and Monitor Amp Power Supplies
- Separate Software Power-Down Modes for Data and Voice Channels
- Independent Voice and Data Channel Sample Rates Up to 11.025 kHz
- 16-Bit Signal Processing
- Dynamic Range of 83 dB in the Data and Voice Channels
- Total Signal-to-Noise + Distortion of 74 dB for the ADCs
- Total Signal-to-Noise + Distortion of 73 dB for the DACs
- Programmable Gain Amplifiers
- 600-Ω TAPI Audio and Data Channel Drivers
- 60-Ω Headphone Driver With Programmable Gain Amplifier
- 8-Ω AT41 Differential Speaker Driver With Programmable Gain Amplifier
- Maximum Microphone Bias of 5 mA at 2.5 V
- Maximum Handset Reference of 2.5 mA at 2.5 V
- Maximum Data Channel Reference of 10 mA at 2.5 V
- 5-V MV_{DD} Power Reset Circuit
- Flash Write Enable Circuit, for Writing the Flash Memory Device
- Available in a 64-Pin PM (QFP) Package Operating From 0°C to 70°C

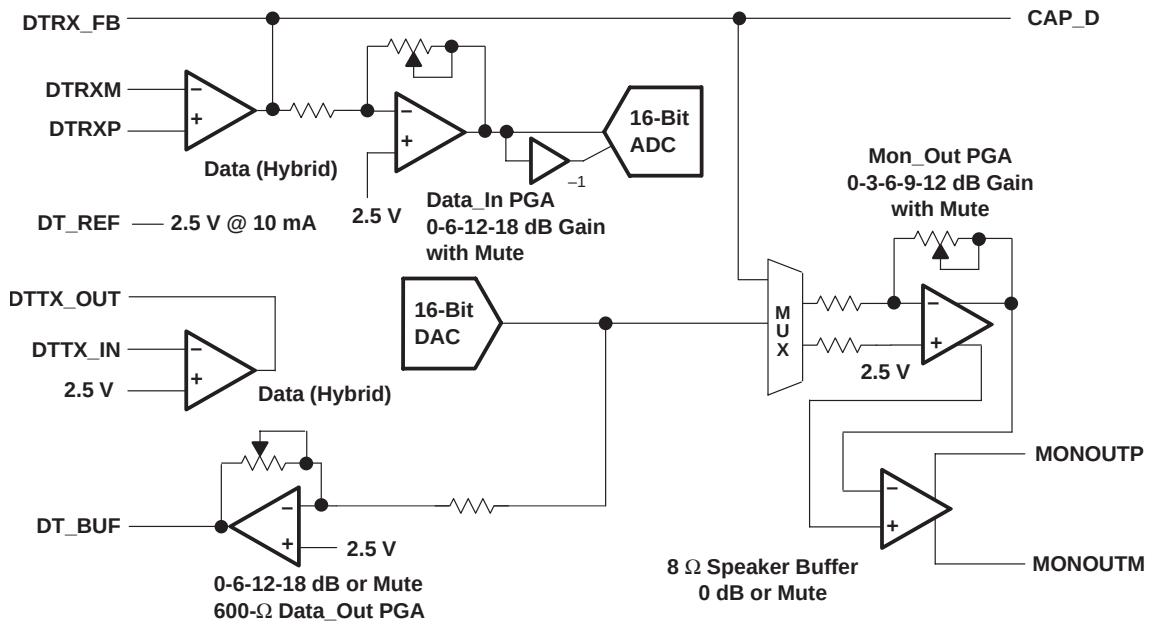
1.2 Functional Block Diagram



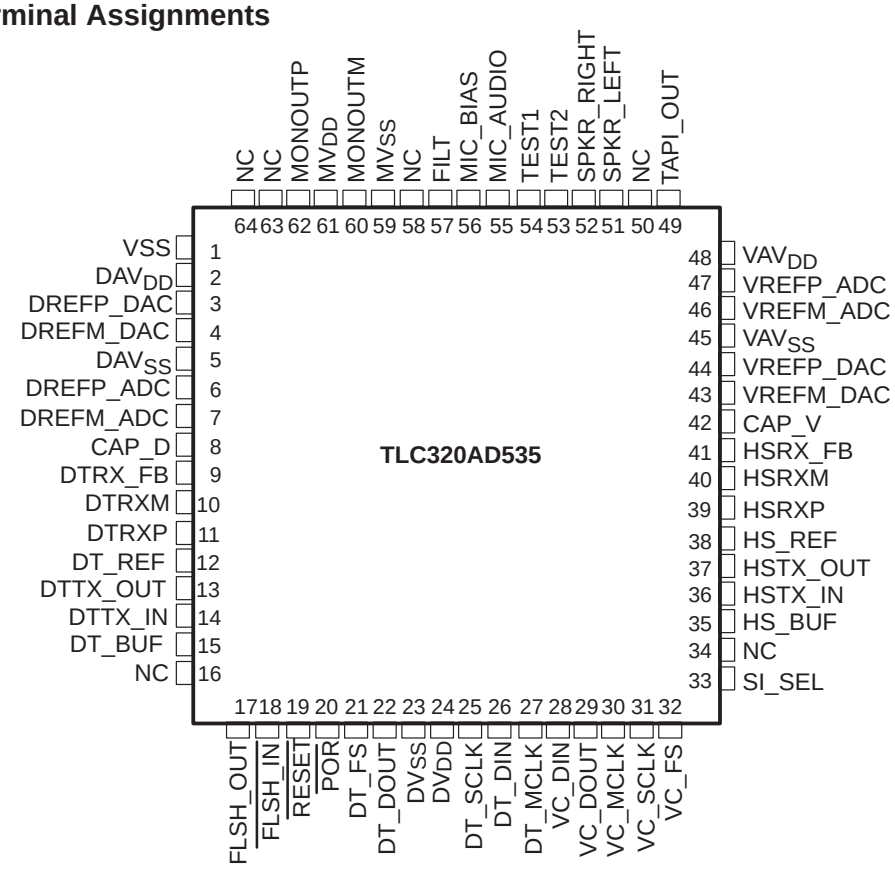
1.3 Voice Channel Codec Logic Diagram



1.4 Data Channel Codec Logic Diagram



1.5 Terminal Assignments



NC–Make no external connection

1.6 Ordering Information

T_A	PACKAGE
	PLASTIC QUAD FLATPACK (PM)
0°C to 70°C	TLC320AD535

1.7 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CAP_D	8	I	External terminal. To eliminate dc offset, a capacitor can be placed between CAP_D and DTRX_FB ac-coupling the input to the data channel ADC.
CAP_V	42	I	External terminal. To eliminate dc offset, a 0.1-μF capacitor can be placed between CAP_V and HSRX_FB for ac-coupling the input to the voice channel ADC.
DAV_{DD}	2	I	Data channel analog power supply (5 V)
DAV_{SS}	5	I	Data channel analog ground
DREFM_ADC	7	O	Data channel ADC voltage reference filter output. DREFM_ADC provides low-pass filtering for the internal bandgap reference. The optimal ceramic capacitor value is 0.1 μF, which is connected between DREFM_ADC and DREFP_ADC. The nominal DC voltage at this terminal is 0 V.
DREFM_DAC	4	O	Data channel DAC voltage reference filter output. DREFM_DAC provides low-pass filtering for the internal bandgap reference. The optimal ceramic capacitor value is 0.1 μF, which is connected between DREFM_DAC and DREFP_DAC. The nominal dc voltage at this terminal is 0 V.
DREFP_ADC	6	O	Data channel ADC voltage reference filter output. DREFP_ADC provides low-pass filtering for the internal bandgap reference. The optimal ceramic capacitor value is 0.1 μF, which is connected between DREFM_ADC and DREFP_ADC. The dc voltage at this terminal is 3.375 V.
DREFP_DAC	3	O	Data channel DAC voltage reference filter output. DREFP_DAC provides low-pass filtering for the internal bandgap reference. The optimal ceramic capacitor value is 0.1 μF, which is connected between DREFM_DAC and DREFP_DAC. The dc voltage at this terminal is 3.375 V.
DT_BUF	15	O	Data channel buffer amp analog output. DT_BUF is programmed for 0-dB gain or is muted using the control registers. This output is normally fed to the DTTX_IN terminal through an input resistor.
DT_DIN	26	I	Data channel digital data input. DT_DIN handles DAC input data as well as control register programming information during the data channel frame sync interval and is synchronized to DT_SCLK.
DT_DOUT	22	O	Data channel digital data output. Data channel ADC output bits are transmitted during the data channel frame sync period that is synchronized to DT_SCLK. DT_DOUT is at high impedance when DT_FS is not activated.
DT_FS	21	O	Data channel serial port frame sync signal. DT_FS signals the beginning of transmit for ADC data and receiving of DAC data in the data channel. This signal can be active high (FS high mode) or active low (FS low mode) depending on the voltage applied to SI_SEL (See Section 4, *Serial Communications* for more details).
DT_MCLK	27	I	Data channel master clock input. All of the internal clocks for the data channel are derived from this clock.
DT_REF	12	O	Handset amplifier reference voltage. The voltage at this pin is set at 2.5 V. The maximum source current at this terminal is 2.5 mA.
DTRX_FB	9	O	Data channel receive path amplifier feedback node. DTRX_FB connects to the output of the data channel receive path amplifier and allows a parallel resistor/capacitor to be placed in the amplifier feedback path for setting gain and filter poles.
DTRXM	10	I	Data channel receive path amplifier analog inverting input
DTRXP	11	I	Data channel receive path amplifier analog noninverting input.

1.7 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DT_SCLK	25	O	Data channel shift clock signal. This signal clocks serial data into DT_DIN and out of DT_DOUT during the data channel frame-sync interval.
DTTX_IN	14	I	Data channel transmit amplifier analog inverting input. This node is normally fed by the DT_BUF output through an input resistor. The noninverting input of the amplifier is connected internally to 2.5 V.
DTTX_OUT	13	O	Data channel transmit amplifier analog output
DV_{DD}	24	I	Digital power supply (5 V)
DV_{SS}	23	I	Digital ground
FILT	57	O	Bandgap filter node. FILT provides decoupling of the 3.375-V bandgap reference. The optimal capacitor value is 0.1 μF (ceramic). This node should not be used as a voltage source.
$\overline{\text{FLSH\_IN}}$	18	I	External ASIC logic input. When brought low $\overline{\text{FLSH\_IN}}$ enables the FLSH_OUT output.
FLSH_OUT	17	O	Power output to write/erase flash EEPROM device (such as Intel 28F400B or AMD Am29F400). Outputs 5 V (± 10%) at 45 mA maximum when FLSH_IN is brought low. FLSH_OUT does not go to a logic high state when off. There is an internal NMOS pull down to maintain the specified voltage. An external pull down is not required.
HS_BUF	35	O	Handset buffer amplifier analog output. HS_BUF can be programmed for 0-dB gain or muted using the control registers. This output is normally fed to the HSTX_IN terminal through an input resistor.
HS_REF	38	O	Handset amplifier reference voltage HS_REF is set at 2.5 V. The maximum source current at this terminal is 2.5 mA.
HSRX_FB	41	O	Feedback node for handset receive path amplifier. HSRX_FB is connected to the output of the handset receive path amplifier and allows a parallel resistor/capacitor to be placed in the amplifier feedback path for setting gain and filter poles.
HSRXM	40	I	Handset receive path amplifier analog inverting input
HSRXP	39	I	Handset receive path amplifier analog noninverting input
HSTX_IN	36	I	Handset transmit amplifier analog inverting input. This node is normally fed by the HSBUF output through an input resistor. The noninverting input of the amplifier is connected internally to 2.5 V.
HSTX_OUT	37	O	Handset transmit amplifier analog output
MIC_AUDIO	55	I	Microphone preamplifier analog input. MIC_AUDIO can be programmed to add either 0-dB or 20-dB gain using the control registers.
MIC_BIAS	56	O	Output that provides 2.5 V bias for electret microphone. The maximum source current at this terminal is 5 mA.
MONOUTM	60	O	8 Ω monitor speaker amplifier analog output. MONOUTM is set for 0-dB gain or is muted using the control registers.
MONOUTP	62	O	8 Ω monitor speaker amplifier analog output. MONOUTP is set for 0-dB gain or is muted using the control registers.
MV_{DD}	61	I	Monitor amplifier supply (5 V)
MV_{SS}	59	I	Monitor amplifier ground
$\overline{\text{POR}}$	20	O	Power on reset signal. $\overline{\text{POR}}$ remains low while the 5-V supply at MV_{DD} is below its threshold voltage and for 40 ms after it rises above the reset threshold.

1.7 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{RESET}}$	19	I	Codec device reset. $\overline{\text{RESET}}$ initializes all device internal registers to their default values. This signal is an active low.
SI_SEL	33	I	Serial interface mode select. When SI_SEL is tied to DV_{DD}, the serial port is in FS high mode. When SI_SEL is tied to DV_{SS}, the serial port is in FS low mode (See Section 4, *Serial Communications* for more details).
SPKR_LEFT	51	O	Analog output from 60-Ω speaker line amplifier. SPKR_LEFT is set for 0-dB gain or is muted using the control registers.
SPKR_RIGHT	52	O	Analog output from 60-Ω speaker line amplifier. SPKR_RIGHT is set for 0-dB gain or is muted using the control registers.
TAPI_OUT	49	O	TAPI buffer amplifier analog output. This 600-Ω amplifier is set for 0-dB gain or is muted using the control registers.
TEST1	54	I/O	Test input/output port. TEST1 is for factory testing only and should be left unconnected.
TEST2	53	I/O	Test input/output port. TEST2 is for factory testing only and should be left unconnected.
VAV_{DD}	48	I	Voice channel analog power supply (5 V)
VAV_{SS}	45	I	Voice channel analog ground
VC_DIN	28	I	Voice channel digital data input. VC_DIN handles DAC input data as well as control register programming information during the voice channel frame sync interval. VC_DIN is synchronized to VC_SCLK.
VC_DOUT	29	O	Voice channel digital data output. Voice channel ADC output bits are transmitted during the voice channel frame sync period synchronized to VC_SCLK. VC_DOUT is at high impedance when VC_FS is not activated.
VC_FS	32	O	Voice channel serial port frame sync signal. VC_FS signals the beginning of transmit for ADC data and receive of DAC data in the voice channel. This signal can be active high (FS nigh mode) or active low (FS low mode) depending on the voltage applied to SI_SEL (See Section 4, *Serial Communication* for more details).
VC_MCLK	30	I	Voice channel master clock input. All internal clocks for the voice channel are derived from this clock.
VC_SCLK	31	O	Voice channel shift clock signal. VC_SCLK clocks serial data into VC_DIN and out of VC_DOUT during the voice channel frame-sync interval.
VREFM_ADC	46	O	Voice channel ADC voltage reference filter output. VREFM_ADC provides low-pass filtering of the internal bandgap reference. The optimal ceramic capacitor value is 0.1 μF, which is connected between VREFM_ADC and VREFP_ADC. The nominal dc voltage at this terminal is 0 V.
VREFM_DAC	43	O	Voice channel DAC voltage reference filter output. VREFM_DAC provides low-pass filtering of the internal bandgap reference. The optimal ceramic capacitor value is 0.1 μF, which is connected between VREFM_DAC and VREFP_DAC. The nominal dc voltage at this terminal is 0 V.
VREFP_ADC	47	O	Voice channel ADC voltage reference filter output. VREFP_ADC provides low-pass filtering the internal bandgap reference. The optimal ceramic capacitor value is 0.1 μF, which is connected between VREFM_ADC and VREFP_ADC. The dc voltage at this terminal is 3.375 V.

1.7 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
VREFP_DAC	44	O	Voice channel DAC voltage reference filter output. VREFP_DAC provides low-pass filtering of the internal bandgap reference. The optimal ceramic capacitor value is 0.1 μF, which is connected between VREFM_DAC and VREFP_DAC. The dc voltage at this terminal is 3.375 V.
V_{SS}	1	I	Internal substrate connection. V_{SS} should be tied to either DAV_{SS} or VAV_{SS} for normal operation.

NOTE: All terminals marked NC should be left unconnected.

2 Functional Description

2.1 Device Requirements and System Overview

The TLC320AD535 device consists of two codec channels, a hybrid circuit with external resistors and capacitors for setting gain and filter poles, two independent serial ports, and other miscellaneous logic functions.

2.2 Codec Functions

The codec portion of the TLC320AD535 device performs the functions required for two channels of analog-to-digital conversion, digital-to-analog conversion, lowpass filtering, control of analog input and output gains, internal oversampling coupled with internal decimation and interpolation, and two 16-bit serial port interfaces to the host processor. The two serial ports operate independently and are capable of operating at different sample rates. The maximum sample rate of either codec channel is 11.025 kHz.

2.3 Hybrid Functions

The hybrid circuitry in the data channel includes integrated amplifiers whose gains and filter pole frequencies are set by external resistors and capacitors. This allows maximum flexibility to make adjustments for board variations and international standards while providing integration of the function. The filter amplifier stages in the data channel are followed by a programmable gain amplifier, which feeds 8-Ω differential speaker drivers for the AT41 call progress monitor speakers. The monitor speaker driver can be programmed for 0-dB gain or muted through the control 2 register. The source for the monitor speaker input can be either the output of the amplified DAC output (Data_Out PGA) or the ADC input signal through control register 1 (See *Appendix A*).

A 2.5-V reference voltage (DT_REF) is provided as a reference for the transformer. It is necessary to reference to 2.5 V (rather than ground), since the amplifiers are powered off by single-rail supplies.

2.4 Voice Channel Analog

The analog circuitry in the voice channel includes a microphone bias, which sources a maximum of 5 mA at 2.5 V, and preamplifiers for the microphone, which can be selected for 0-dB or 20-dB gain. The device also has a handset interface with receive and transmit amplifiers. These three inputs can be summed in any combination and the result sent to a Line_In programmable gain amplifier (PGA) stage with gain range from 12 dB to –36 dB in 1.5 dB noiseless steps. This feeds the voice channel ADC. In the DAC path, the output of the DAC is sent to a Line-Out PGA with gain range from 12 dB to –36 dB in 1.5 dB noiseless steps. This feeds both a 600-Ω TAPI output driver and a 60-Ω mono speaker driver that can be muted or programmed for 0-dB gain. The time-out for noiseless gain change or the maximum time the system can wait for a zero crossing of a signal before it will effect the gain change request is approximately 9 ms.

2.5 Miscellaneous Logic and Other Circuitry

The logic functions include the circuitry required to implement two independent serial ports and control register programming through secondary communication on those serial ports. There are five control registers that are programmed during secondary communications from either the data channel serial port or the voice channel serial port. These control registers set amplifier gains, choose multiplexer inputs, select loopback functions, and read the ADC overflow flags. The device also includes a power-on reset (POR) circuit to monitor the 5-V MV_{DD} power supply in the system and provides a reset signal when the supply MV_{DD} voltage drops below its threshold voltage. In addition, there is a flash write enable (FWE) circuit that takes an external logic input and provides 40 mA of current to power the write enable circuit of an external memory device. The flash write enable circuit is powered from the digital power supply.

3 Codec Functional Description

3.1 Operating Frequencies

The TLC320AD535 is capable of supporting any sample rate up to the maximum sample rate of 11.025 kHz in either the data channel or voice channel. The sample rate is set by the frequency of the codec master clock that is input to the serial port for that channel.

The sampling (conversion) frequency is derived from the internally generated codec master clock divider circuit by the following equation:

$$f_S = \text{Sampling (conversion) frequency} = (\text{MCLKx}/512) \quad (1)$$

Where xMCLK refers to either the voice channel or data channel codec clock (VC_MCLK or DT_MCLK) fed to the codec externally by the clock rate divider circuit. The clock rate divider circuit divides the system master clock to obtain the necessary clock frequency to feed the codecs.

The inverse of the sampling frequency is the conversion period. The sample rates of the voice and data channels can be set independently by their respective codec master clocks. The two codec channels can be sampled at different rates simultaneously.

3.2 ADC Signal Channel

The input signals are amplified and filtered by on-chip buffers before being applied to their respective ADC input. In the case of the voice channel, inputs from a microphone input and the handset input may be summed together before being amplified/attenuated by the ADC line PGA. The ADC converts the signal into discrete output digital words in 2s-complement format, corresponding to the analog signal value at the sampling time. These 16-bit digital words, representing sampled values of the analog input signal, are sent to the host through the serial port interface for their respective channels. If the ADC reaches its maximum value, a control register flag is set. This overflow bit resides at D0 in the data channel control register 2 or the voice channel control register 5. These bits can only be read from their respective serial ports, and the overflow flag is cleared only if it is read through the voice channel serial port, and similarly for the data channel. Two external pins (CAP_V and CAP_D) add a series capacitor before the ADC inputs to ac couple the inputs to the ADC, eliminating dc offset. The ADC and DAC conversions are synchronous and phase-locked.

3.3 DAC Signal Channel

The DAC receives the 16-bit data words (2s complement) from the host through the serial port interface for each channel. The data is converted to analog voltages by their respective sigma-delta DACs comprised of a digital interpolation filter and a digital modulator. The outputs of the DACs are each then passed to internal low pass filters to complete the signal reconstruction resulting in an analog signal. Those analog signals are then buffered and amplified by an output driver capable of driving the required load. The gain of these output amplifiers is programmed by the Codec Control Registers, as shown in *Appendix A*.

3.4 Sigma-Delta ADC

Each ADC is an oversampling sigma-delta modulator. The ADC provides high resolution and low noise performance using oversampling techniques and the noise shaping advantages of sigma-delta modulators.

3.5 Decimation Filter

Each decimation filter reduces the digital data rate to the sampling rate. This is accomplished by decimating with a ratio equal to the oversampling ratio. The output of this filter is a 16-bit 2s-complement data word clocking at the selected sample rate.

3.6 Sigma-Delta DAC

Each DAC is an oversampling sigma-delta modulator. The DAC performs high-resolution, low-noise digital-to-analog conversion using oversampling sigma-delta techniques.

3.7 Interpolation Filter

Each interpolation filter resamples the digital data at a rate of N times the incoming sample rate, where N is the oversampling ratio. The high-speed data output from this filter is then applied to the sigma-delta DAC.

3.8 Analog and Digital Loopbacks

The test capabilities include an analog loopback and digital loopback. The loopbacks provide a means of testing the ADC/DAC channels and are used for in-circuit system-level tests. The loopback feeds the ADC output to the DAC input on the IC for each individual channel. The analog loopback functions test only the codec portions of the device and do not include the hybrid amplifiers.

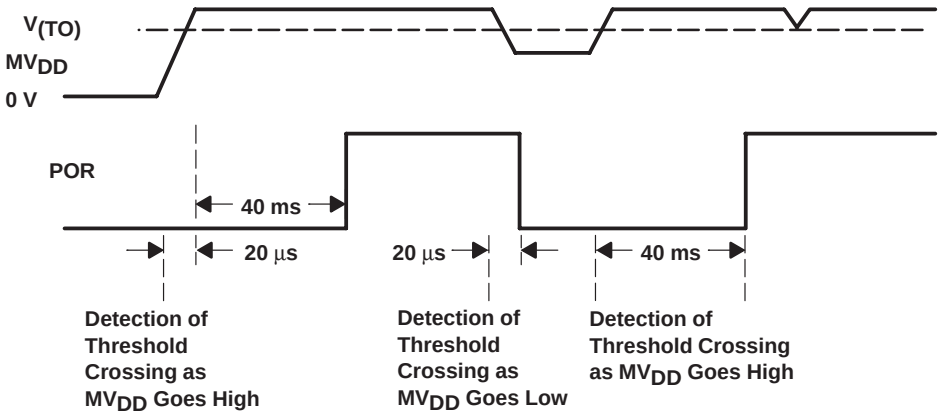
Analog loopback loops the DAC output back into the ADC input of the same channel. Digital loopback loops the ADC output back into the DAC input of the respective channel. Analog loopback is enabled by setting the D4 bit in the control register 1 for the data channel or control register 3 for the voice channel. Digital loopback is enabled by setting the D5 bit high in control register 1 for the data channel or control register 3 for the voice channel.

3.9 Software Power Down

The software power down resets all internal counters, but leaves the contents of the programmable control registers unchanged for the selected channel. The device has separate and independent software power down bits for the voice and data channels. The software power down feature is invoked by setting the D6 bit high in control register 1 for the data channel or setting the D6 bit in control register 3 for the voice channel. There is no hardware powerdown function in the TLC320AD535.

3.10 Reset Circuit

This circuit monitors the 5-V MV_{DD} power supply coming into the device from the bus and asserts an active low power-on-reset (POR) signal whenever this supply voltage drops below its threshold voltage. The reset signal remains low while the supply voltage is below the threshold voltage. It remains low for 40 ms (nominal) after the supply voltage has risen above the reset threshold voltage. Once the voltage rises above the threshold, an internal counter is activated and holds the POR signal low for an additional 40 ms (nominal). The signal then goes high and remains high as long as the MV_{DD} supply remains in the acceptable voltage range. This circuit is, in effect, on initial power-up of the device and POR is held low until the supply voltage rises above the threshold. In addition, a reset is triggered if a transient spike of sufficient magnitude and duration occurs. The supply must drop below the threshold voltage for a period of time greater than the delay time shown in the following table (delay time, MV_{DD} to reset). If a spike occurs that drops below the threshold, but the supply voltage returns above the threshold within the delay time, POR remains in the high state.



PARAMETER	MIN	NOM	MAX	UNIT
Delay time, MV_{DD} to reset	10	20	40	µs
Delay time reset pulse (POR)	20	40	80	ms
Threshold voltage $V_{(TO)}$	4.5	4.63	4.75	V

3.11 Test Module

The test module serves the purpose of facilitating design verification testing and simplifying factory production testing. There are two input/output terminals (TEST1 and TEST2) dedicated to implementing the test functions. The function of these terminals is for factory self-test only, and NO CONNECTION (NC) should be made to either of these terminals.

4 Serial Communications

DT_DOUT, DT_DIN, DT_SCLK, and DT_FS are the serial communication signals for the data channel serial port, while VC_DOUT, VC_DIN, VC_SCLK, and VC_FS are the serial communication signals for the voice channel serial port. The digital output data from the ADC is taken from DT_DOUT (or VC_DOUT). The digital input data for the DAC is applied to DT_DIN (or VC_DIN). The synchronization clock for the serial communication data and the frame-sync is taken from DT_SCLK and VC_SCLK for the data and voice channels, respectively. The frame-sync pulse which signals the beginning of the ADC and DAC data transfer interval is taken from DT_FS and VC_FS for the data and voice channels, respectively.

For signal data transmitted from the ADC or to the DAC, a primary serial communication is used. A secondary communication reads or writes words to the control registers, which control both the options and the circuit configurations of the device.

The purpose of primary and secondary communications is to allow conversion data and control data to be transferred across the same serial port. A primary transfer is always dedicated to conversion data. A secondary transfer is used to set up or read the control register values described in *Appendix A*, *Programmable Register Set*. A primary transfer occurs for every conversion period. A secondary transfer occurs only when requested. Secondary serial communication is requested by software - D0 of the primary data input to DT_DIN for the data channel serial port or to VC_DIN for the voice channel serial port. A secondary request can be made for the voice channel without making a secondary request for the data channel, or vice versa. Control registers 1 and 2 can only be written to or read from the data channel serial port. Control registers 3 through 6 can only be written to or read from the voice channel serial port.

4.1 Primary Serial Communication

Primary serial communication transmits and receives conversion signal data. After power up or reset, the device goes into the 15-bit DAC mode. The DAC word length is 15 bits and the last bit of the primary 16-bit serial communication word is a control bit used to request secondary serial communication. For all serial communications, the most significant bit is transferred first. For the 16-bit ADC word, D15 is the most significant bit, and D0 is the least significant bit. For the 15-bit DAC data word in a primary communication, D15 is the most significant bit, D1 is the least significant bit, and D0 is used for the secondary communication request control. All digital data values are in 2s-complement data format. Refer to Figure 4–1.

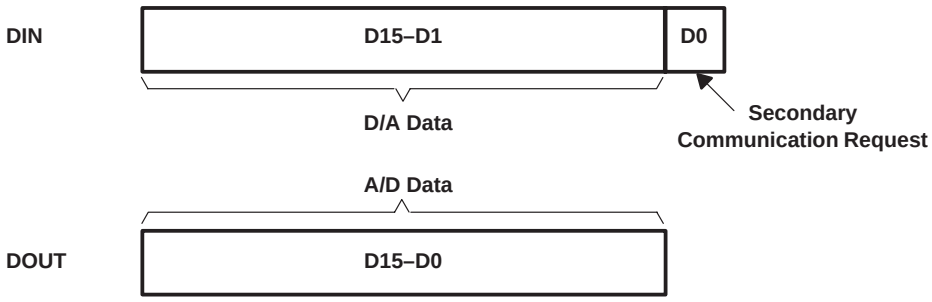


Figure 4–1. Primary Communication DIN and DOUT Data Format

4.1.1 FS High Mode Primary Communication Timing

There are two possible modes for serial data transfer. One mode is the FS high mode which is selected by tying the SI_SEL pin to DV_{DD}. Figure 4–2 shows the timing relationship for SCLK, FS, DOUT and DIN in a primary communication for either the voice or data channel when in FS high mode. The timing sequence for this operation is as follows:

1. FS is brought high and remains high for one SCLK period, then goes low.
2. A 16-bit word is transmitted from the ADC (DT_DOUT and VC_DOUT) and a 16-bit word is received for DAC conversion (DT_DIN and VC_DIN).

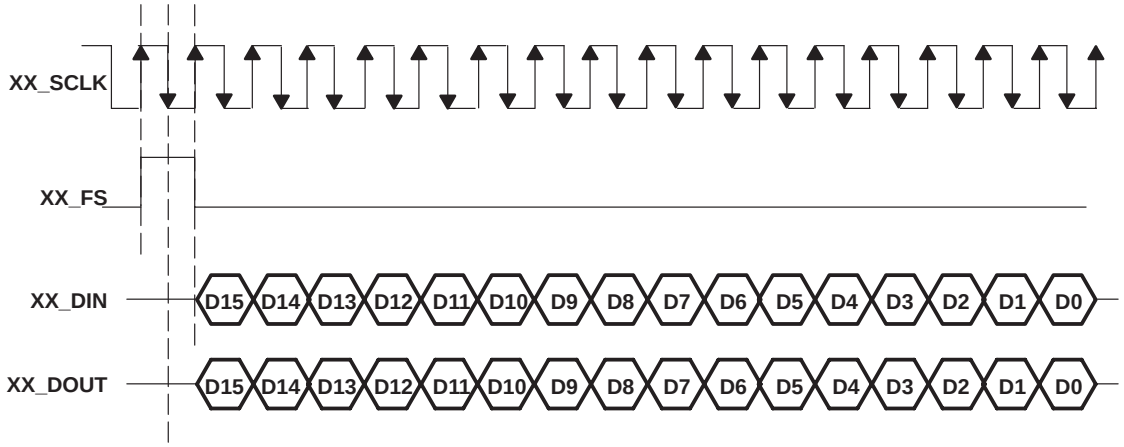


Figure 4–2. FS High Mode Primary Serial Communication Timing

4.1.2 FS Low Mode Primary Communication Timing

The second possible serial interface mode is the FS low mode, which is selected by tying the SI_SEL pin to DV_{SS}. This mode differs from the FS high mode in that the frame sync signal (FS) is active low, data transfer starts on the falling edge of FS, and FS remains low throughout the data transfer. Figure 4–3 shows the timing relationship for SCLK, FS, DOUT and DIN in a primary communication for either the voice or data channel when in FS low mode. The timing sequence for this operation is as follows:

1. FS is brought low by the TLC320AD535.
2. A 16-bit word is transmitted from the ADC (DT_DOUT and VC_DOUT) and a 16-bit word is received for DAC conversion (DT_DIN and VC_DIN).
3. FS is brought high signaling the end of the data transfer.

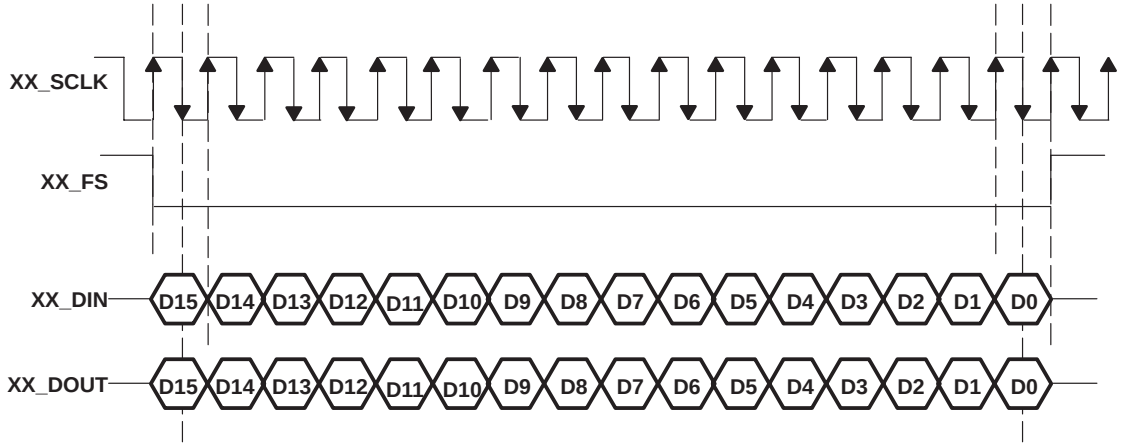


Figure 4–3. FS Low Mode Primary Serial Communication Timing

4.2 Secondary Serial Communication

Secondary serial communication reads or writes 16-bit words that program both the options and the circuit configurations of the device for either the voice channel or the data channel. Register programming always occurs during secondary communication for that channel. Control registers 1 and 2 can only be written to or read from the data channel serial port. Control registers 3 through 6 can only be written to or read from the voice channel serial port. Four primary and secondary communication cycles are required to program the four voice channel registers. In the same manner, two primary and secondary communication cycles are necessary to program the data channel control registers. If the default value for a particular register is desired, then the register addressing can be omitted during secondary communications. The NOOP (no operation) command addresses a pseudo-register, register 0, and no register programming takes place during this secondary communication. This can be used for either the data channel or the voice channel serial port.

During a secondary communication, a register is written to or read from. When writing a value to a register, the DT_DIN (or VC_DIN) line contains the value to be written. The data returned on DT_DOUT (or VC_DOUT) is 00h.

The method for requesting a secondary communication is by asserting the least significant bit (D0) of DT_DIN (or VC_DIN) high as shown in Table 4–1.

Table 4–1. Least-Significant-Bit Control Function

CONTROL BIT D0	CONTROL BIT FUNCTION
0	No secondary communication request
1	Secondary communication request

Figure 4–4 shows the data format XX_DIN and XX_DOUT during secondary communication.

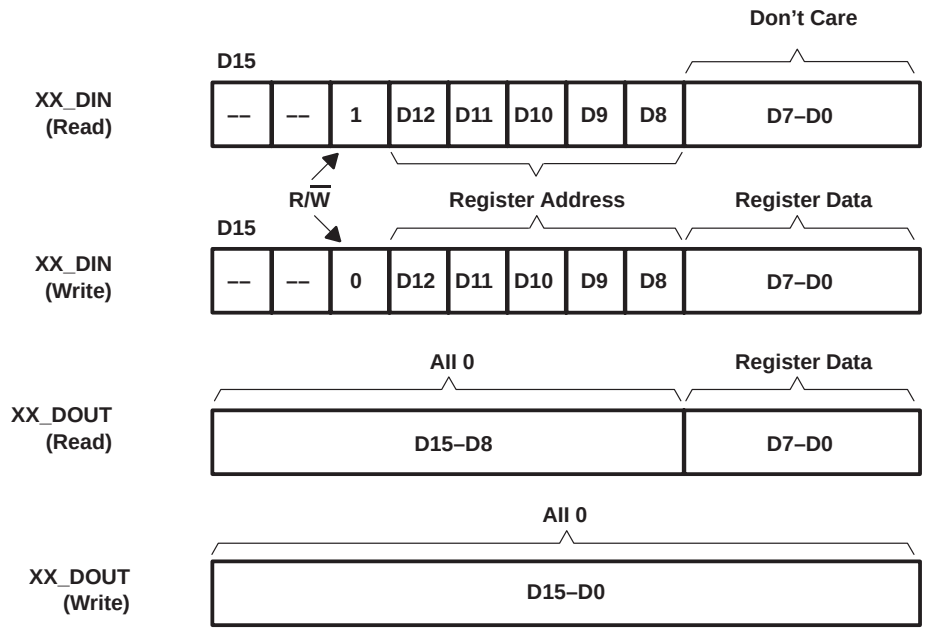


Figure 4–4. Secondary Communication DIN and DOUT Data Format

4.2.1 FS High Mode Secondary Communication Timing

On the rising edge of SCLK, coinciding with the falling edge of FS for that channel, D15–D0 is input serially to DT_DIN (or VC_DIN), and D15–D0 is output serially on DT_DOUT (or VC_DOUT). If a secondary communication request is made, FS goes high again 128 SCLKs after the beginning of the primary frame to signal the beginning of the secondary frame one SCLK period later. See Figure 4–5.

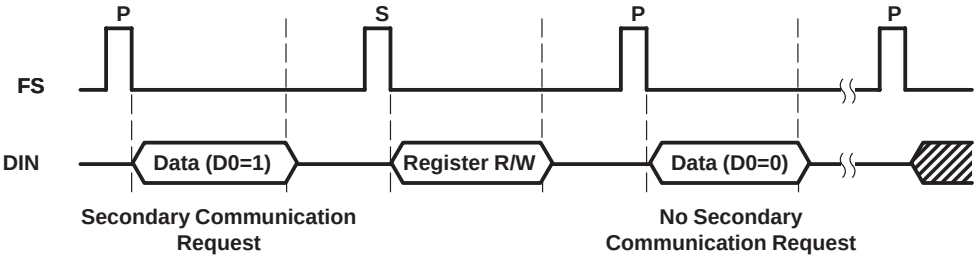


Figure 4–5. FS Output During Software Secondary Serial Communication Request (FS High Mode)

4.2.2 FS Low Mode Secondary Communication Timing

On the falling edge of FS for that channel, D15–D0 is input serially to DT_DIN (or VC_DIN) and D15–D0 is output serially on DT_DOUT (or VC_DOUT). FS remains low during the data transfer and then returns high. If a secondary communication request is made, FS goes low 128 SCLKs after the beginning of the primary frame to signal the beginning of the secondary frame. See Figure 4–6.

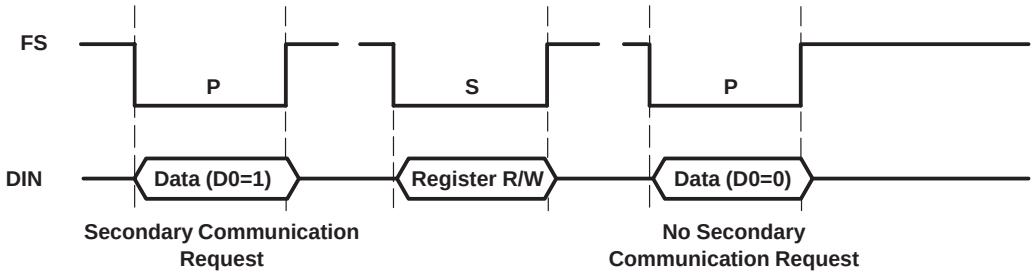


Figure 4–6. FS Output During Software Secondary Serial Communication Request (FS Low Mode)

5 Specifications

5.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, DV_{DD}, AV_{DD} (see Note 1) . . . . . –0.3 V to 7 V
Output voltage range, all digital output signals . . . . . –0.3 V to DV_{DD} + 0.3 V
Input voltage range, all digital input signals . . . . . –0.3 V to DV_{DD} + 0.3 V
Case temperature for 10 seconds: PM package . . . . . 260°C
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

5.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, DAV_{DD}, VAV_{DD}, MV_{DD}, DV_{DD} (see Note 2)	4.5	5	5.5	V
Analog signal peak-to-peak input voltage†, DT_RXM, DT_RXP, MIC_AUDIO, HS_RXM, HS_RXP, $V_{I(analog)}$			3	V
Differential output load resistance, TAPI_OUT, DT_BUF, HS_BUF, R_L	600			Ω
Differential output load resistance, MONOUTP, MONOUTM, R_L	8			Ω
Differential output load resistance, SPKR_RIGHT, SPKR_LEFT, R_L	60			Ω
Input impedance, MIC_AUDIO		50		kΩ
Master clock			5.645	MHz
Load capacitance, C_L			20	pF
ADC or DAC conversion rate		8	11.025	kHz
Operating free-air temperature, T_A	0		70	°C

† Preamplifier gain set to 0 dB

NOTE 2: Voltages at analog inputs and outputs and xV_{DD} are with respect to the xV_{SS} terminal.

5.3 Electrical Characteristics Over Operating Free-Air Temperature Range, DV_{DD} = 5 V, xAV_{DD} = 5 V, MV_{DD}=5 V

5.3.1 Digital Inputs and Outputs, f_S = 8 kHz, Outputs Not Loaded

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, any digital output	I_O = –360 µA	2.4	4.6		V
V_{OL}	Low-level output voltage, any digital output	I_O = 2 mA		0.2	0.4	V
I_{IH}	High-level input current, any digital input	V_{IH} = 5 V			10	µA
I_{IL}	Low-level input current, any digital input	V_{IL} = 0.6 V			10	µA
C_i	Input capacitance, any digital input			10		pF
C_o	Output capacitance, any digital output			10		pF
$I_{I(lkg)}$	Input leakage current, any digital input				30	µA
I_{OZ}	Output leakage current, any digital output				30	µA

5.3.2 ADC Path Filter, f_S = 8 kHz (see Note 3)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	0 to 300 Hz	–0.5		0.2	dB
	300 Hz to 3 kHz	–0.5		0.25	
	3.3 kHz	–0.5		0.3	
	3.6 kHz			–3	
	4 kHz			–35	
	≥ 4.4 kHz			–74	

NOTE 3: The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The analog input test signal is a sine wave with 0 dB = 3 $V_{I(PP)}$ as the reference level for the ADC analog input signal. The –3-dB passband is 0 to 3600 Hz for an 8-kHz sample rate. This pass-band scales linearly with the sample rate.

5.3.3 ADC Dynamic Performance, f_S = 8 kHz

5.3.3.1 ADC Signal-to-Noise (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio (SNR)	V_I = –1 dB	76	81		dB
	V_I = –9 dB	68	73		
	V_I = –40 dB	37	42		

NOTE 4: The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output are referred to 2.5 V.

5.3.3.2 ADC Signal-to-Distortion (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion (THD)	V_I = –3 dB	71	76		dB
	V_I = –9 dB	74	79		
	V_I = –40 dB	58	63		

NOTE 4: The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output are referred to 2.5 V.

5.3.3.3 ADC Signal-to-Distortion + Noise (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion + noise (THD + N)	V_I = –3dB	69	74		dB
	V_I = –9 dB	65	70		
	V_I = –40 dB	38	43		

NOTE 4: The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output are referred to 2.5 V.

5.3.4 ADC Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(PP)}$	Peak-input voltage, TAPI_IN, MIC_AUDIO	Preamp gain = 0 dB			3	V
	Dynamic range			79		dB
	Intrachannel isolation			80		dB
E_G	Gain error	V_I = –1 dB at 1020 kHz		±0.6		dB
$E_{O(ADC)}$	ADC channel offset error including hybrid amplifiers	With a 0.1-μF capacitor between CAP_D and DTRX_FB		5		mV
$E_{O(ADC)}$	ADC channel offset error including hybrid amplifiers	With no capacitor between CAP_D and DTRX_FB		15		mV
	Idle channel noise (on-chip reference)			26	75	μV rms
	Channel delay			$17/f_S$		s

5.3.5 DAC Path Filter, f_S = 8 kHz (see Note 5)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	0 to 300 Hz	–0.5		0.3	dB
	300 Hz to 3 kHz	–0.25		0.25	
	3.3 kHz	–0.35		0.3	
	3.6 kHz			–3	
	4 kHz			–35	
	≥ 4.4 kHz			–74	

NOTE 5: The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dB). The –3 dB passband is 0 to 3600 Hz for an 8-kHz sample rate. This pass band scales linearly with the sample rate.

5.3.6 DAC Dynamic Performance, DV_{DD} = 5 V

5.3.6.1 DAC Signal-to-Noise (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio (SNR)	V_I = 0 dB	71	76		dB
	V_I = –9 dB	62	67		
	V_I = –40 dB	31	36		

NOTE 4: The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output are referred to 2.5 V.

5.3.6.2 DAC Signal-to-Distortion (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion (THD)	V_I = –3 dB	77	82		dB
	V_I = –9 dB	70	75		
	V_I = –40 dB	65	70		

NOTE 4: The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output are referred to 2.5 V.

5.3.6.3 DAC Signal-to-Distortion + Noise (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion + noise (THD + N)	V_I = –3 dB	68	73		dB
	V_I = –9 dB	62	67		
	V_I = –40 dB	30	35		

NOTE 4: The test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output are referred to 2.5 V.

5.3.7 DAC Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Dynamic range			79		dB
	Intrachannel isolation			80		dB
E_G	Gain error	V_I = –1 dB at 1020 kHz		±0.6		dB
	Idle channel narrow-band noise	0 kHz to 4 kHz (see Note 6)			125	μV rms
	Channel delay			$18/f_S$		s
V_{OO}	Output offset voltage, HS_BUF, DT_BUF	DIN = All zeros		15		mV
V_O	Analog output voltage, MONOUTP-MONOUTM	Differential with respect to $MV_{DD}/2$ and full-scale digital input (see Note 7)	–1.78		1.78	V
V_O	Analog output voltage, TAPI_OUT, SPKR_LEFT, SPKR_RIGHT	Single-ended with respect to HS_REF and full-scale digital input	–1.5		1.5	V

NOTES: 6. The conversion rate is 8 kHz.
7. This amplifier should only be used in differential mode.

5.3.8 Logic DC Electrical Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage	–0.3		1.5	V
V_{IH}	High-level input voltage	2.4		DV_{DD}+0.3	V
$I_{I(lkg)}$	Input leakage current			10	μA
$I_{O(lkg)}$	Output leakage current			10	μA
V_{OH}	High-level output voltage at rated load current	2.4		DV_{DD}–0.5	V
V_{OL}	Low-level output voltage at rated load current	AV_{SS}–0.5		0.4	V

5.3.9 Power Supply Rejection (see Note 8)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD1}	Supply-voltage rejection ratio, ADC channel DAV_{DD} and VAV_{DD}	f_i = 0 to $f_S/2$		50		dB
V_{DD2}	Supply-voltage rejection ratio, ADC channel, DV_{DD}	f_i = 0 to $f_S/2$		40		
V_{DD3}	Supply-voltage rejection ratio, DAC channel, DAV_{DD} and VAV_{DD}	f_i = 0 to $f_S/2$		50		
V_{DD4}	Supply-voltage rejection ratio, DAC channel, DV_{DD}	f_i = 0 to 30 kHz		50		

NOTE 8: Power supply rejection measurements are made with both the ADC and the DAC channels idle and a 200 mV peak-to-peak signal applied to the appropriate supply.

5.3.10 Power Supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DD(analog)}$	Codec power supply current, analog (including hybrid and drivers)	Operating		40	60	mA
$I_{DD(digital)}$	Codec power supply current, digital	Operating		10		mA
$I_{DD(monitor)}$	Power supply current, 8 Ω monitor speaker driver	Operating		135	315	mA

5.3.11 Reset Circuit

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TO)}$	Reset threshold voltage	T_A= 25°C		4.63		V
		T_A= 0°C to 70°C	4.50		4.75	V
V_{OL}	POR output low-level voltage	$I_{(SINK)}$ = 1.2 mA			0.3	V
V_{OL}	POR output low-level voltage	$I_{(SINK)}$ = 3.2 mA			0.4	V
V_{OH}	POR output high-level voltage	I = –500 µA	0.8 DV_{DD}			V
$t_{d(RPD)}$	POR low delay time after threshold exceeded		20	40	80	ms
$t_{d(RDD)}$	Delay time after threshold crossed before POR activates		10	20	40	µs

5.3.12 Flash Write Enable Circuit

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(FLSH\_OUT)}$	Output high-level voltage, FLSH_OUT	FLSH_IN low	4.5	5	5.5	V
$V_{OL(FLSH\_OUT)}$	Output low-level voltage, FLSH_OUT	FLSH_IN high	0		1.5	V
$I_{O(FLSH\_OUT)}$	Output current, FLSH_OUT	FLSH_IN low		40	45	mA

5.3.13 8-Ω Drive

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output gain when PGA gain is mute	–12 dB (input)		–96		dB
Output gain when PGA gain is 0 dB		–1.5	0.7	1.5	
Output gain when PGA gain is 12 dB		10.5	12.5	13.5	

5.4 Timing Characteristics (see Parameter Measurement Information)

5.4.1 Timing Requirements

PARAMETER		MIN	TYP	MAX	UNIT
t_{d1}	Delay time, SCLK↑ to FS↓			0	ns
t_{su1}	Setup time, DIN, before SCLK low	25			ns
t_{h1}	Hold time, DIN, after SCLK high			20	ns
t_{d3}	Delay time, MCLK↓ to SCLK↑			50	ns
t_{wH}	Pulse duration, MCLK high	32			ns
t_{wL}	Pulse duration, MCLK low	20			ns

5.4.2 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d2}	Delay time, SLCK↑ to DOUT	C_L = 20 pF			20	ns
t_{en1}	Enable time, $\overline{FS}$↓ to DOUT				25	
t_{dis1}	Disable time, $\overline{FS}$↑ to DOUT Hi-Z			20		

5.5 Parameter Measurement Information

NOTE A: Timing shown is for the TLC320AD535 operating as the master device. The programmed data value in the FSD register is 0.

Figure 5–1. SCLK Timing

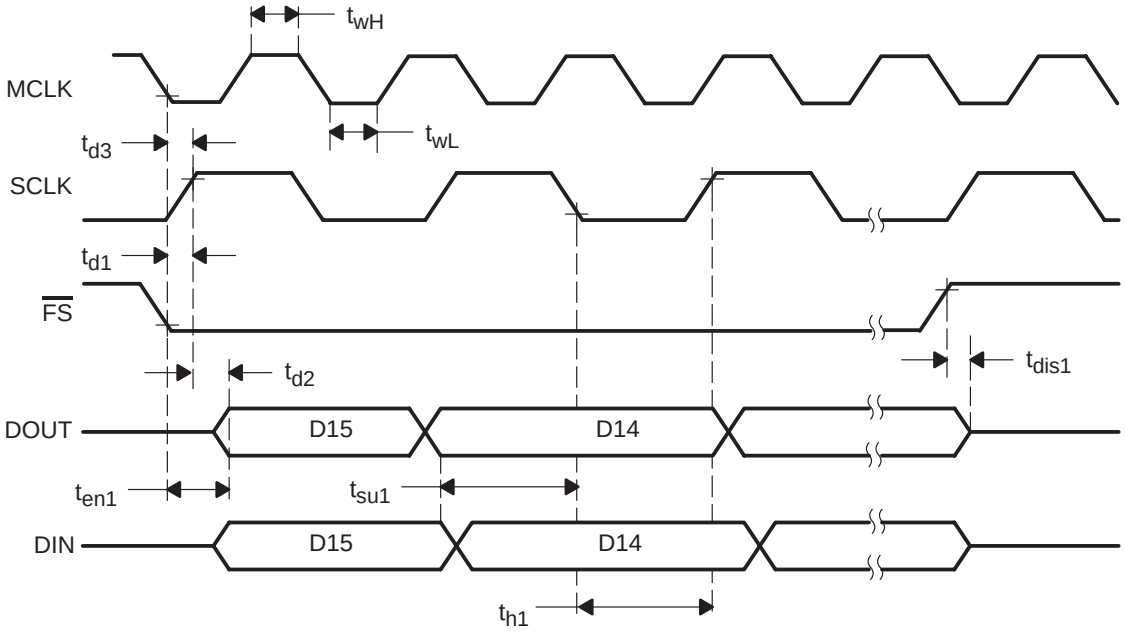


Figure 5–2. Serial Communication Timing

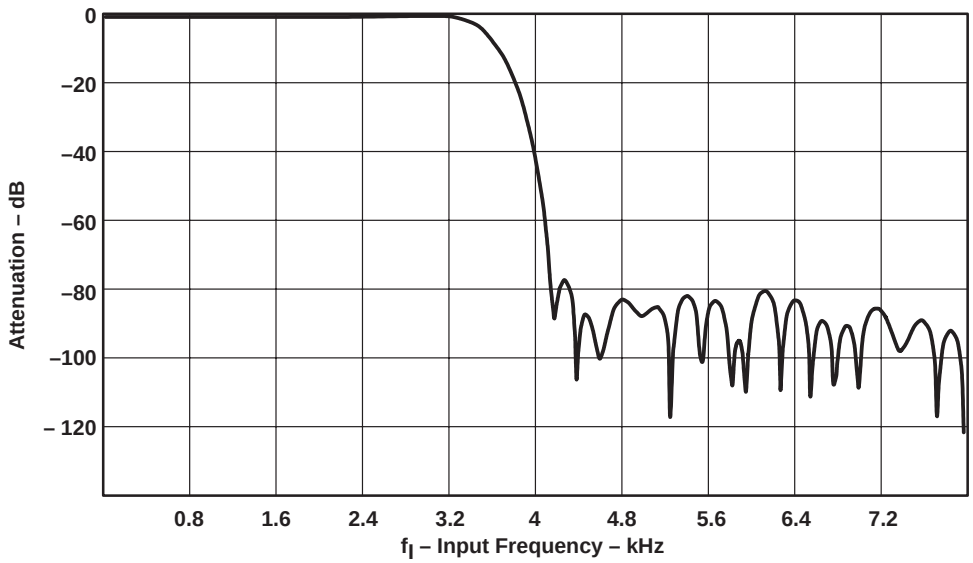


Figure 5–3. ADC Decimation Filter Response

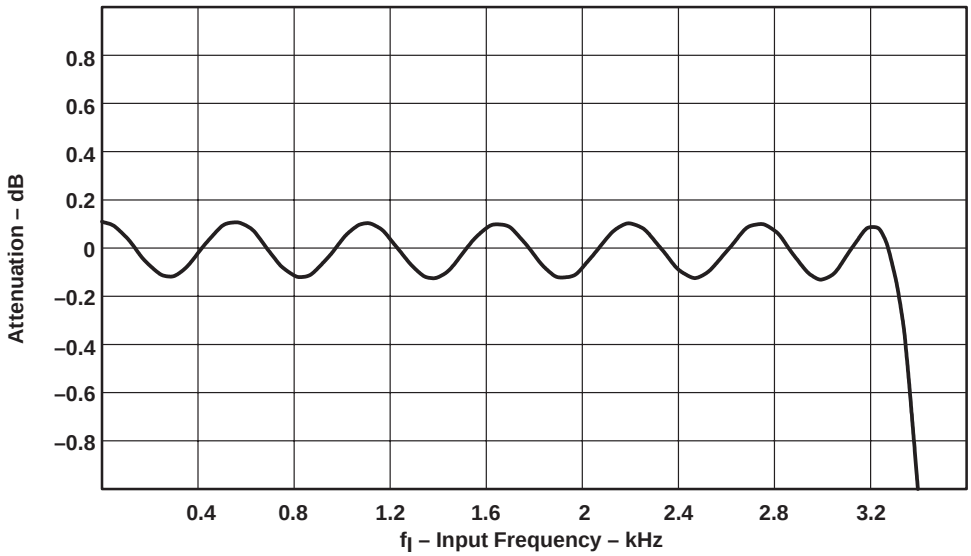


Figure 5–4. ADC Decimation Filter Passband Ripple

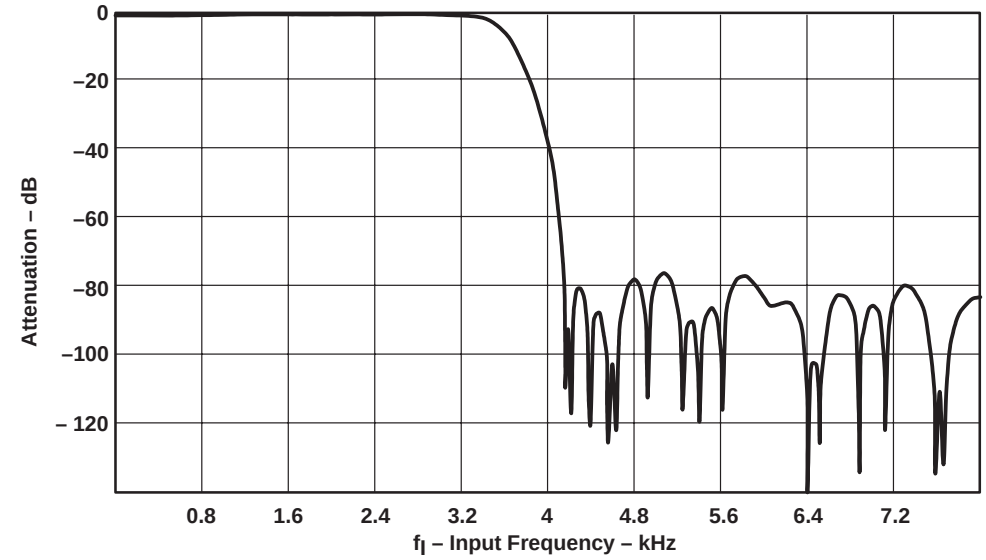


Figure 5–5. DAC Interpolation Filter Response

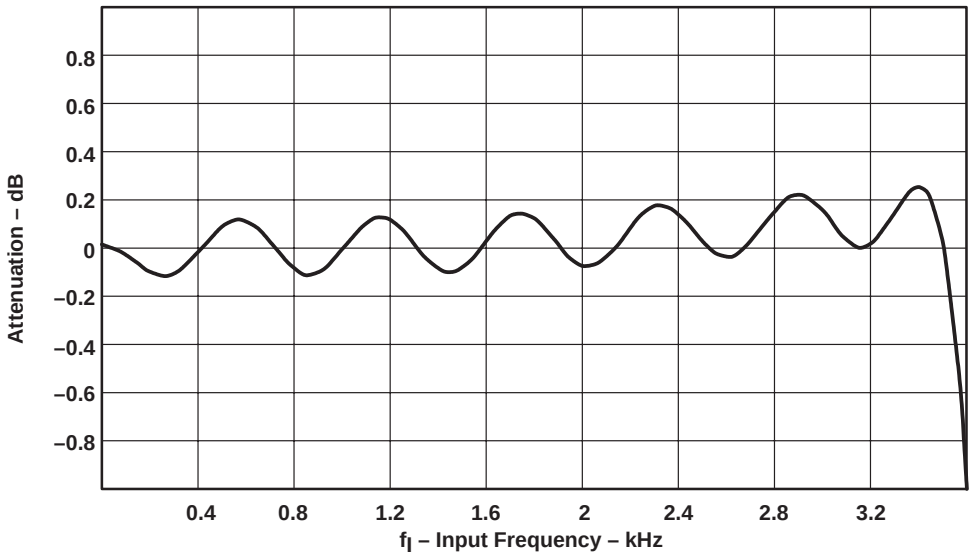


Figure 5–6. DAC Interpolation Filter Passband Ripple

6 Application Information

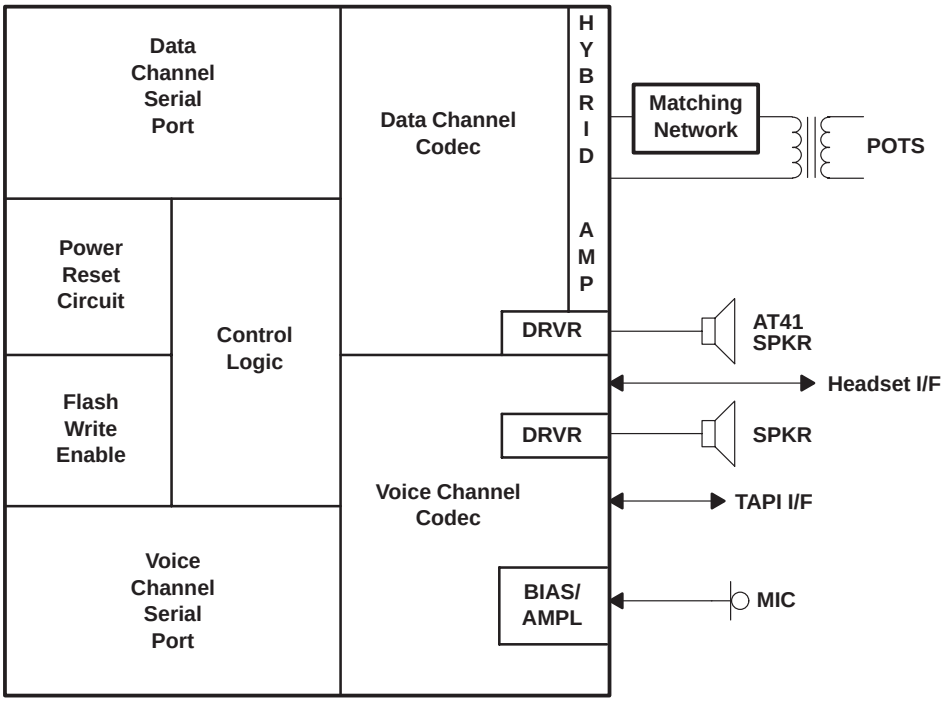
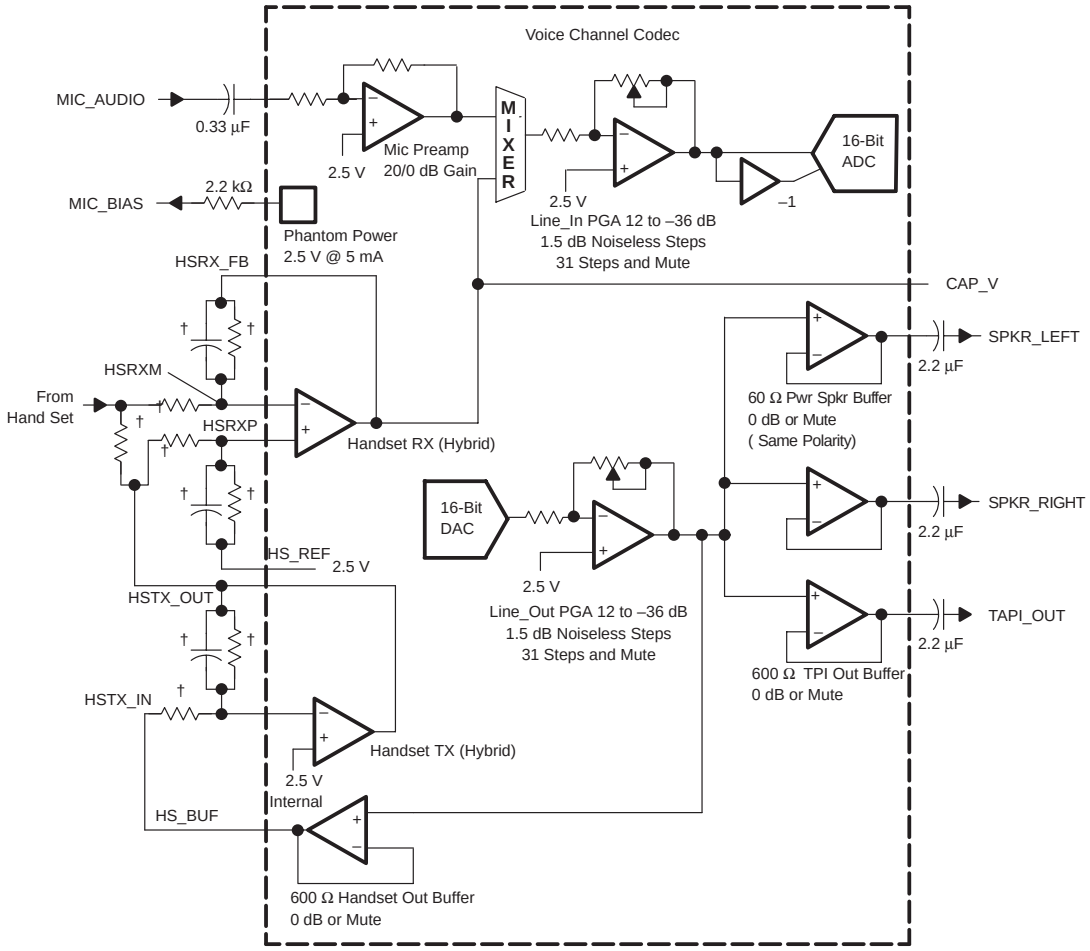
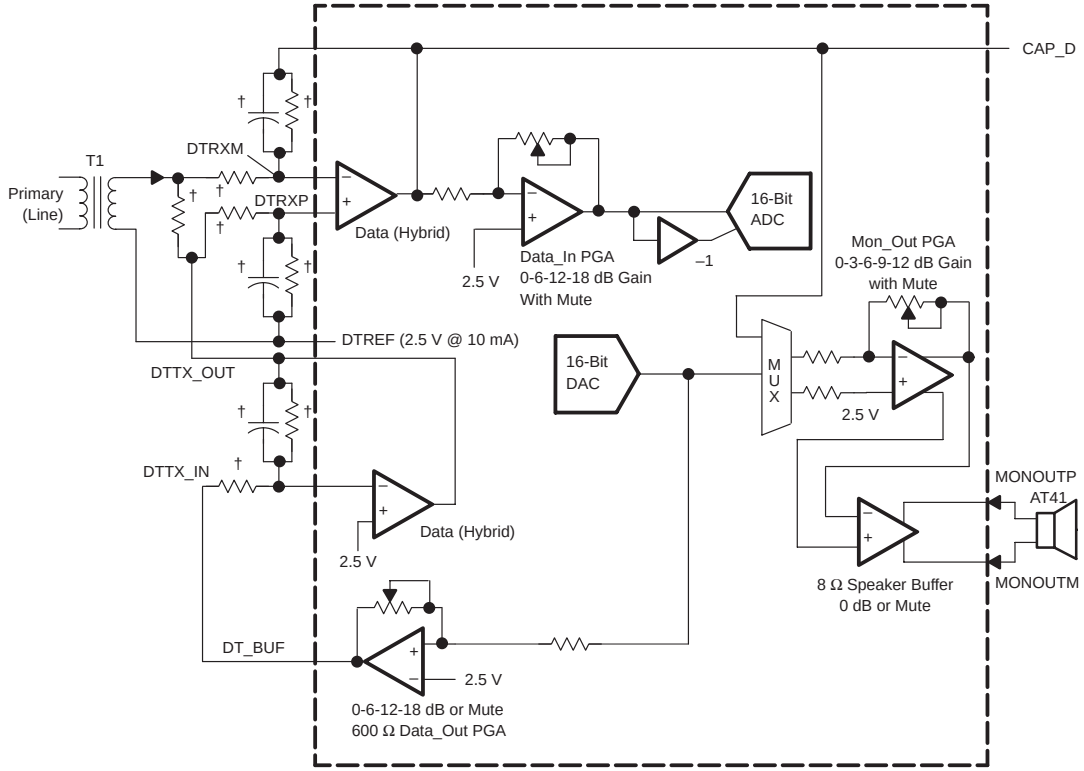


Figure 6–1. Functional Block of a Typical Application



† Required to meet communication standards

Figure 6–2. Voice Channel Codec Typical Application



† Required to meet communication standards

Figure 6–3. Data Channel Codec Typical Application

Appendix A
Programmable Register Set

Bits D12–D8 in a secondary serial communication comprise the address of the register that is written with data carried in bits D7–D0. D13 determines a read or write cycle to the addressed register. When low (0), a write cycle is selected. Table A–1 shows the register map.

Table A–1. Register Map

REGISTER NO.	D15	D14	D13	D12	D11	D10	D9	D8	REGISTER NAME
0	0	0	R/$\overline{W}$	0	0	0	0	0	No operation
1	0	0	R/$\overline{W}$	0	0	0	0	1	Control 1
2	0	0	R/$\overline{W}$	0	0	0	1	0	Control 2
3	0	0	R/$\overline{W}$	0	0	0	1	1	Control 3
4	0	0	R/$\overline{W}$	0	0	1	0	0	Control 4
5	0	0	R/$\overline{W}$	0	0	1	0	1	Control 5
6	0	0	R/$\overline{W}$	0	0	1	1	0	Control 6

Table A–2. Control 1 Register, Data Channel Control

D7	D6	D5	D4†	D3	D2	D1	D0	DESCRIPTION
1	—	—	0	—	—	—	—	Software reset for data channel asserted
0	—	—	0	—	—	—	—	Software reset for data channel not asserted
—	1	—	0	—	—	—	—	S/W power down for data channel enabled
—	0	—	0	—	—	—	—	S/W power down for data channel disabled
—	—	1	0	—	—	—	—	Data channel digital loopback asserted
—	—	0	0	—	—	—	—	Data channel digital loopback not asserted
—	—	—	0	1	—	—	—	Select data_in PGA for monitor amp input
—	—	—	0	0	—	—	—	Select DAC output for monitor amp input
—	—	—	0	—	1	0	1	Monitor amp PGA gain = 12 dB
—	—	—	0	—	1	0	0	Monitor amp PGA gain = 9 dB
—	—	—	0	—	0	1	1	Monitor amp PGA gain = 6 dB
—	—	—	0	—	0	1	0	Monitor amp PGA gain = 3 dB
—	—	—	0	—	0	0	1	Monitor amp PGA gain = 0 dB
—	—	—	0	—	0	0	0	Monitor amp PGA gain = mute

† D4 = reserved
Default value: 00000000

Table A–3. Control 2 Register, Data Channel Control

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	0	0	—	—	—	—	—	Data in (DTRX) PGA gain = mute
0	1	1	—	—	—	—	—	Data in (DTRX) PGA gain = 18 dB
0	1	0	—	—	—	—	—	Data in (DTRX) PGA gain = 12 dB
0	0	1	—	—	—	—	—	Data in (DTRX) PGA gain = 6 dB
0	0	0	—	—	—	—	—	Data in (DTRX) PGA gain = 0 dB
—	—	—	1	0	0	—	—	DAC Data out PGA gain = Mute
—	—	—	0	1	1	—	—	DAC Data out PGA gain = –18 dB
—	—	—	0	1	0	—	—	DAC Data out PGA gain = –12 dB
—	—	—	0	0	1	—	—	DAC Data out PGA gain = –6 dB
—	—	—	0	0	0	—	—	DAC Data out PGA gain = 0 dB
—	—	—	—	—	—	1	—	8 ohm monitor speaker driver gain = 0 dB
—	—	—	—	—	—	0	—	8 ohm monitor speaker driver gain = Mute
—	—	—	—	—	—	—	X	Data Channel ADC overflow indicator: ← 1 = overflow

Default value: 00000000

Table A–4. Control 3 Register, Voice Channel Control

D7	D6	D5	D4	D3†	D2	D1	D0	DESCRIPTION
1	—	—	—	0	—	—	—	Voice channel software reset
0	—	—	—	0	—	—	—	Voice channel software reset not asserted
—	1	—	—	0	—	—	—	Software power down for voice channel enabled
—	0	—	—	0	—	—	—	Software power down for voice channel disabled
—	—	1	—	0	—	—	—	Voice channel digital loopback
—	—	0	—	0	—	—	—	Voice channel digital loopback not asserted
—	—	—	1	0	—	—	—	Voice channel digital loopback
—	—	—	0	0	—	—	—	Voice channel digital loopback not asserted
—	—	—	—	0	1	—	—	Microphone preamp selected for ADC input
—	—	—	—	0	0	—	—	Microphone preamp not selected for ADC input
—	—	—	—	0	—	1	—	Handset preamp not selected for ADC input
—	—	—	—	0	—	0	—	Handset preamp selected for ADC input
—	—	—	—	0	—	—	1	TAPI output buffer gain = mute
—	—	—	—	0	—	—	0	TAPI output buffer gain = 0 dB

† D3 = reserved

Default value: 00000000

Table A–5. Control 4 Register, Voice Channel Control

D7†	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
0	1	—	—	—	—	—	—	Microphone preamp gain = 20 dB
0	0	—	—	—	—	—	—	Microphone preamp gain = 0 dB
0	—	1	1	0	0	0	0	Voice ADC input PGA gain = mute
0	—	1	0	0	0	0	1	Voice ADC input PGA gain = 12 dB
0	—	1	0	0	0	0	0	Voice ADC input PGA gain = 10.5 dB
0	—	0	1	1	1	1	1	Voice ADC input PGA gain = 9 dB
0	—	0	1	1	1	1	0	Voice ADC input PGA gain = 7.5 dB
0	—	0	1	1	1	0	1	Voice ADC input PGA gain = 6 dB
0	—	0	1	1	1	0	0	Voice ADC input PGA gain = 4.5 dB
0	—	0	1	1	0	1	1	Voice ADC input PGA gain = 3 dB
0	—	0	1	1	0	1	0	Voice ADC input PGA gain = 1.5 dB
0	—	0	1	1	0	0	1	Voice ADC input PGA gain = 0 dB
0	—	0	1	1	0	0	0	Voice ADC input PGA gain = –1.5 dB
0	—	0	1	0	1	1	1	Voice ADC input PGA gain = –3 dB
0	—	0	1	0	1	1	0	Voice ADC input PGA gain = –4.5 dB
0	—	0	1	0	1	0	1	Voice ADC input PGA gain = –6 dB
0	—	0	1	0	1	0	0	Voice ADC input PGA gain = –7.5 dB
0	—	0	1	0	0	1	1	Voice ADC input PGA gain = –9 dB
0	—	0	1	0	0	1	0	Voice ADC input PGA gain = –10.5 dB
0	—	0	1	0	0	0	1	Voice ADC input PGA gain = –12 dB
0	—	0	1	0	0	0	0	Voice ADC input PGA gain = –13.5 dB
0	—	0	0	1	1	1	1	Voice ADC input PGA gain = –15 dB
0	—	0	0	1	1	1	0	Voice ADC input PGA gain = –16.5 dB
0	—	0	0	1	1	0	1	Voice ADC input PGA gain = –18 dB
0	—	0	0	1	1	0	0	Voice ADC input PGA gain = –19.5 dB
0	—	0	0	1	0	1	1	Voice ADC input PGA gain = –21 dB
0	—	0	0	1	0	1	0	Voice ADC input PGA gain = –22.5 dB
0	—	0	0	1	0	0	1	Voice ADC input PGA gain = –24 dB
0	—	0	0	1	0	0	0	Voice ADC input PGA gain = –25.5 dB
0	—	0	0	0	1	1	1	Voice ADC input PGA gain = –27 dB
0	—	0	0	0	1	1	0	Voice ADC input PGA gain = –28.5 dB
0	—	0	0	0	1	0	1	Voice ADC input PGA gain = –30 dB
0	—	0	0	0	1	0	0	Voice ADC input PGA gain = –31.5 dB
0	—	0	0	0	0	1	1	Voice ADC input PGA gain = –33 dB
0	—	0	0	0	0	1	0	Voice ADC input PGA gain = –34.5 dB
0	—	0	0	0	0	0	1	Voice ADC input PGA gain = –36 dB
0	—	0	0	0	0	0	0	Voice ADC input PGA gain = 0 dB

† D7 = reserved
Default value: 00000000

Table A–6. Control 5 Register, Voice Channel Control

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	1	0	0	0	0	—	—	Voice DAC output PGA gain = mute
1	0	0	0	0	1	—	—	Voice DAC output PGA gain = 12 dB
1	0	0	0	0	0	—	—	Voice DAC output PGA gain = 10.5 dB
0	1	1	1	1	1	—	—	Voice DAC output PGA gain = 9 dB
0	1	1	1	1	0	—	—	Voice DAC output PGA gain = 7.5 dB
0	1	1	1	0	1	—	—	Voice DAC output PGA gain = 6 dB
0	1	1	1	0	0	—	—	Voice DAC output PGA gain = 4.5 dB
0	1	1	0	1	1	—	—	Voice DAC output PGA gain = 3 dB
0	1	1	0	1	0	—	—	Voice DAC output PGA gain = 1.5 dB
0	1	1	0	0	1	—	—	Voice DAC output PGA gain = 0 dB
0	1	1	0	0	0	—	—	Voice DAC output PGA gain = –1.5 dB
0	1	0	1	1	1	—	—	Voice DAC output PGA gain = –3 dB
0	1	0	1	1	0	—	—	Voice DAC output PGA gain = –4.5 dB
0	1	0	1	0	1	—	—	Voice DAC output PGA gain = –6 dB
0	1	0	1	0	0	—	—	Voice DAC output PGA gain = –7.5 dB
0	1	0	0	1	1	—	—	Voice DAC output PGA gain = –9 dB
0	1	0	0	1	0	—	—	Voice DAC output PGA gain = –10.5 dB
0	1	0	0	0	1	—	—	Voice DAC output PGA gain = –12 dB
0	1	0	0	0	0	—	—	Voice DAC output PGA gain = –13.5 dB
0	0	1	1	1	1	—	—	Voice DAC output PGA gain = –15 dB
0	0	1	1	1	0	—	—	Voice DAC output PGA gain = –16.5 dB
0	0	1	1	0	1	—	—	Voice DAC output PGA gain = –18 dB
0	0	1	1	0	0	—	—	Voice DAC output PGA gain = –19.5 dB
0	0	1	0	1	1	—	—	Voice DAC output PGA gain = –21 dB
0	0	1	0	1	0	—	—	Voice DAC output PGA gain = –22.5 dB
0	0	1	0	0	1	—	—	Voice DAC output PGA gain = –24 dB
0	0	1	0	0	0	—	—	Voice DAC output PGA gain = –25.5 dB
0	0	0	1	1	1	—	—	Voice DAC output PGA gain = –27 dB
0	0	0	1	1	0	—	—	Voice DAC output PGA gain = –28.5 dB
0	0	0	1	0	1	—	—	Voice DAC output PGA gain = –30 dB
0	0	0	1	0	0	—	—	Voice DAC output PGA gain = –31.5 dB
0	0	0	0	1	1	—	—	Voice DAC output PGA gain = –33 dB
0	0	0	0	1	0	—	—	Voice DAC output PGA gain = –34.5 dB
0	0	0	0	0	1	—	—	Voice DAC output PGA gain = –36 dB
0	0	0	0	0	0	—	—	Voice DAC output PGA gain = 0 dB
—	—	—	—	—	—	1	—	60 Ω Spkr_L/R buffer gain = 0 dB
—	—	—	—	—	—	0	—	60 Ω Spkr_L/R buffer gain = Mute
—	—	—	—	—	—	—	X	Voice Channel ADC overflow: 1 = overflow

Default value: 00000000

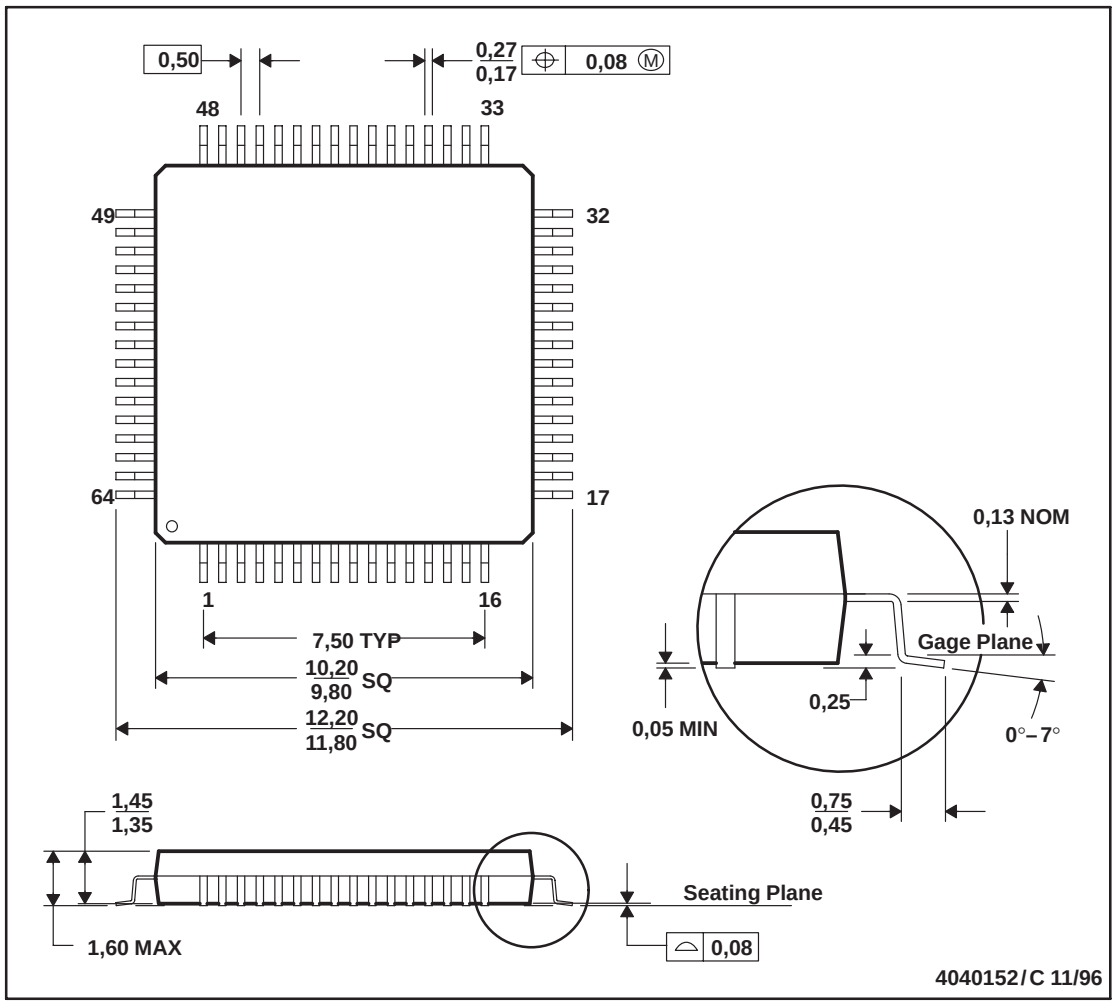
Table A–7. Control 6 Register, Voice Channel Control

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	—	—	—	—	—	—	—	Handset out buffer gain = mute
0	—	—	—	—	—	—	—	Handset out buffer gain = 0 dB
—	X	X	X	X	X	X	X	Reserved

Default value: 00000000

Appendix B
Mechanical Data

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

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