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TLC2932 Evaluation Module

Technical Reference

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Mixed-Signal Products

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TLC2932 Evaluation Module Technical Reference

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October 1997

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Read This First

About This Manual

The Texas Instruments (TI™) TLC2932 Evaluation Module Technical Reference Manual for the TLC2932 high-performance phase-locked loop provides information to assist managers and hardware/software engineers in application development.

How to Use This Manual

This document contains the following chapters:

Chapter 1 **Overview**
A general description of the TLC2932 Evaluation Module (TLC2932EVM), key features, and a functional overview are included.

Chapter 2 **Hardware**
A general description of the TLC2932EVM hardware is included.

Appendix A **TLC2932 Data Sheet**
A copy of the TLC2932 data sheet is included.

Appendix B **TC9122P Data Sheet Summary**
A summary of the TC9122P data sheet is included.

Symbol Convention

This document uses the following convention:

TC TOSHIBA device number prefix

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This book may contain cautions and warnings.

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The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

TLC2932 High-Performance Phase-Locked Loop Data Sheet (literature number SLAS097E) is included in Appendix A of this book. It contains electrical specifications, available temperature options, general overview of the device, and application information.

TLC2932 Phase-Locked Loop Building Block With Analog Voltage-Controlled Oscillator and Phase Frequency Detector Application Report (literature number SLAA011B) contains an overview of phase-locked loop functional blocks, transfer function analyses, evaluation module (EVM) board design, and performance characteristics.

Data Acquisition Circuits Data Book (literature number SLAD001) contains the data sheets for devices that perform analog-to-digital, digital-to-analog, and related functions. It also has selection tables and package and ordering information.

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Contents

Figures

Tables

Chapter 1

Overview

The TLC2932 evaluation module (TLC2932EVM) provides a method to evaluate the performance of the TLC2932 phase-locked-loop (PLL) building block. The TLC2932EVM contains a phase frequency detector (PFD) and a voltage-controlled oscillator (VCO). This manual explains how to construct basic frequency synthesis circuits including the design of a low-pass filter (LPF). This chapter includes the following topics:

Topic **Page**

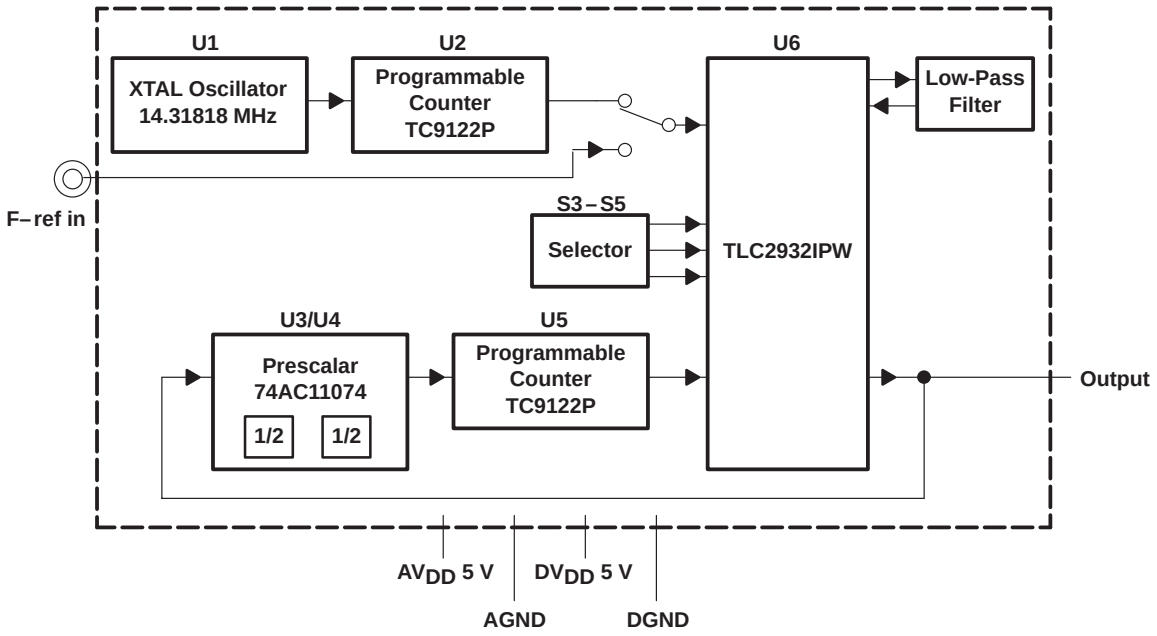
1.1 Introduction

The TLC2932EVM for the TLC2932IPW Texas Instruments CMOS phase-locked loop (PLL) integrated circuit (IC) contains a TLC2932IPW, two TC9122P programmable counters, a loop filter, and other devices, as shown in Figure 1–1. These devices comprise a clock synthesizer on the module to evaluate basic PLL functionality and performance. The general external connections of the TLC2932EVM are shown in Figure 1–2.

The TLC2932EVM includes the following:

- A reference frequency is generated by the crystal (XTAL) oscillator and supplied to PFD input through the programmable counter. An external reference (F–ref in) can be input through the Baby N Connector (BNC).
- The 14.31818-MHz XTAL oscillator on the EVM is a standard part. It can be replaced by any other XTAL oscillator with an oscillation frequency in the functional range of the TC9122P programmable counter.
- A lag-lead filter standard connection is available on the board. For more flexible filter design, a free area beside the socket of TLC2932IPW is provided.
- Dip switches on the board are used to set the TC9122P programmable counter and can be used to set the N/M counter as a frequency synthesizer.

Figure 1–1. TLC2932EVM Block Diagram



1.2 TLC2932EVM Operating Specifications

If the on-board XTAL oscillator supplied with the EVM is used, DV_{DD} should be adjusted to 5.5 V instead of 5 V nominal because of the improved performance of the TC9122P counter at the higher DV_{DD}.

Table 1–1 lists the supply voltage operating specifications.

Table 1–1. Supply Voltage Operating Specifications

Clock Generator Used	DV_{DD} (nominal) (V)	AV_{DD} (nominal) (V)
On-board oscillator with TC9122P programmable counter	5.5	5
Externally applied reference frequency at F–ref in	5	5

1.3 Evaluation of the Clock Synthesizer

This section includes a typical evaluation using the TLC2932EVM. The PLL block [voltage-controlled oscillator (VCO), phase frequency detector (PFD), low-pass filter (LPF), and counter] parameters of this evaluation include the following:

VCO: R1 = 2.2 kΩ as R_{BIAS}, lock frequency = 14.31818 MHz

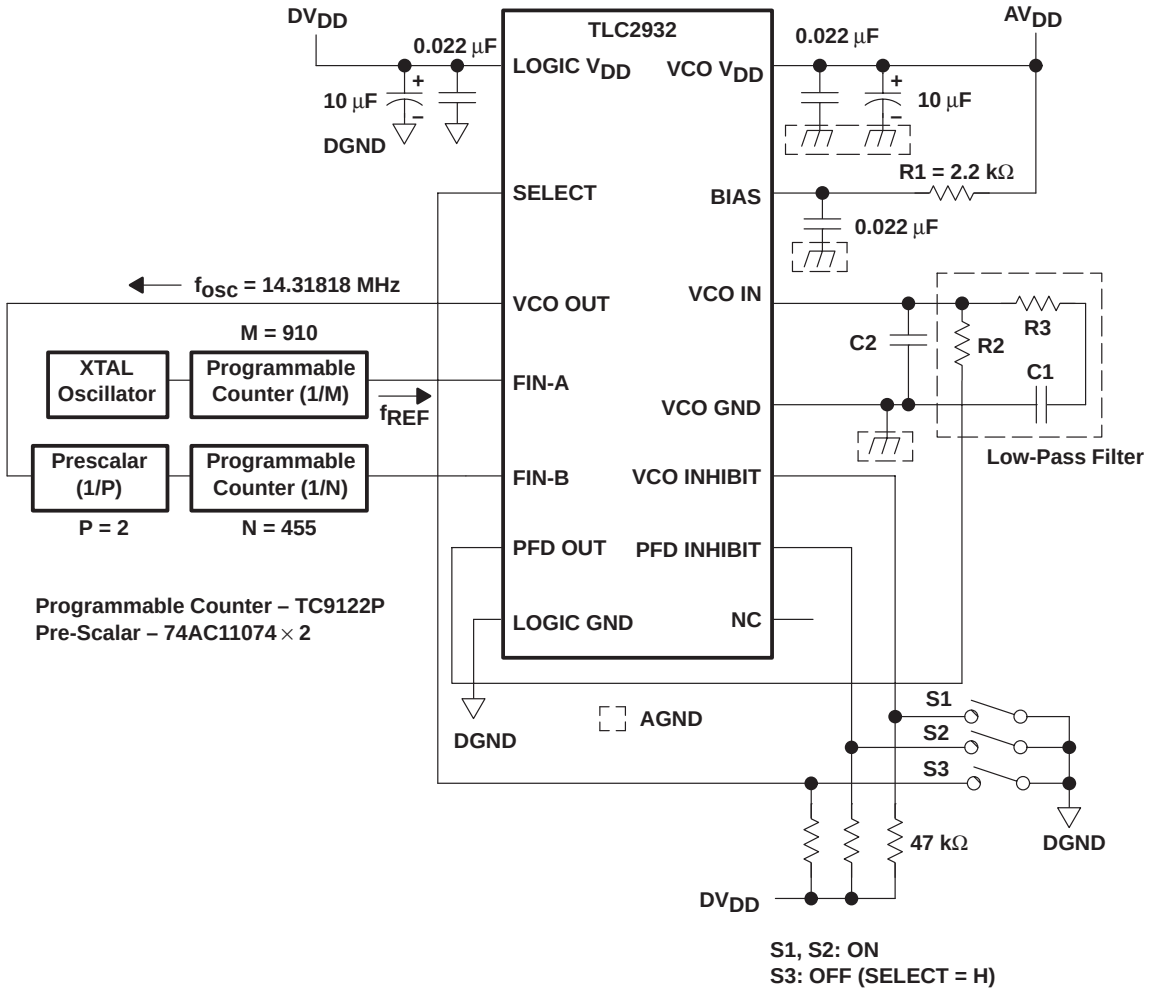
PFD: Comparison frequency = f_{REF} = 15.734 kHz, 14.31818-MHz XTAL oscillator as reference

LPF: Lag-lead filter C and R values are calculated in the following section

Counter: N/M = 455/910, 1/2 divide prescalar (P = 2)

Figure 1–2 shows a block diagram of the TLC2932EVM with the given conditions set.

Figure 1–2. TLC2932EVM Block Diagram With the Given Conditions Set



1.3.1 Calculation of the LPF C and R Values

This section examines the calculations used to derive the C and R values for the lag-lead filter. The design parameters selected for this example include the following:

VCO range: Selected from the VCO characteristic curve below (see Figure 1–3)

Lock up time: t_S = 1 ms

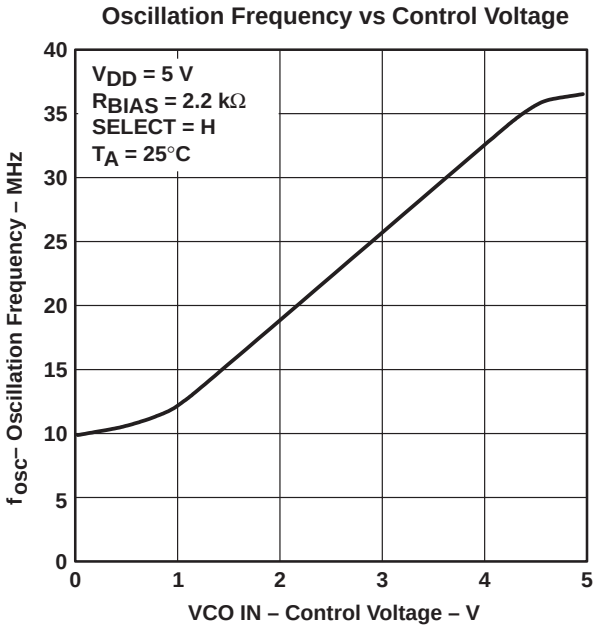
P · N count: 910

Damping factor: $\zeta = 0.7$

Selected radians to lock-up time: $\omega_n t_S = 4.5$ rad

Natural angular frequency: $\omega_n = \omega_n t_S / t_S = 4500$ rad/sec (1)

Figure 1–3. VCO Characteristic Curve



In the case of the lag-lead filter, ω_n and ζ are calculated according to the following equations:

$$\omega_n = \sqrt{(Kp \cdot Kv)/\{(P \cdot N) \cdot (T1 + T2)\}} \quad (2)$$

$$\zeta = \left(\omega_n/2\right) \cdot \left[T2 + \left(N/(Kp \cdot Kv)\right)\right] \quad (3)$$

$$(T1 = R2 \cdot C1,\ T2 = R3 \cdot C1)$$

PFD gain

$$Kp = \frac{V_{OH} - V_{OL}}{4\pi} \cong 0.32 \text{ V/rad} \quad (4)$$

where V_{OH} and V_{OL} are obtained from the data sheet

VCO gain from Figure 1–3

$$Kv = \left[\left\{(32 - 12)\text{MHz} \cdot 10^6\right\}/(4 - 1)\text{V}\right] \cdot 2\pi \quad (5)$$

$$\cong 41.9 \text{ Mrad/V/sec}$$

The R2 and R3 values for the LPF are calculated according to the following equations:

$$R2 = \left[\left\{\left(Kp \cdot Kv/\omega_n{}^2\right) \cdot 1/(P \cdot N)\right\} - \left\{\left(2\zeta/\omega_n\right) + N/(Kp \cdot Kv)\right\}\right]/C1 \quad (6)$$

$$R3 = \left\{\left(2\zeta/\omega_n\right) - N/(Kp \cdot Kv)\right\}/C1 \quad (7)$$

When C1 is set to 1 μF, the R2 and R3 calculated values are:

R2 = 470 Ω, R3 = 240 Ω

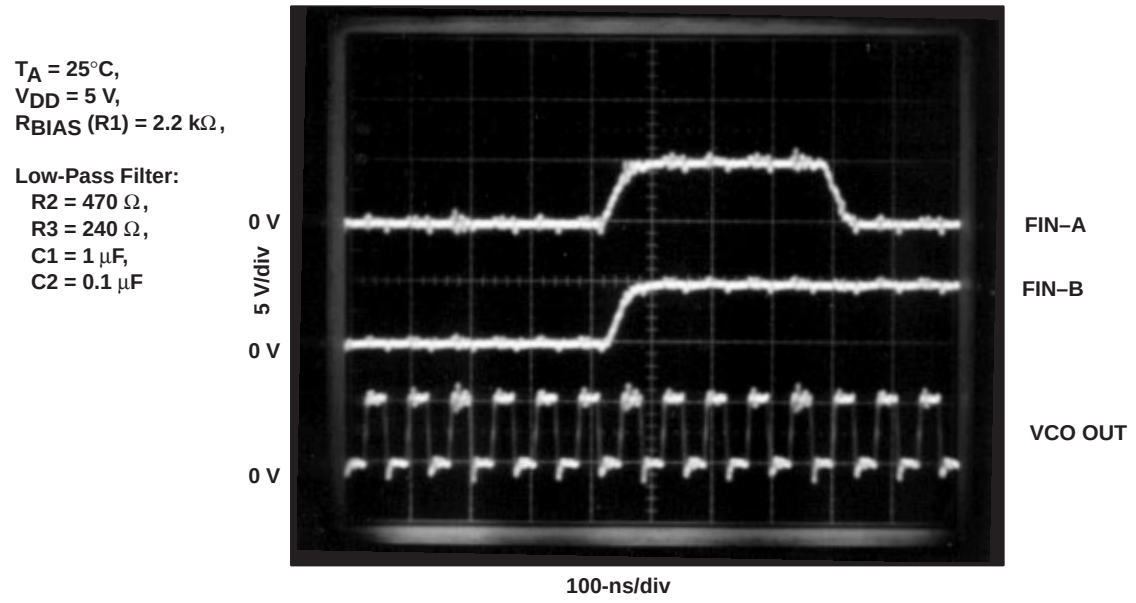
Capacitor C2 is added to minimize high-frequency pickup at the VCO input, and the C2 value should be set equal to or smaller than C1 · 1/10 to have a minimal effect on the LPF poles, hence:

C2 = 0.1 μF is selected for this application.

1.3.2 Evaluation Board Output Waveform

Figure 1–4 shows the input frequencies and the VCO output waveform using the C and R values calculated in the previous section.

Figure 1–4. Input Frequencies and VCO Output Waveform



1.3.3 Using an Active Filter as the LPF

For active filtering on the EVM, space is available to build the filter using an operational amplifier. Note the inverted output of the filter; this inverted output can be compensated for by changing the JP2 connections of 1 to 4, 2 to 3 (normally 1 to 2, 3 to 4 for lag-lead filter).

To find the best C and R values for each application, some evaluation may be required. The LPF characteristics resulting from standard values of R and C can cause the PLL performance to be slightly different from theoretical results.

1.4 Operation Notes

- When an external reference frequency is input through the J1 connector, an R7 resistor should be inserted as termination.
- The VCO output should drive only one external device to avoid overload.
- Because this evaluation board has a high-frequency VCO functional block, it requires the closest connection and shortest possible lead-in of each I/O to optimize board performance.
- The supply voltage for this board should be 5 V or as specified in Section 1.2, *TLC2932EVM Operating Specifications,* as determined by the peripheral IC supply voltage requirements, because the TLC2932IPW can use both 5 V and 3 V.
- For details of the 74AC11074 prescalar on this board, see the TI *CMOS Data Book*.
- For a description of the programmable counter functions, see the general reference information included in this document from the TOSHIBA TC9122P data sheet.
- A bypass capacitor for the BIAS terminal should be used for any application and placed as close as possible to terminal 13. This capacitor is included on the TLC2932EVM and designated as C17.

Chapter 2

Hardware

This chapter includes the following topics:

2.1 Board Schematic

The TLC2932EVM board schematic is shown in Figure 2–1.

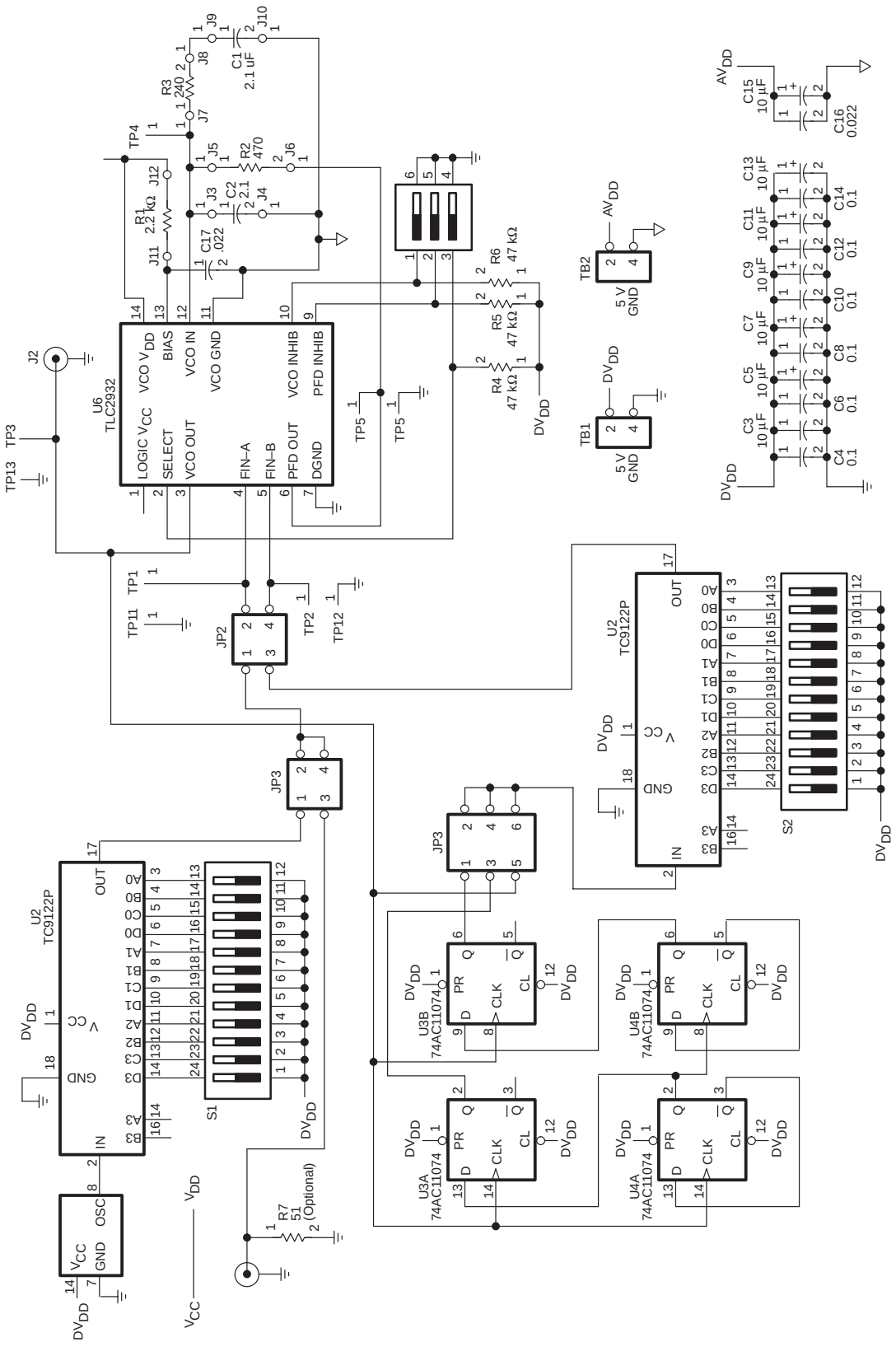
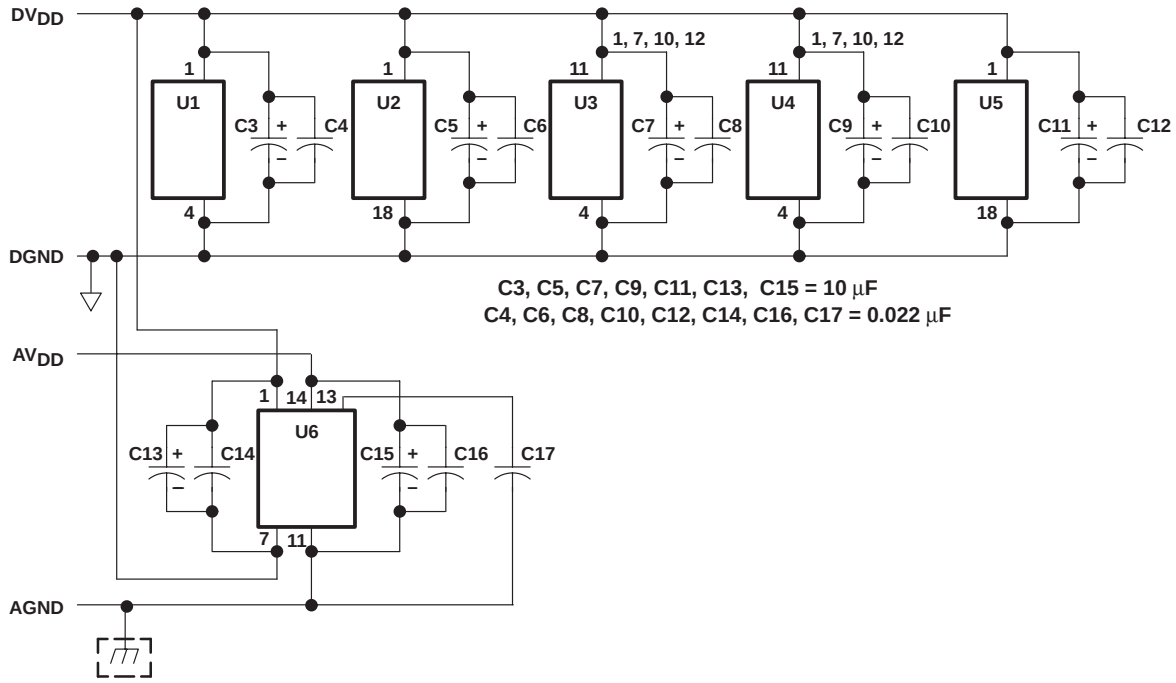


Figure 2–1. TLC2932EVM Board Schematic

2.2 Power, Ground, and Capacitor Connections

The power, ground, and capacitor connections of the TLC2932EVM are shown in Figure 2–2.

Figure 2–2. V_{DD} and GND Line Connections and Bypass Capacitors



2.3 Board Layout

The TLC2932EVM board layout is shown in Figure 2–3.

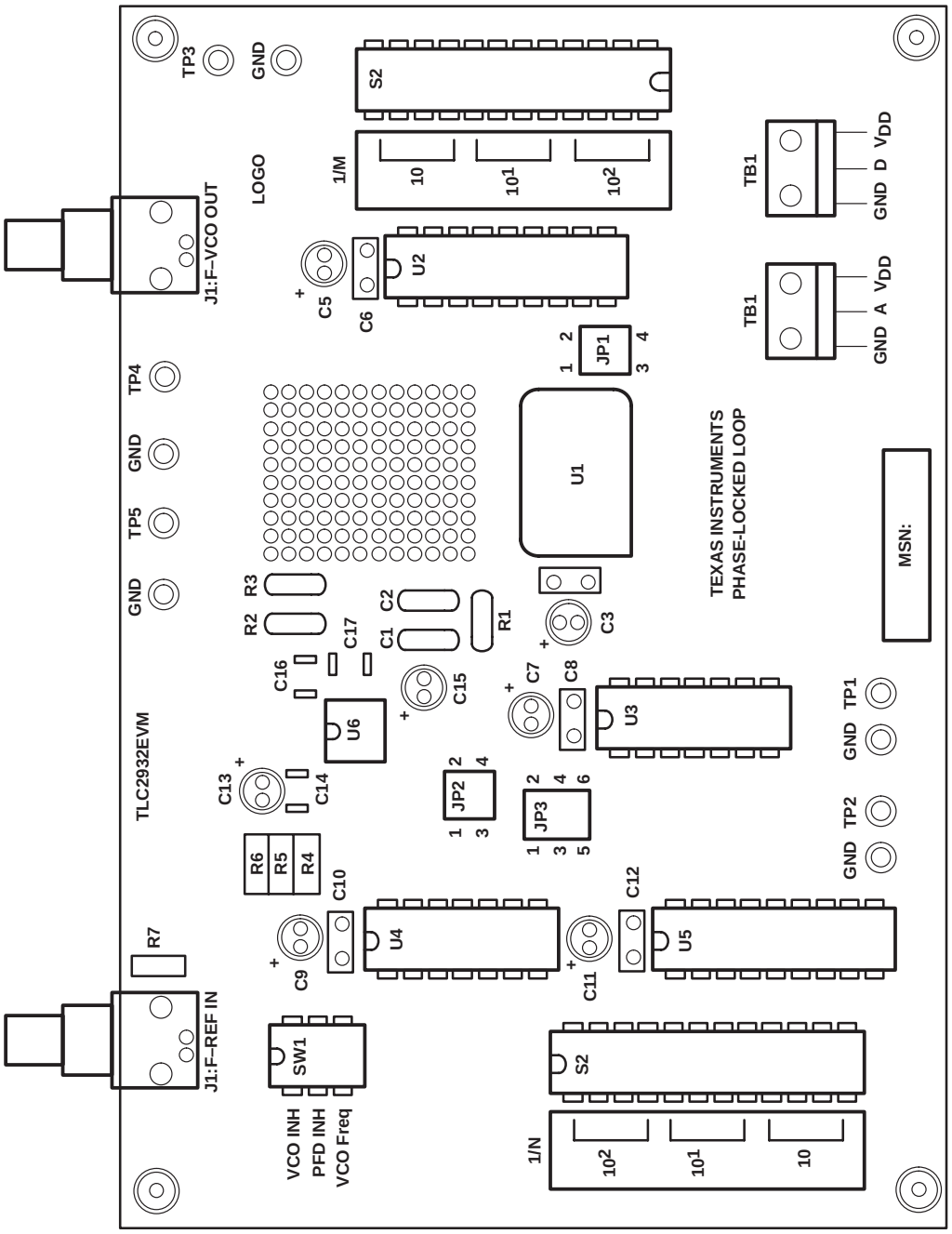


Figure 2–3. TLC2932EVM Board Layout

2.4 Board Layers

Figure 2–4. Layer 1

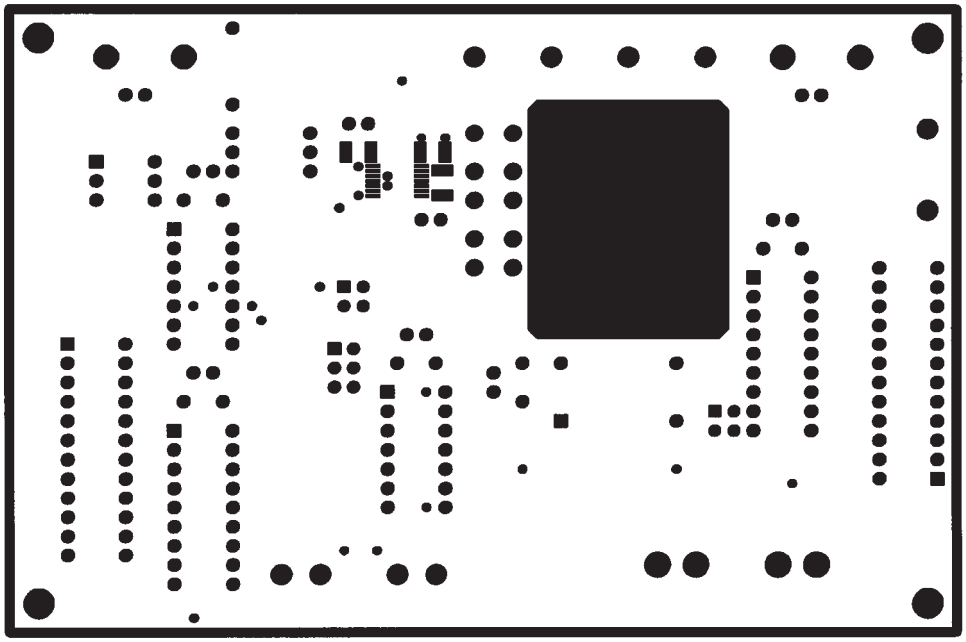


Figure 2–5. Layer 2

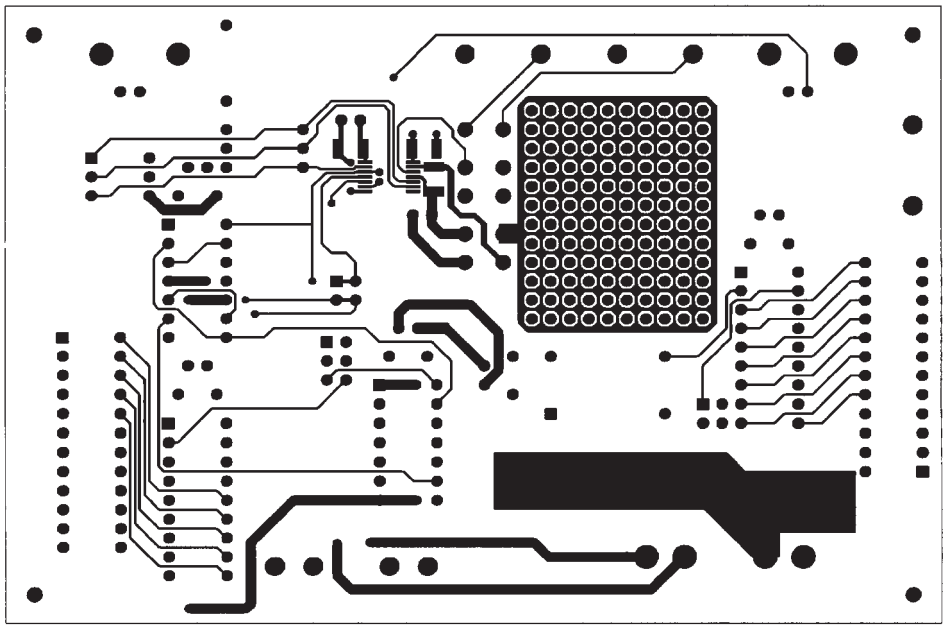


Figure 2–6. Layer 3

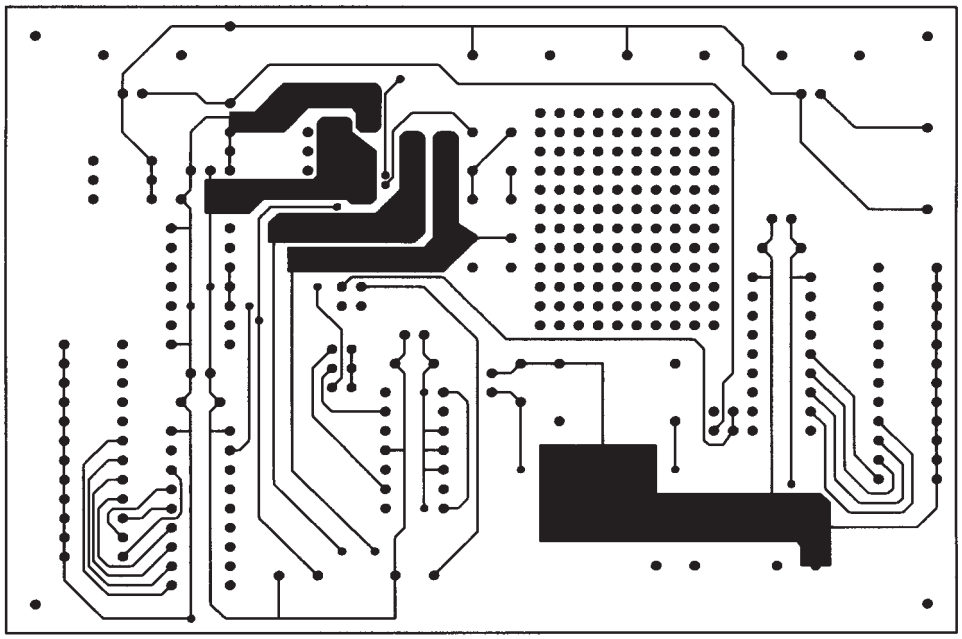
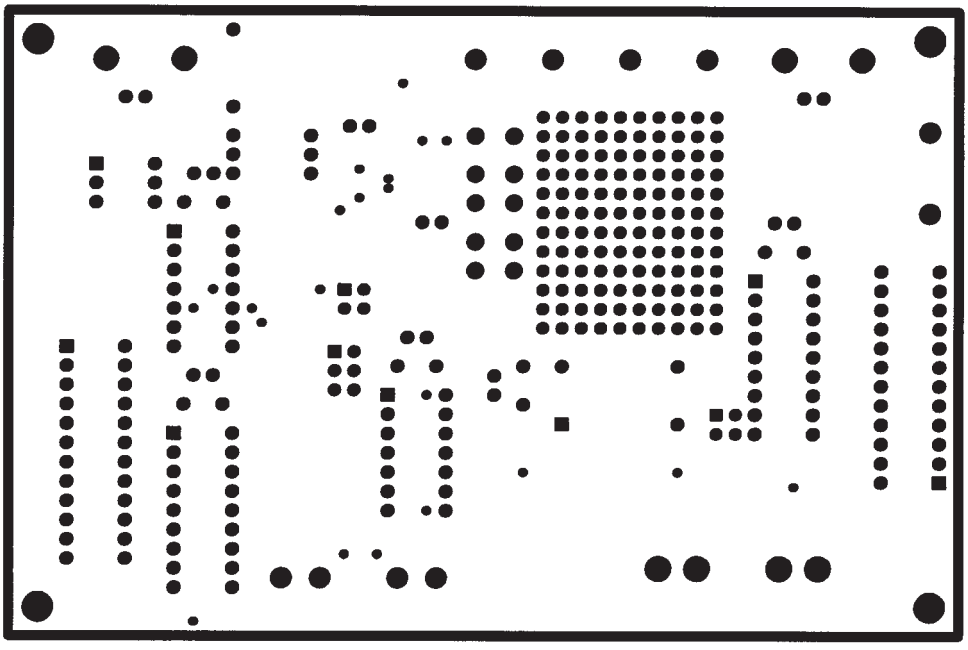


Figure 2–7. Layer 4



2.5 Part Descriptions

The TLC2932EVM parts are listed in Table 2–1.

Table 2–1. Part Descriptions

Number	Quantity	Reference	Description
1	1	C1	1-μF ceramic capacitor, 0.2-inch LS, (AVX SR30C105KAA or equivalent)
2	1	C2	0.1-μF ceramic capacitor, 0.2-inch LS, (AVX SR215C104KAA or equivalent)
3	7	C3, C5, C7, C9 C11, C13, C15	10-μF 16-V aluminum capacitors
4	5	C4, C6, C8, C10, C12	0.1-μF ceramic capacitors, 0.2 inch LS, radial lead (AVX SR21C104KAA or equivalent)
5	3	C14, C16, C17	0.022-μF capacitors, X7R, 1206 SMT
6	1	JP1	Header 2 x 2
7	1	JP3	Header 3 x 2
8	2	J1, J2	BNC connectors, PCB mount, RT angle
9	10	J3, J4, J5, J6, J7, J8, J9, J10, J11, J12	Pin sockets
10	1	R1	2.2 kΩ, 5%, 1/4 W resistor
11	1	R2	470 Ω, 5%, 1/4 W resistor
12	1	R3	240 Ω, 5%, 1/4 W resistor
13	3	R4, R5, R6	47 kΩ, 5%, 1/4 W resistors
14	2	S1, S2	12-position DIP switch
15	1	S3	3-position DIP switch
16	2	(JP1, JP3)	Shorting plug, header pin
17	2	TB1, TB2	Term block, screw terminal
18	10	TP1, TP2, TP3, TP4, TP5, TP11, TP12, TP13, TP14, TP15	Terminal, test point
19	1	U1	XTAL oscillator 14.31818 MHz
20	2	U2, U5	TC9122 programmable counter
21	2	U3, U4	74AC11074 prescalar
22	1	U6	TLC2932 PLL functional block
23	2	[JP2] (1–2, 3–4)	Bus wire, #24
24	1		PC board

Appendix A

TLC2932 Data Sheet

This appendix presents a copy of the TLC2932 data sheet.

A.1 TLC2932 Data Sheet

Appendix B

TC9122P Data Sheet Summary

This appendix presents a summary of the TC9122P data sheet.

Topic **Page**

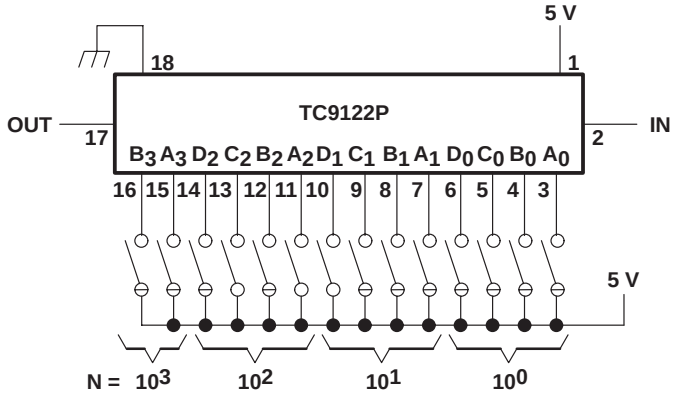
B.1 Reference Information for the TC9122P Programmable Counter

The device connections, terminal functions, absolute maximum ratings, and electrical characteristics reference data included in this document is from the TOSHIBA TC9122P data sheet.

B.2 Device Connections

The connections of the TC9122P are shown in Figure B–1.

Figure B–1. TC9122P Connections



B.3 Terminal Functions

The TC9122P terminal functions are shown in Table B–1.

Table B–1.TC9122P Terminal Functions

Terminal No.	Name		Description	Notes
2	IN		Programmable counter input. As this input has the self-biased amplifier internally, input frequency can be a small signal by capacitive coupling the input.	Internal amplifier
3–6	A_0–D_0	10^0	Program input to set divide value N by BCD. N can be set from 8 to 3999. The values below must not be set. (see values below)	Each terminal has a pull-down resistor internally.
7–10	A_1–D_1	10^1		
11–14	A_2–D_2	10^2		
15, 16	A_3, B_3	10^3		
17	OUT		Programmable counter output. 1/N of the IN frequency appears at this output.	
1, 18	V_{DD}, GND		Power supply and ground.	

A_0	B_0	C_0	D_0	A_1	B_1	C_1	D_1	A_2	B_2	C_2	D_2	A_3	B_3
1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0

B.4 Absolute Maximum Ratings, T_A = 25°C

The TC9122P absolute maximum ratings at T_A = 25°C are shown in Table B–2.

Table B–2.TC9122P Absolute Maximum Ratings

Supply voltage range, V_{DD}	–0.3 V to 10 V
Input voltage range, V_I	–0.3 V to V_{CC} + 0.3 V
Operating temperature range, T_A	–30°C to 75°C
Storage temperature range, T_{stg}	–55°C to 125°C

B.5 Electrical Characteristics at V_{DD} = 7.5 V, T_A = 25°C

The TC9122P electrical characteristics are shown in Table B–3.

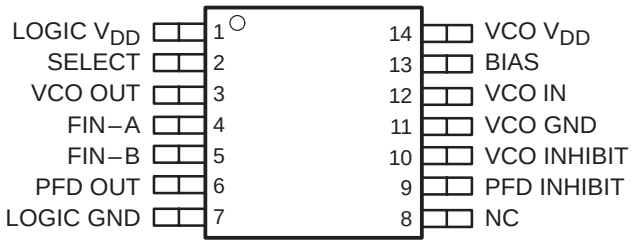
Table B–3.TC9122P Electrical Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage		4.5		8.5	V
$V_{I(PP)}$	Input voltage swing	f_I = 15 MHz, V_I = 2 Vp-p	2		7	Vp-p
I_{DD}	Supply current			15	30	mA
V_{IH}	High-level input voltage		5.5		V_{DD}+0.3	V
V_{IL}	Low-level input voltage		–0.3		2	V
V_{OH}	High-level output voltage	I_{OH} = –0.5 mA	6.5			V
V_{OL}	Low-level output voltage	I_{OL} = 0.5 mA			1	V
f	Operating frequency (see Note 1)		1		15	MHz
R_{IN}	Input pulldown resistor		20		80	kΩ
R_f	Amplifier feedback resistor		100		500	kΩ

NOTE 1: V_{DD} = 7.5 V ±10%, $V_{I(PP)}$ = 2 Vp-p, T_A = 30°C to 75°C

- **Voltage-Controlled Oscillator (VCO) Section:**
  - **Complete Oscillator Using Only One External Bias Resistor (R_{BIAS})**
  - **Lock Frequency:**
    22 MHz to 50 MHz (V_{DD} = 5 V ±5%, T_A = –20°C to 75°C, ×1 Output)
    11 MHz to 25 MHz (V_{DD} = 5 V ±5%, T_A = –20°C to 75°C, ×1/2 Output)
  - **Output Frequency . . . ×1 and ×1/2 Selectable**
- **Phase-Frequency Detector (PFD) Section Includes a High-Speed Edge-Triggered Detector With Internal Charge Pump**
- **Independent VCO, PFD Power-Down Mode**
- **Thin Small-Outline Package (14 terminal)**
- **CMOS Technology**
- **Typical Applications:**
  - **Frequency Synthesis**
  - **Modulation/Demodulation**
  - **Fractional Frequency Division**
- **Application Report Available†**
- **CMOS Input Logic Level**

PW PACKAGE†
(TOP VIEW)

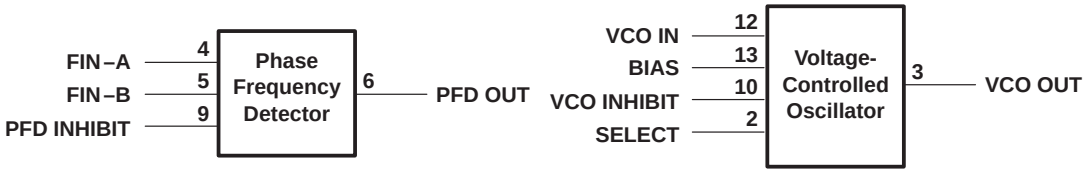


† Available in tape and reel only and ordered as the TLC2932IPWLE.
NC – No internal connection

description

The TLC2932I is designed for phase-locked-loop (PLL) systems and is composed of a voltage-controlled oscillator (VCO) and an edge-triggered-type phase frequency detector (PFD). The oscillation frequency range of the VCO is set by an external bias resistor (R_{BIAS}). The VCO has a 1/2 frequency divider at the output stage. The high-speed PFD with internal charge pump detects the phase difference between the reference frequency input and signal frequency input from the external counter. Both the VCO and the PFD have inhibit functions, which can be used as a power-down mode. The TLC2932I is suitable for use as a high-performance PLL due to the high speed and stable oscillation capability of the device.

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGE
	SMALL OUTLINE (PW)
–20°C to 75°C	TLC2932IPWLE

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† TLC2932 Phase-Locked-Loop Building Block With Analog Voltage-Controlled Oscillator and Phase Frequency Detector (SLAA011).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
FIN–A	4	I	Input reference frequency $f_{(REF\ IN)}$ is applied to FIN–A.
FIN–B	5	I	Input for VCO external counter output frequency $f_{(FIN-B)}$. FIN–B is nominally provided from the external counter.
LOGIC GND	7		GND for the internal logic.
LOGIC V_{DD}	1		Power supply for the internal logic. This power supply should be separate from VCO V_{DD} to reduce cross-coupling between supplies.
NC	8		No internal connection.
PFD INHIBIT	9	I	PFD inhibit control. When PFD INHIBIT is high, PFD output is in the high-impedance state, see Table 3.
PFD OUT	6	O	PFD output. When the PFD INHIBIT is high, PFD output is in the high-impedance state.
BIAS	13	I	Bias supply. An external resistor (R_{BIAS}) between VCO V_{DD} and BIAS supplies bias for adjusting the oscillation frequency range.
SELECT	2	I	VCO output frequency select. When SELECT is high, the VCO output frequency is $\times$1/2 and when low, the output frequency is $\times$1, see Table 1.
VCO IN	12	I	VCO control voltage input. Nominally the external loop filter output connects to VCO IN to control VCO oscillation frequency.
VCO INHIBIT	10	I	VCO inhibit control. When VCO INHIBIT is high, VCO OUT is low (see Table 2).
VCO GND	11		GND for VCO.
VCO OUT	3	O	VCO output. When the VCO INHIBIT is high, VCO output is low.
VCO V_{DD}	14		Power supply for VCO. This power supply should be separated from LOGIC V_{DD} to reduce cross-coupling between supplies.

detailed description

VCO oscillation frequency

The VCO oscillation frequency is determined by an external resistor (R_{BIAS}) connected between the VCO V_{DD} and the BIAS terminals. The oscillation frequency and range depends on this resistor value. The bias resistor value for the minimum temperature coefficient is nominally 3.3 kΩ with 3-V at the VCO V_{DD} terminal and nominally 2.2 kΩ with 5-V at the VCO V_{DD} terminal. For the lock frequency range refer to the recommended operating conditions. Figure 1 shows the typical frequency variation and VCO control voltage.

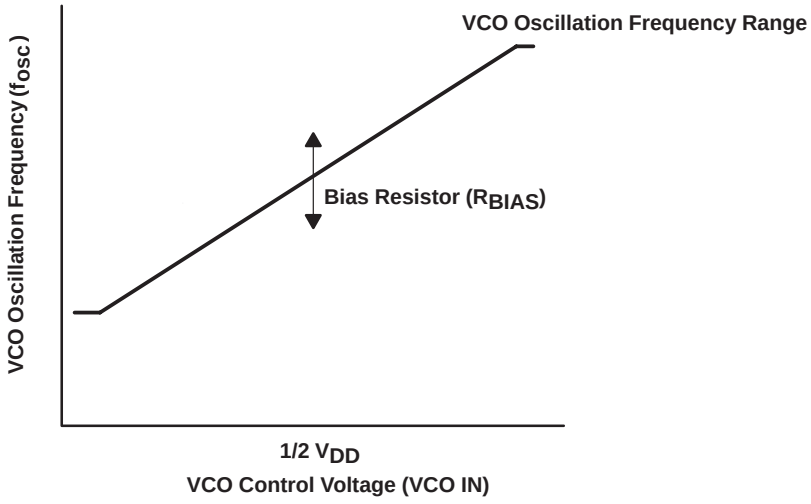


Figure 1. VCO Oscillation Frequency

VCO output frequency 1/2 divider

The TLC2932I SELECT terminal sets the f_{osc} or 1/2 f_{osc} VCO output frequency as shown in Table 1. The 1/2 f_{osc} output should be used for minimum VCO output jitter.

Table 1. VCO Output 1/2 Divider Function

SELECT	VCO OUTPUT
Low	f_{osc}
High	1/2 f_{osc}

VCO inhibit function

The VCO has an externally controlled inhibit function which inhibits the VCO output. A high level on the VCO INHIBIT terminal stops the VCO oscillation and powers down the VCO. The output maintains a low level during the power-down mode, refer to Table 2.

Table 2. VCO Inhibit Function

VCO INHIBIT	VCO OSCILLATOR	VCO OUTPUT	$I_{DD(VCO)}$
Low	Active	Active	Normal
High	Stopped	Low level	Power Down

PFD operation

The PFD is a high-speed, edge-triggered detector with an internal charge pump. The PFD detects the phase difference between two frequency inputs supplied to FIN–A and FIN–B as shown in Figure 2. Nominally the reference is supplied to FIN–A, and the frequency from the external counter output is fed to FIN–B.

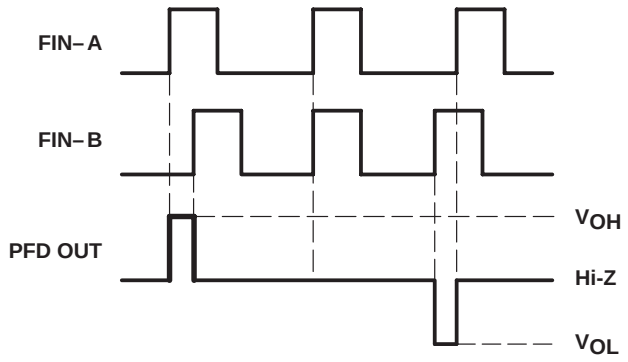


Figure 2. PFD Function Timing Chart

PFD output control

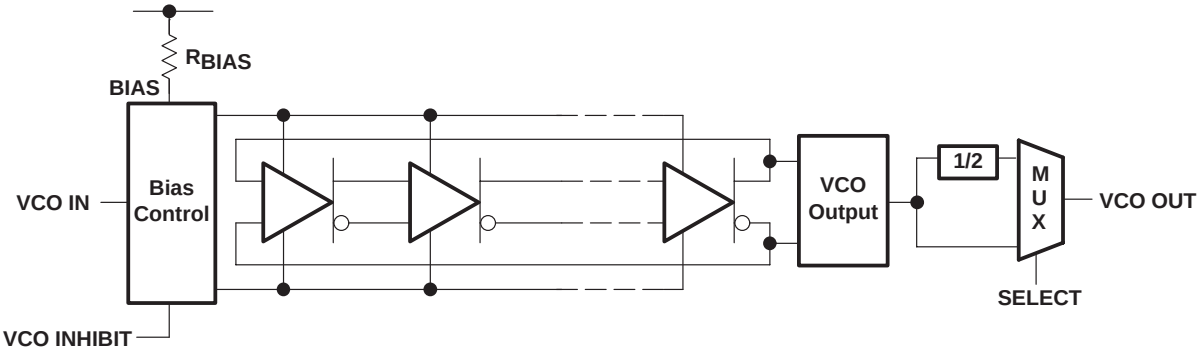
A high level on the PFD INHIBIT terminal places the PFD output in the high-impedance state and the PFD stops phase detection as shown in Table 3. A high level on the PFD INHIBIT terminal also can be used as the power-down mode for the PFD.

Table 3. VCO Output Control Function

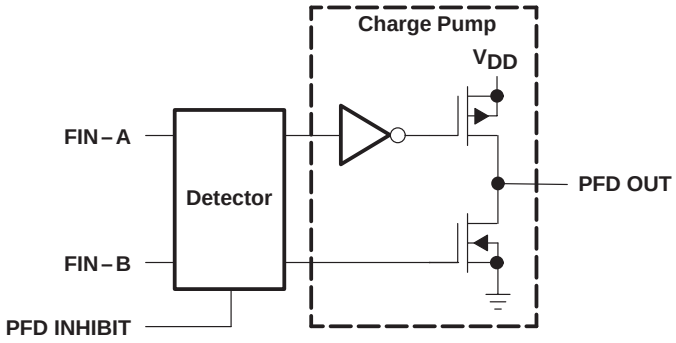
PFD INHIBIT	DETECTION	PFD OUTPUT	$I_{DD(PFD)}$
Low	Active	Active	Normal
High	Stopped	Hi-Z	Power Down

schematics

VCO block schematic



PFD block schematic



absolute maximum ratings†

Supply voltage (each supply), V_{DD} (see Note 1)	7 V
Input voltage range (each input), V_I (see Note 1)	–0.5 V to V_{DD} + 0.5 V
Input current (each input), I_I	±20 mA
Output current (each output), I_O	±20 mA
Continuous total power dissipation, at (or below) T_A = 25°C (see Note 2)	700 mW
Operating free-air temperature range, T_A	–20°C to 75°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network GND.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 5.6 mW/°C.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (each supply, see Note 3)	V_{DD} = 3 V	2.85	3	3.15	V
	V_{DD} = 5 V	4.75	5	5.25	
Input voltage, V_I (inputs except VCO IN)		0		V_{DD}	V
Output current, I_O (each output)		0		±2	mA
VCO control voltage at VCO IN		0.9		V_{DD}	V
Lock frequency (×1 output)	V_{DD} = 3 V	14		21	MHz
	V_{DD} = 5 V	22		50	
Lock frequency (×1/2 output)	V_{DD} = 3 V	7		10.5	MHz
	V_{DD} = 5 V	11		25	
Bias resistor, R_{BIAS}	V_{DD} = 3 V	2.2	3.3	4.3	kΩ
	V_{DD} = 5 V	1.5	2.2	3.3	

NOTE 3: It is recommended that the logic supply terminal (LOGIC V_{DD}) and the VCO supply terminal (VCO V_{DD}) should be at the same voltage and separated from each other.

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 3 V (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.3	V
V_{IT}	Input threshold voltage at SELECT, VCO INHIBIT		0.9	1.5	2.1	V
I_I	Input current at SELECT, VCO INHIBIT	$V_I = V_{DD}$ or GND			±1	µA
$Z_{i(VCO\ IN)}$	Input impedance	VCO IN = 1/2 V_{DD}		10		MΩ
$I_{DD(INH)}$	VCO supply current (inhibit)	See Note 4		0.01	1	µA
$I_{DD(VCO)}$	VCO supply current	See Note 5		5	15	mA

NOTES: 4. Current into VCO V_{DD}, when VCO INHIBIT = V_{DD}, PFD is inhibited.
5. Current into VCO V_{DD}, when VCO IN = 1/2 V_{DD}, R_{BIAS} = 3.3 kΩ, VCO INHIBIT = GND, and PFD is inhibited.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	2.7			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.2	V
I_{OZ}	High-impedance-state output current	PFD INHIBIT = high, $V_I = V_{DD}$ or GND			±1	µA
V_{IH}	High-level input voltage at FIN–A, FIN–B		2.7			V
V_{IL}	Low-level input voltage at FIN–A, FIN–B				0.5	V
V_{IT}	Input threshold voltage at PFD INHIBIT		0.9	1.5	2.1	V
C_i	Input capacitance at FIN–A, FIN–B			5		pF
Z_i	Input impedance at FIN–A, FIN–B			10		MΩ
$I_{DD(Z)}$	High-impedance-state PFD supply current	See Note 6		0.01	1	µA
$I_{DD(PFD)}$	PFD supply current	See Note 7		0.1	1.5	mA

NOTES: 6. Current into LOGIC V_{DD}, when FIN–A, FIN–B = GND, PFD INHIBIT = V_{DD}, no load, and VCO OUT is inhibited.
7. Current into LOGIC V_{DD}, when FIN–A, FIN–B = 1 MHz ($V_{I(PP)}$ = 3 V, rectangular wave), NC = GND, no load, and VCO OUT is inhibited.

operating characteristics over recommended operating free-air temperature range, V_{DD} = 3 V (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Operating oscillation frequency	R_{BIAS} = 3.3 kΩ, VCO IN = 1/2 V_{DD}	15	19	23	MHz
$t_{s(fosc)}$	Time to stable oscillation (see Note 8)	Measured from VCO INHIBIT↓			10	µs
t_r	Rise time	C_L = 15 pF, See Figure 3		7	14	ns
		C_L = 50 pF, See Figure 3		14		
t_f	Fall time	C_L = 15 pF, See Figure 3		6	12	ns
		C_L = 50 pF, See Figure 3		10		
	Duty cycle at VCO OUT	R_{BIAS} = 3.3 kΩ, VCO IN = 1/2 V_{DD},	45%	50%	55%	
$\alpha_{(fosc)}$	Temperature coefficient of oscillation frequency	R_{BIAS} = 3.3 kΩ, VCO IN = 1/2 V_{DD}, T_A = –20°C to 75°C		0.04		%/°C
$k_{SVS(fosc)}$	Supply voltage coefficient of oscillation frequency	R_{BIAS} = 3.3 kΩ, VCO IN = 1.5 V, V_{DD} = 2.85 V to 3.15 V		0.02		%/mV
	Jitter absolute (see Note 9)	R_{BIAS} = 3.3 kΩ		100		ps

NOTES: 8. The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.
9. The low-pass-filter (LPF) circuit is shown in Figure 28 with calculated values listed in Table 7. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully designed PCB with no device socket.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operating frequency		20			MHz
t_{PLZ}	PFD output disable time from low level	See Figures 4 and 5 and Table 4		21	50	ns
t_{PHZ}	PFD output disable time from high level			23	50	
t_{PZL}	PFD output enable time to low level			11	30	ns
t_{PZH}	PFD output enable time to high level			10	30	
t_r	Rise time	C_L = 15 pF, See Figure 4		2.3	10	ns
t_f	Fall time			2.1	10	ns

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.5	V
V_{IT}	Input threshold voltage at SELECT, VCO INHIBIT		1.5	2.5	3.5	V
I_I	Input current at SELECT, VCO INHIBIT	$V_I = V_{DD}$ or GND			±1	μA
$Z_{i(VCO\ IN)}$	Input impedance	VCO IN = 1/2 V_{DD}		10		MΩ
$I_{DD(INH)}$	VCO supply current (inhibit)	See Note 4		0.01	1	μA
$I_{DD(VCO)}$	VCO supply current	See Note 5		15	35	mA

NOTES: 4. Current into VCO V_{DD}, when VCO INHIBIT = V_{DD}, and PFD is inhibited.
5. Current into VCO V_{DD}, when VCO IN = 1/2 V_{DD}, R_{BIAS} = 3.3 kΩ, VCO INHIBIT = GND, and PFD is inhibited.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 2 mA	4.5			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.2	V
I_{OZ}	High-impedance-state output current	PFD INHIBIT = high, $V_I = V_{DD}$ or GND			±1	μA
V_{IH}	High-level input voltage at FIN–A, FIN–B		4.5			V
V_{IL}	Low-level input voltage at FIN–A, FIN–B				1	V
V_{IT}	Input threshold voltage at PFD INHIBIT		1.5	2.5	3.5	V
C_i	Input capacitance at FIN–A, FIN–B			5		pF
Z_i	Input impedance at FIN–A, FIN–B			10		MΩ
$I_{DD(Z)}$	High-impedance-state PFD supply current	See Note 6		0.01	1	μA
$I_{DD(PFD)}$	PFD supply current	See Note 7		0.15	3	mA

NOTES: 6. Current into LOGIC V_{DD}, when FIN–A, FIN–B = GND, PFD INHIBIT = V_{DD}, no load, and VCO OUT is inhibited.
7. Current into LOGIC V_{DD}, when FIN–A, FIN–B = 1 MHz ($V_{I(PP)}$ = 5 V, rectangular wave), PFD INHIBIT = GND, no load, and VCO OUT is inhibited.

operating characteristics over recommended operating free-air temperature range, V_{DD} = 5 V (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Operating oscillation frequency	R_{BIAS} = 2.2 kΩ, VCO IN = 1/2 V_{DD}	30	41	52	MHz
$t_{s(fosc)}$	Time to stable oscillation (see Note 8)	Measured from VCO INHIBIT↓			10	µs
t_r	Rise time	C_L = 15 pF, See Figure 3		5.5	10	ns
		C_L = 50 pF, See Figure 3		8		
t_f	Fall time	C_L = 15 pF, See Figure 3		5	10	ns
		C_L = 50 pF, See Figure 3		6		
	Duty cycle at VCO OUT	R_{BIAS} = 2.2 kΩ, VCO IN = 1/2 V_{DD},	45%	50%	55%	
$\alpha_{(fosc)}$	Temperature coefficient of oscillation frequency	R_{BIAS} = 2.2 kΩ, VCO IN = 1/2 V_{DD}, T_A = –20°C to 75°C		0.06		%/°C
$k_{SVS(fosc)}$	Supply voltage coefficient of oscillation frequency	R_{BIAS} = 2.2 kΩ, VCO IN = 2.5 V, V_{DD} = 4.75 V to 5.25 V		0.006		%/mV
	Jitter absolute (see Note 9)	R_{BIAS} = 2.2 kΩ		100		ps

NOTES: 8: The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.
9. The LPF circuit is shown in Figure 28 with calculated values listed in Table 7. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully designed PCB with no device socket.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operating frequency		40			MHz
t_{PLZ}	PFD output disable time from low level	See Figures 4 and 5 and Table 4		21	40	ns
t_{PHZ}	PFD output disable time from high level			20	40	
t_{PZL}	PFD output enable time to low level			7.3	20	ns
t_{PZH}	PFD output enable time to high level			6.5	20	
t_r	Rise time	C_L = 15 pF, See Figure 4		2.3	10	ns
t_f	Fall time			1.7	10	ns

PARAMETER MEASUREMENT INFORMATION

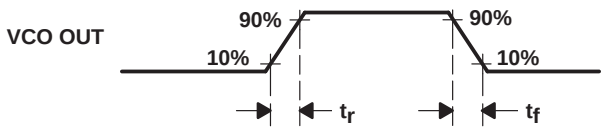
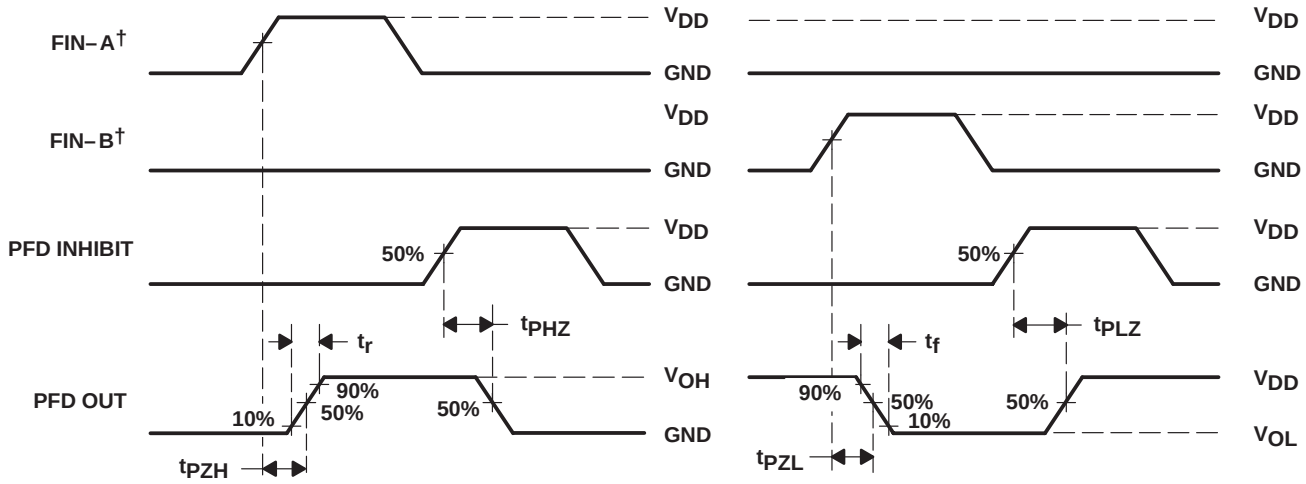


Figure 3. VCO Output Voltage Waveform



(a) OUTPUT PULLDOWN (see Figure 5 and Table 4)

(b) OUTPUT PULLUP (see Figure 5 and Table 4)

† FIN–A and FIN–B are for reference phase only, not for timing.

Figure 4. PFD Output Voltage Waveform

Table 4. PFD Output Test Conditions

PARAMETER	R_L	C_L	S_1	S_2
t_{PZH}	1 kΩ	15 pF	Open	Close
t_{PHZ}				
t_r				
t_{PZL}			Close	Open
t_{PLZ}				
t_f				

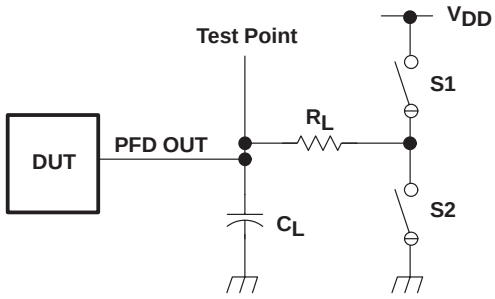


Figure 5. PFD Output Test Conditions

TYPICAL CHARACTERISTICS

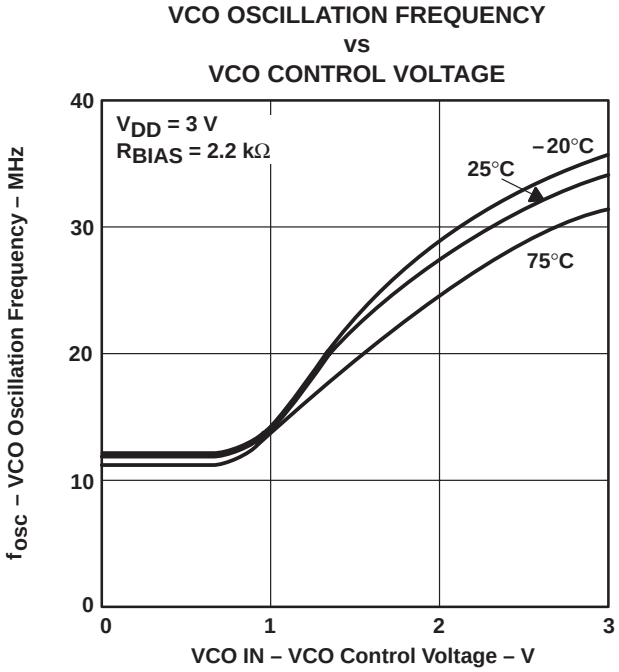


Figure 6

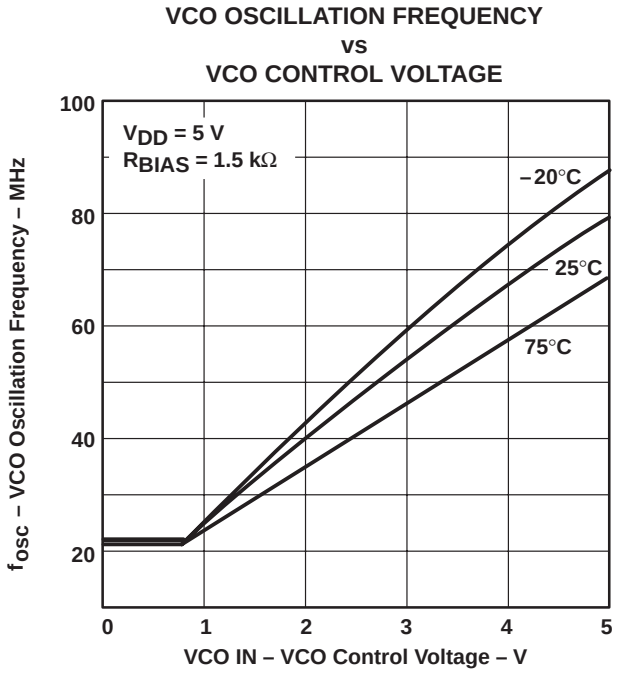


Figure 7

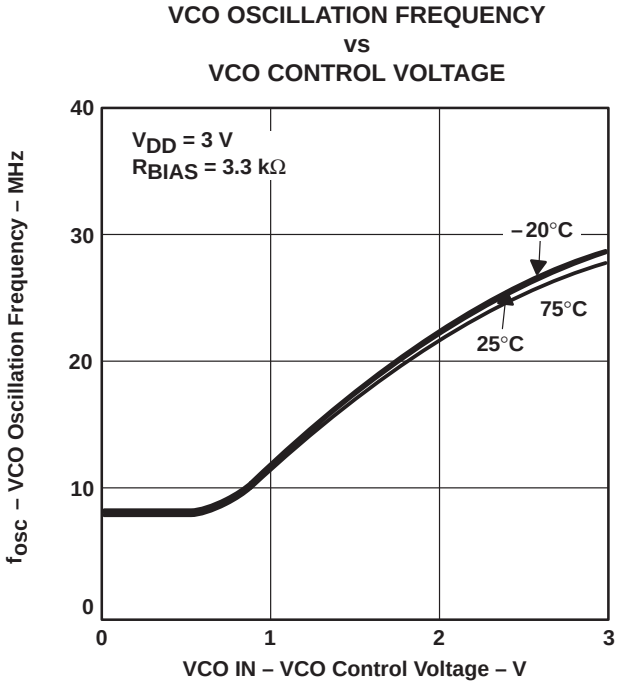


Figure 8

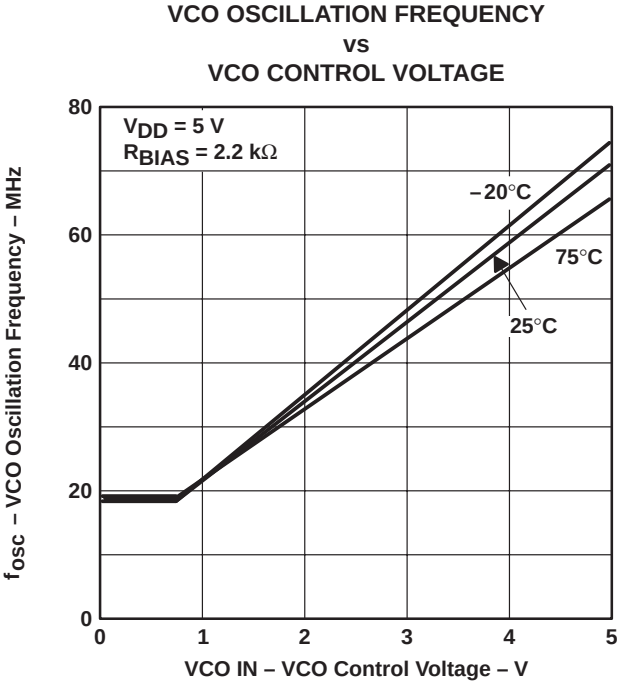


Figure 9

TYPICAL CHARACTERISTICS

VCO OSCILLATION FREQUENCY vs VCO CONTROL VOLTAGE

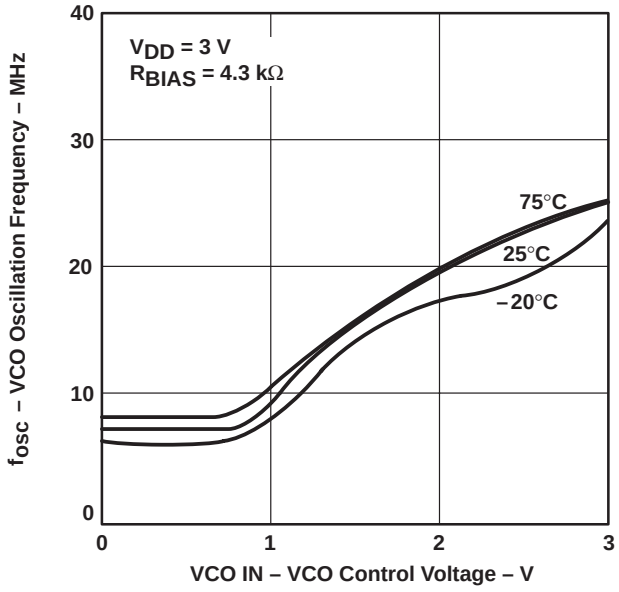


Figure 10

VCO OSCILLATION FREQUENCY vs VCO CONTROL VOLTAGE

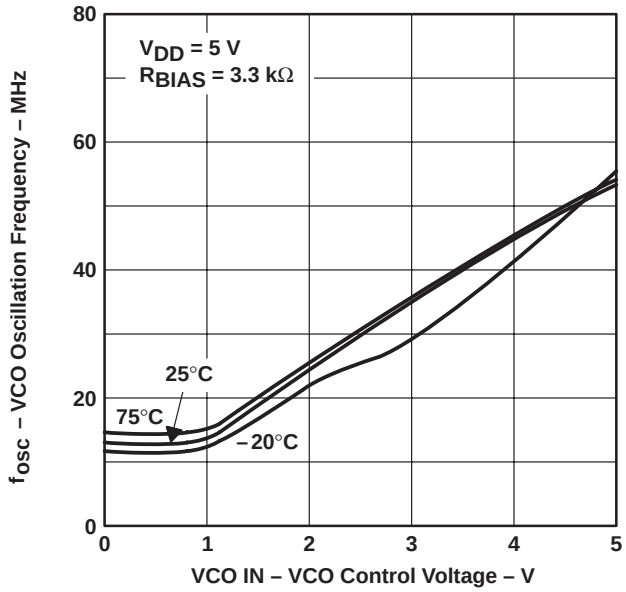


Figure 11

VCO OSCILLATION FREQUENCY vs BIAS RESISTOR

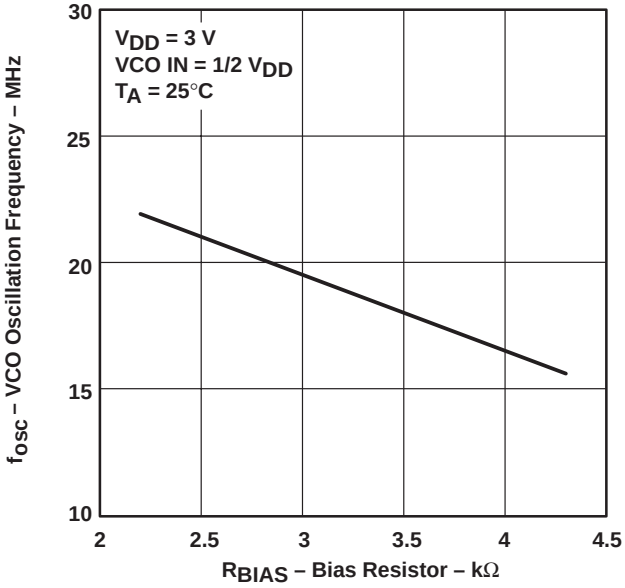


Figure 12

VCO OSCILLATION FREQUENCY vs BIAS RESISTOR

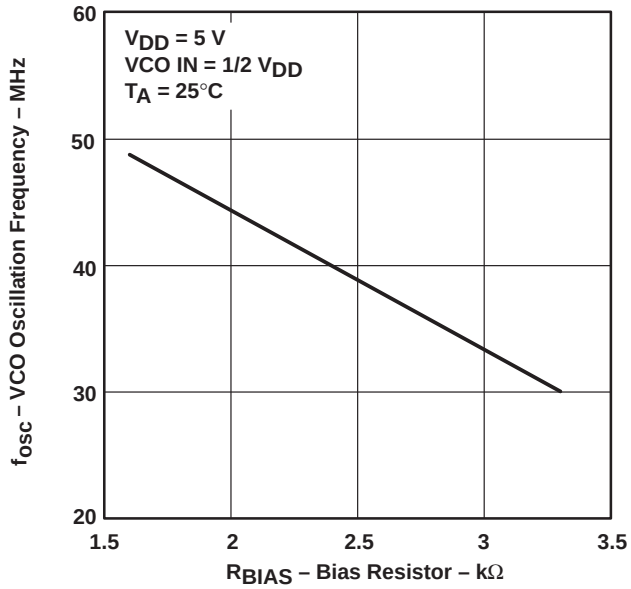


Figure 13

TYPICAL CHARACTERISTICS

TEMPERATURE COEFFICIENT OF OSCILLATION FREQUENCY vs BIAS RESISTOR

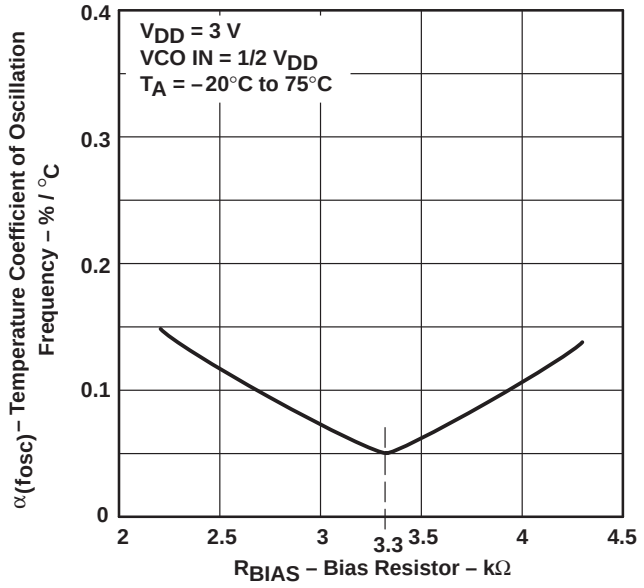


Figure 14

TEMPERATURE COEFFICIENT OF OSCILLATION FREQUENCY vs BIAS RESISTOR

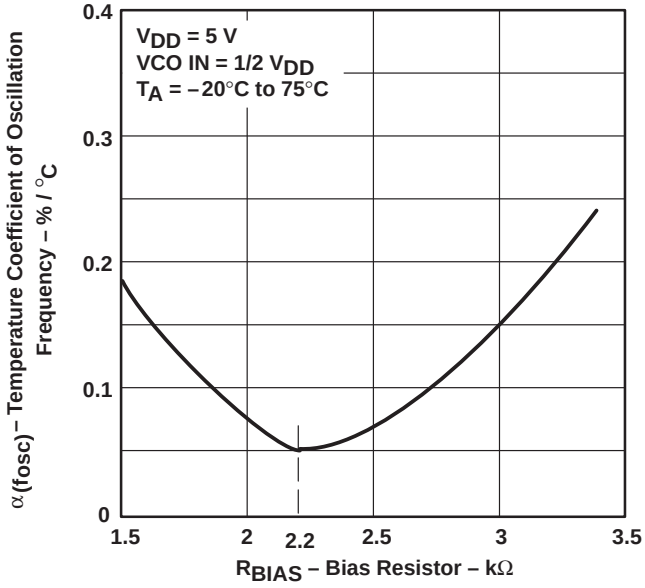


Figure 15

VCO OSCILLATION FREQUENCY vs VCO SUPPLY VOLTAGE

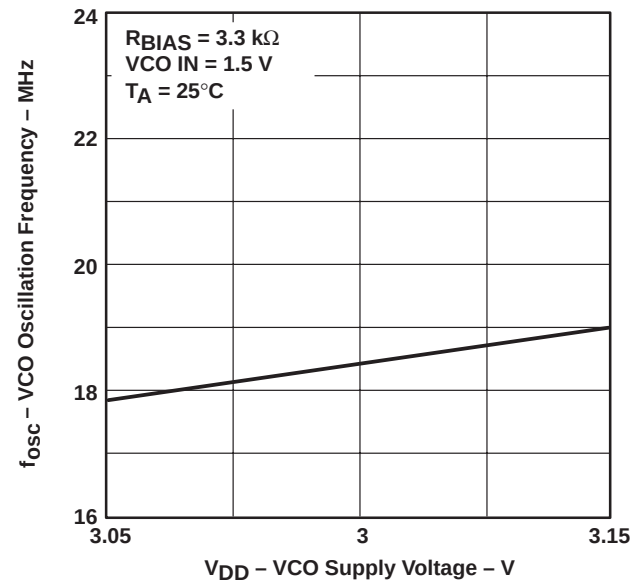


Figure 16

VCO OSCILLATION FREQUENCY vs VCO SUPPLY VOLTAGE

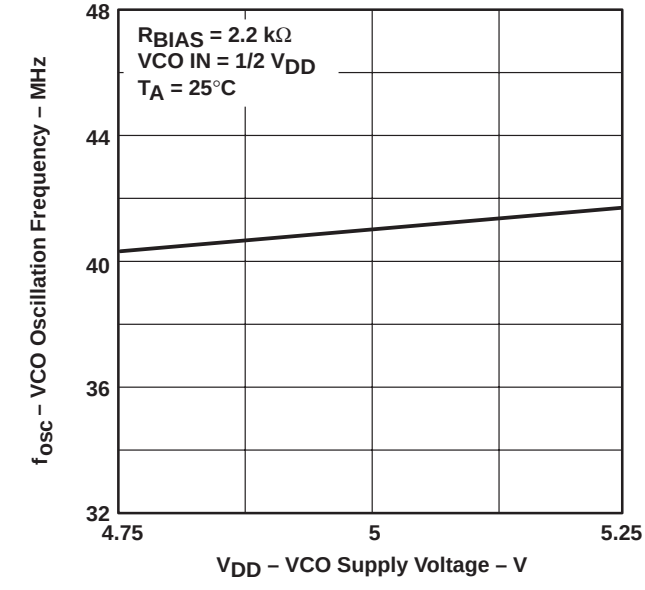


Figure 17

TYPICAL CHARACTERISTICS

SUPPLY VOLTAGE COEFFICIENT OF VCO OSCILLATION FREQUENCY vs BIAS RESISTOR

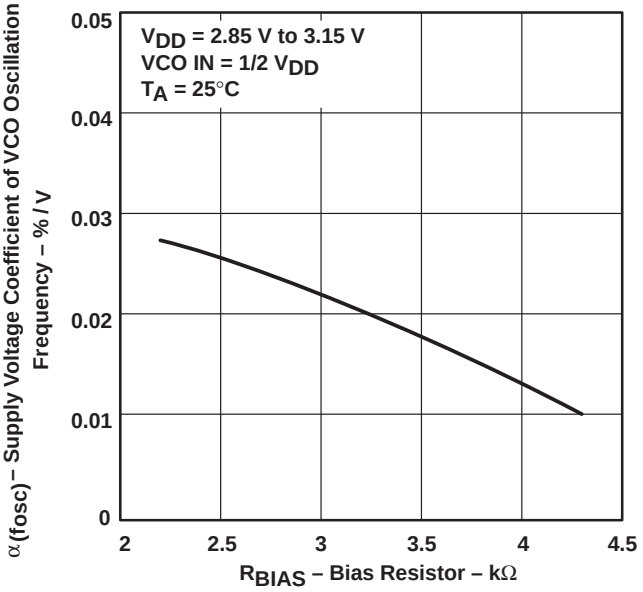


Figure 18

SUPPLY VOLTAGE COEFFICIENT OF VCO OSCILLATION FREQUENCY vs BIAS RESISTOR

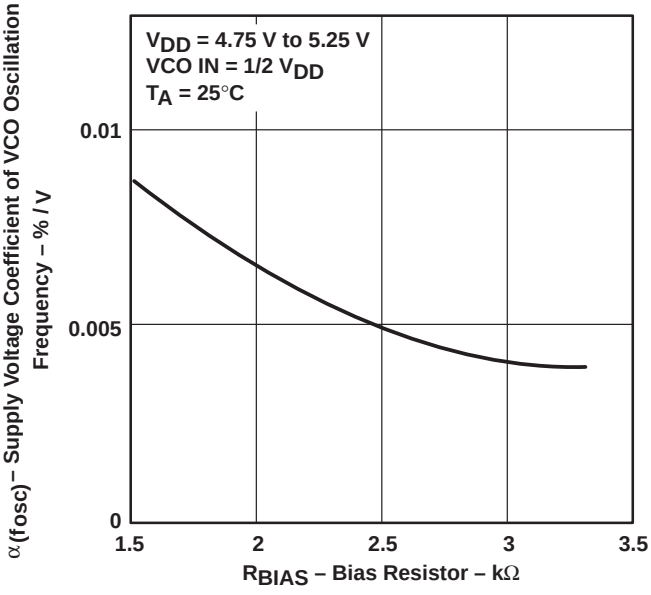


Figure 19

RECOMMENDED LOCK FREQUENCY (×1 OUTPUT) vs BIAS RESISTOR

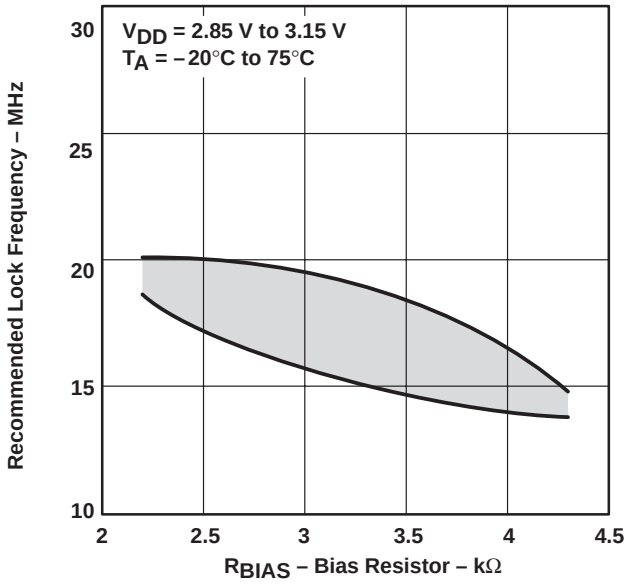


Figure 20

RECOMMENDED LOCK FREQUENCY (×1 OUTPUT) vs BIAS RESISTOR

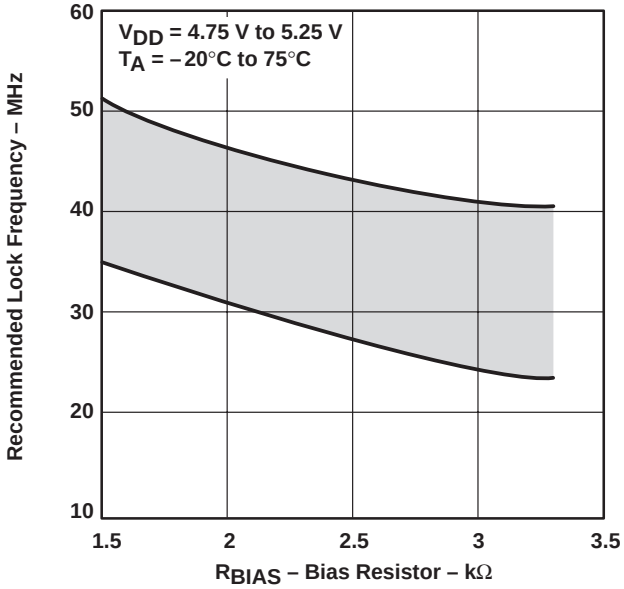


Figure 21

APPLICATION INFORMATION

RECOMMENDED LOCK FREQUENCY (×1/2 OUTPUT) vs BIAS RESISTOR

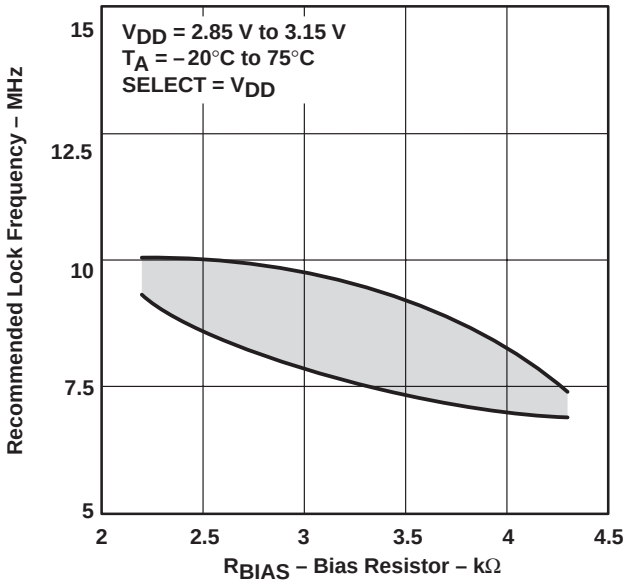


Figure 22

RECOMMENDED LOCK FREQUENCY (×1/2 OUTPUT) vs BIAS RESISTOR

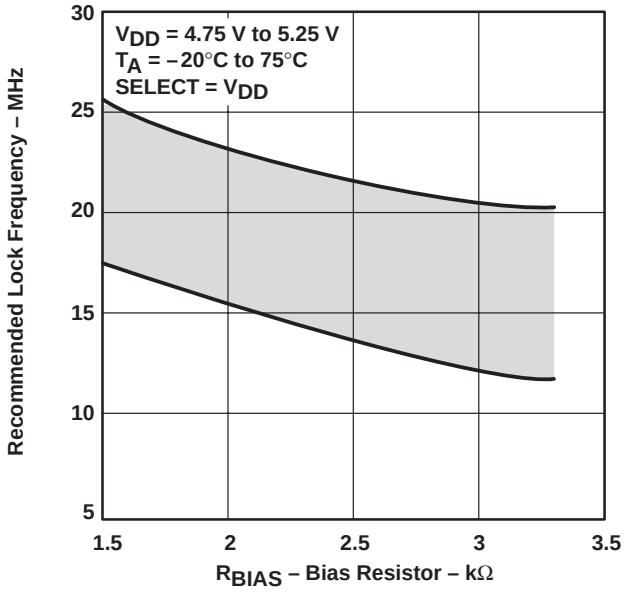


Figure 23

APPLICATION INFORMATION

gain of VCO and PFD

Figure 24 is a block diagram of the PLL. The countdown N value depends on the input frequency and the desired VCO output frequency according to the system application requirements. The K_p and K_V values are obtained from the operating characteristics of the device as shown in Figure 24. K_p is defined from the phase detector V_{OL} and V_{OH} specifications and the equation shown in Figure 24(b). K_V is defined from Figures 8, 9, 10, and 11 as shown in Figure 24(c).

The parameters for the block diagram with the units are as follows:

K_V : VCO gain (rad/s/V)
K_p : PFD gain (V/rad)
K_f : LPF gain (V/V)
K_N : count down divider gain (1/N)

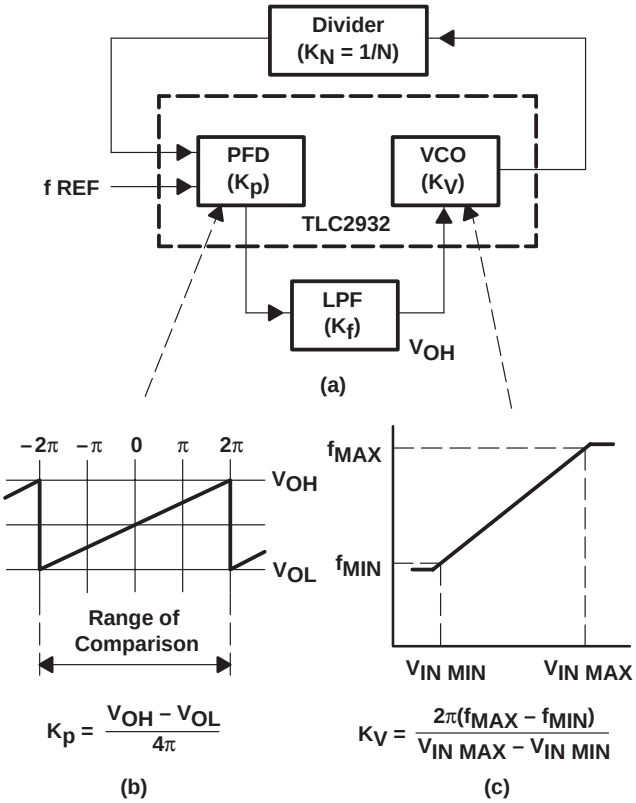


Figure 24. Example of a PLL Block Diagram

external counter

When a large N counter is required by the application, there is a possibility that the PLL response becomes slow due to the counter response delay time. In the case of a high frequency application, the counter delay time should be accounted for in the overall PLL design.

R_{BIAS}

The external bias resistor sets the VCO center frequency with 1/2 V_{DD} applied to the VCO IN terminal. However, for optimum temperature performance, a resistor value of 3.3 kΩ with a 3-V supply and a resistor value of 2.5 kΩ for a 5-V supply is recommended. For the most accurate results, a metal-film resistor is the better choice but a carbon-compositiion resistor can be used with excellent results also. A 0.22 μF capacitor should be connected from the BIAS terminal to ground as close to the device terminals as possible.

hold-in range

From the technical literature, the maximum hold-in range for an input frequency step for the three types of filter configurations shown in Figure 25 is as follows:

$$\Delta\omega_H \simeq 0.8 \left(K_p\right) \left(K_V\right) \left(K_f\,(\infty)\right)$$

Where

$K_f\,(\infty)$ = the filter transfer function value at $\omega = \infty$

APPLICATION INFORMATION

low-pass-filter (LPF) configurations

Many excellent references are available that include detailed design information about LPFs and should be consulted for additional information. Lag-lead filters or active filters are often used. Examples of LPFs are shown in Figure 25. When the active filter of Figure 25(c) is used, the reference should be applied to FIN-B because of the amplifier inversion. Also, in practical filter implementations, C2 is used as additional filtering at the VCO input. The value of C2 should be equal to or less than one tenth the value of C1.

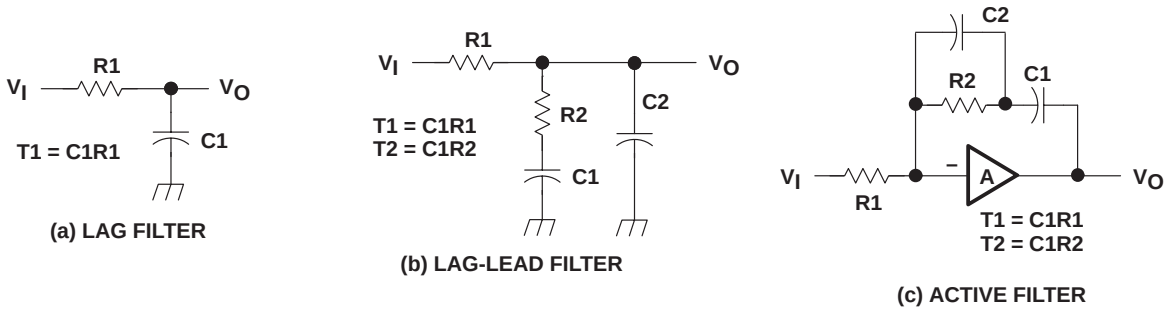


Figure 25. LPF Examples for PLL

the passive filter

The transfer function for the lag-lead filter shown in Figure 25(b) is;

$$\frac{V_O}{V_{IN}} = \frac{1 + s \cdot T2}{1 + s \cdot (T1 + T2)}$$

Where

$$T1 = R1 \cdot C1 \text{ and } T2 = R2 \cdot C1$$

Using this filter makes the closed loop PLL system a second-order type 1 system. The response curves of this system to a unit step are shown in Figure 26.

the active filter

When using the active integrator shown in Figure 25(c), the phase detector inputs must be reversed since the integrator adds an additional inversion. Therefore, the input reference frequency should be applied to the FIN-B terminal and the output of the VCO divider should be applied to the input reference terminal, FIN-A.

The transfer function for the active filter shown in Figure 25(c) is:

$$F(s) = \frac{1 + s \cdot R2 \cdot C1}{s \cdot R1 \cdot C1}$$

Using this filter makes the closed loop PLL system a second-order type 2 system. The response curves of this system to a unit step are shown in Figure 27.

basic design example

The following design example presupposes that the input reference frequency and the required frequency of the VCO are within the respective ranges of the device.

APPLICATION INFORMATION

basic design example (continued)

Assume the loop has to have a 100 μs settling time (t_s) with a countdown N = 8. Using the Type 1, second order response curves of Figure 26, a value of 4.5 radians is selected for $\omega_n t_s$ with a damping factor of 0.7. This selection gives a good combination for settling time, accuracy, and loop gain margin. The initial parameters are summarized in Table 5. The loop constants, K_V and K_p, are calculated from the data sheet specifications and Table 6 shows these values.

The natural loop frequency is calculated as follows:

Since

$$\omega_n t_s = 4.5$$

Then

$$\omega_n = \frac{4.5}{100\ \mu s} = 45\ \text{k-radians/sec}$$

Table 5. Design Parameters

PARAMETER	SYMBOL	VALUE	UNITS
Division factor	N	8	
Lockup time	t	100	μs
Radian value to selected lockup time	$\omega_n t$	4.5	rad
Damping factor	ζ	0.7	

Table 6. Device Specifications

PARAMETER	SYMBOL	VALUE	UNITS
VCO gain	K_V	76.6	Mrad/V/s
f_{MAX}		70	MHz
f_{MIN}		20	MHz
$V_{IN\ MAX}$		5	V
$V_{IN\ MIN}$		0.9	V
PFD gain	K_p	0.342357	V/rad

Table 7. Calculated Values

PARAMETER	SYMBOL	VALUE	UNITS
Natural angular frequency	ω_n	45000	rad/sec
$K = (K_V \bullet K_p)/N$		3.277	Mrad/sec
Lag-lead filter Calculated value Nearest standard value	R1	15870 16000	Ω
Calculated value Nearest standard value	R2	308 300	Ω
Selected value	C1	0.1	μF

APPLICATION INFORMATION

Using the low-pass filter in Figure 25(b) and divider ratio N, the transfer function for phase and frequency are shown in equations 1 and 2. Note that the transfer function for phase differs from the transfer function for frequency by only the divider value N. The difference arises from the fact that the feedback for phase is unity while the feedback for frequency is 1/N.

Hence, transfer function of Figure 24 (a) for phase is

$$\frac{\Phi 2(s)}{\Phi 1(s)} = \frac{K_p \cdot K_V}{N \cdot (T1 + T2)} \left[\frac{1 + s \cdot T2}{s^2 + s \left[1 + \frac{K_p \cdot K_V \cdot T2}{N \cdot (T1 + T2)} \right] + \frac{K_p \cdot K_V}{N \cdot (T1 + T2)}} \right] \quad (1)$$

and the transfer function for frequency is

$$\frac{F_{OUT(s)}}{F_{REF(s)}} = \frac{K_p \cdot K_V}{(T1 + T2)} \left[\frac{1 + s \cdot T2}{s^2 + s \cdot \left[1 + \frac{K_p \cdot K_V \cdot T2}{N \cdot (T1 + T2)} \right] + \frac{K_p \cdot K_V}{N \cdot (T1 + T2)}} \right] \quad (2)$$

The standard two-pole denominator is $D = s^2 + 2\,\zeta\,\omega_n\,s + \omega_n^2$ and comparing the coefficients of the denominator of equation 1 and 2 with the standard two-pole denominator gives the following results.

$$\omega_n = \sqrt{\frac{K_p \cdot K_V}{N \cdot (T1 + T2)}}$$

Solving for T1 + T2

$$T1 + T2 = \frac{K_p \cdot K_V}{N \cdot \omega_n^2} \quad (3)$$

and by using this value for T1 + T2 in equation 3 the damping factor is

$$\zeta = \frac{\omega_n}{2} \cdot \left(T2 + \frac{N}{K_p \cdot K_V} \right)$$

solving for T2

$$T2 = \frac{2\,\zeta}{\omega} - \frac{N}{K_p \cdot K_V}$$

then by substituting for T2 in equation 3

$$T1 = \frac{K_V \cdot K_p}{N \cdot \omega_n^2} - \frac{2\,\zeta}{\omega_n} + \frac{N}{K_p \cdot K_V}$$

APPLICATION INFORMATION

From the circuit constants and the initial design parameters then

$$R2 = \left[\frac{2\,\zeta}{\omega_n} - \frac{N}{K_p \cdot K_V}\right]\frac{1}{C1}$$

$$R1 = \left[\frac{K_p \cdot K_v}{\omega_n{}^2 \cdot N} - \frac{2\,\zeta}{\omega_n} + \frac{N}{K_p \cdot K_V}\right]\frac{1}{C1}$$

The capacitor, C1, is usually chosen between 1 μF and 0.1 μF to allow for reasonable resistor values and physical capacitor size. In this example, C1 is chosen to be 0.1 μF and the corresponding R1 and R2 calculated values are listed in Table 7.

APPLICATION INFORMATION

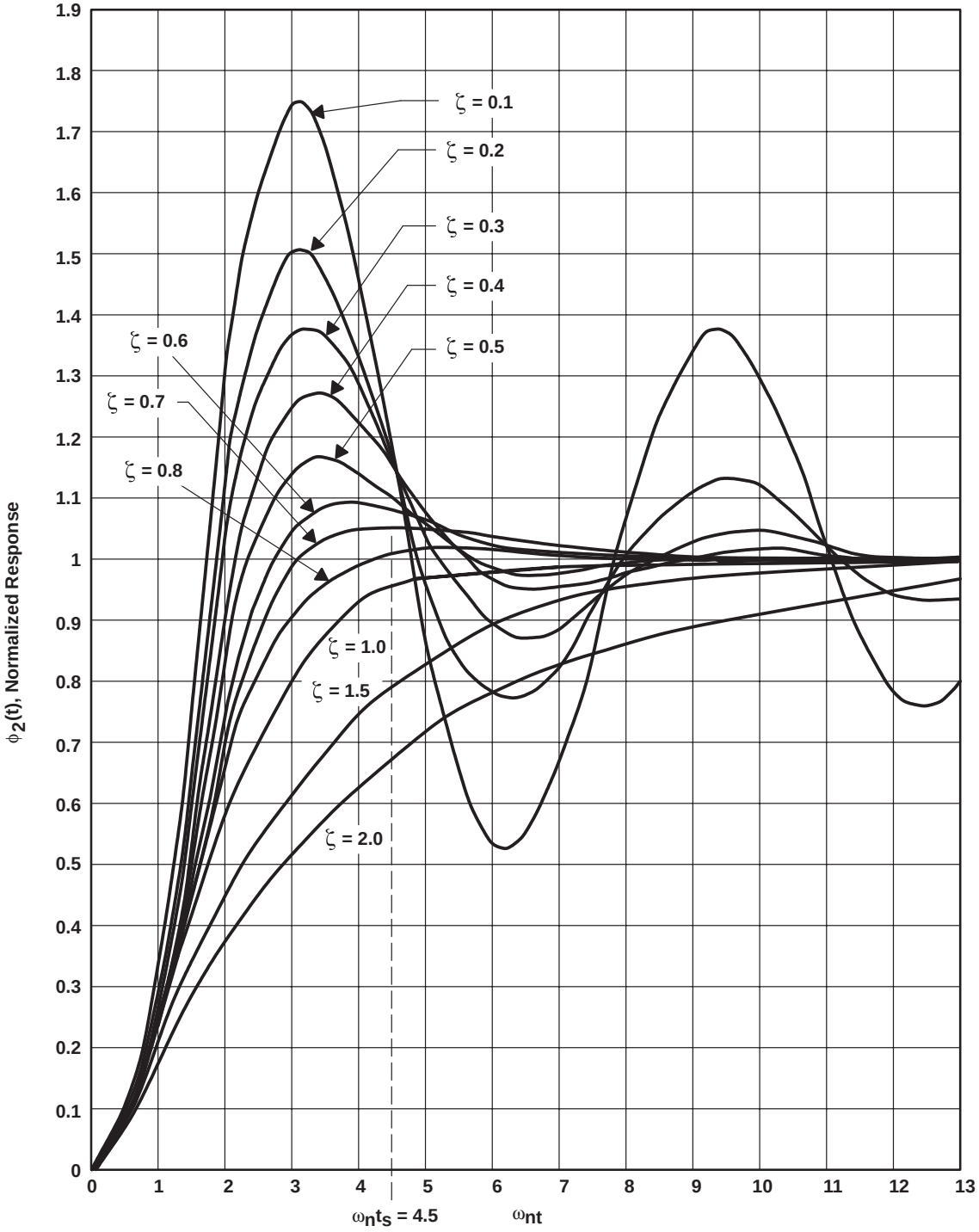


Figure 26. Type 1 Second-Order Step Response

APPLICATION INFORMATION

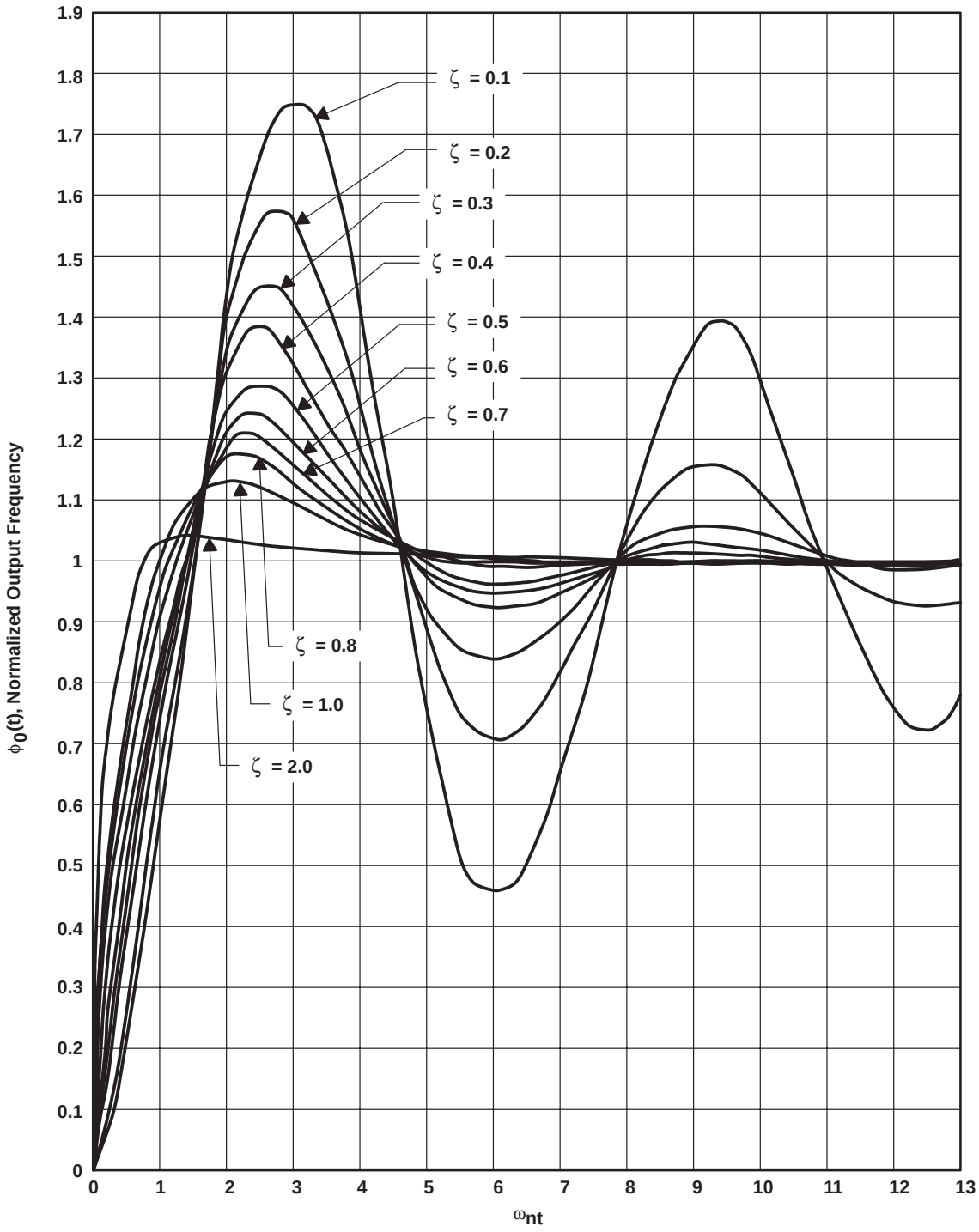


Figure 27. Type 2 Second-Order Step Response

APPLICATION INFORMATION

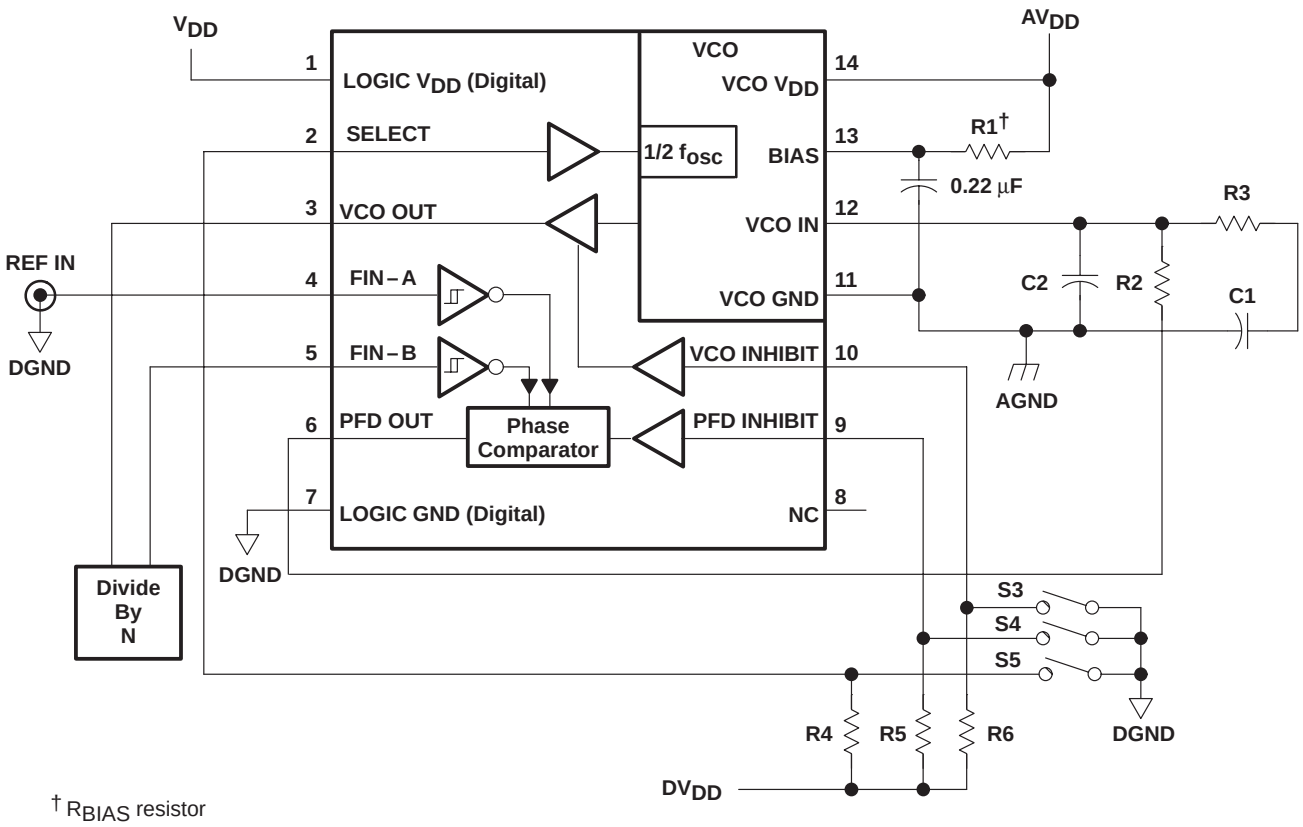


Figure 28. Evaluation and Operation Schematic

PCB layout considerations

The TLC2932I contains a high frequency analog oscillator; therefore, very careful breadboarding and printed-circuit-board (PCB) layout is required for evaluation.

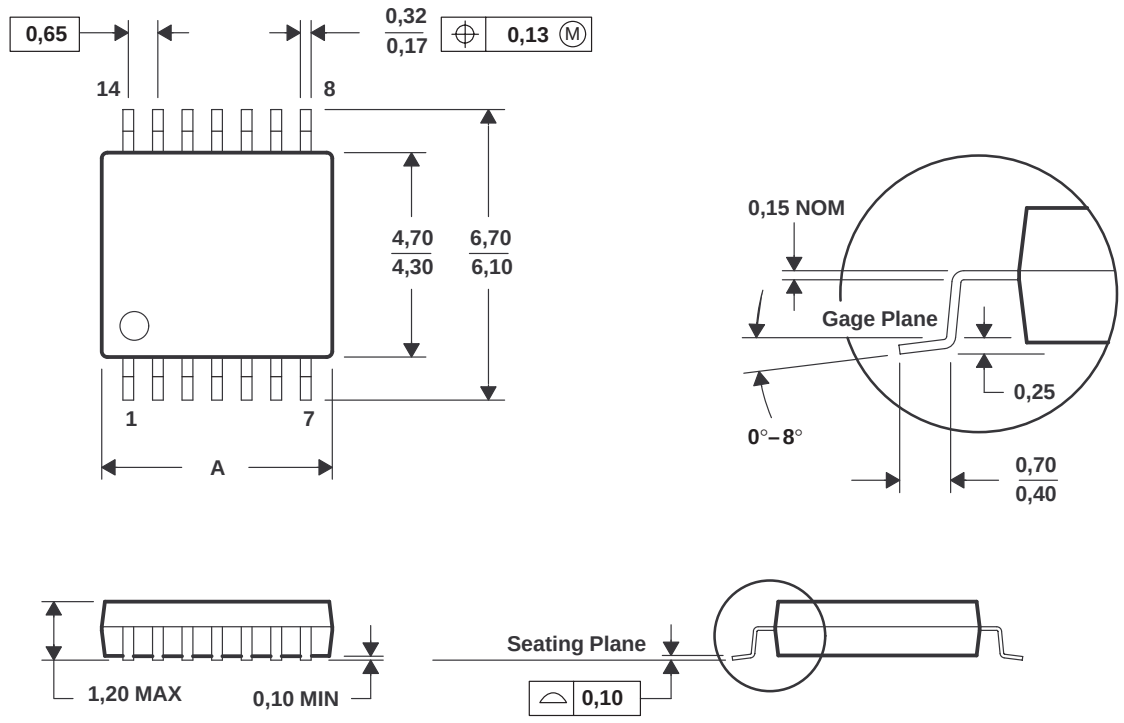
The following design recommendations benefit the TLC2932I user:

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or RF PCB techniques should be used throughout the evaluation and production process.
- Wide ground leads or a ground plane should be used on the PCB layouts to minimize parasitic inductance and resistance. The ground plane is the better choice for noise reduction.
- LOGIC V_{DD} and VCO V_{DD} should be separate PCB traces and connected to the best filtered supply point available in the system to minimize supply cross-coupling.
- VCO V_{DD} to GND and LOGIC V_{DD} to GND should be decoupled with a 0.1-µF capacitor placed as close as possible to the appropriate device terminals.
- The no-connection (NC) terminal on the package should be connected to GND.

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,30	5,30	5,30	6,80	8,10	10,00
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/B 10/94

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.