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TLV1544EVM Evaluation Module for the TLV1544 10-Bit ADC

User's Guide

Mixed-Signal Products

TLV1544EVM Evaluation Module for the TLV1544 10-Bit ADC
User's Guide

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About This Manual

This User's Guide describes the characteristics, operation, and use of the TLV1544EVM Evaluation Moduale for the TLV1544 10-Bit Analog-to-Digital Converter (ADC).

How to Use This Manual

This document contains the following chapters:

❑ Chapter 1 Overview

❑ Chapter 2 Physical Description

❑ Chapter 3 Circuit Description

❑ Chapter 4 Operation

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Chapter 1

Overview

This chapter gives a general overview of the TLV1544EVM Evaluation Module (EVM), and describes some of the factors that must be considered in using the module.

1.1 Purpose

The TLV1544EVM Evaluation Module (EVM) provides a platform for evaluating the TLV1544 10-Bit Analog-to-Digital Converter (ADC) under various signal, reference, and supply conditions.

1.2 EVM Basic Function

There are four analog inputs to the TLV1544EVM, three of these are available for external inputs through BNC connectors. The internal analog input consists of an operational amplifier with a potentiometer for observing simple dc measurements.

The reference voltage can be selected by using the on-board jumpers and the switch, SW1. The reference input can be the supply voltage, an onboard generated absolute reference or an externally generated reference voltage.

An SN74HC244 buffers the digital I/O signals to the output header and test connector.

1.3 Power Requirements

The EVM operates properly over a balanced input voltage range of ±10 volts maximum to ±7 volts minimum. The power supply and externally applied reference voltage should be supplied to the EVM through shielded twisted-pair wire for best performance. This type of power cabling minimizes any stray or transient pickup from the higher frequency digital circuitry.

Voltage Limits

Exceeding the ±10-volt maximum can damage EVM components. Under voltage may cause improper operation of the bipolar op amp channel A1, depending on the application. The positive supply can be lowered to 6 volts and the EVM will maintain the 5-V supply.

1.4 I/O CLK Requirements

The I/O CLK can go up to 10 MHz for most of the voltage range when fast I/O is possible. The maximum I/O CLK is limited to 2.8 MHz for a supply voltage range from 2.7 V. Table 1–1 lists the maximum I/O CLK frequencies for all different supply voltage ranges. This also depends on input source impedance. For example, I/O CLK speed faster than 2.39 MHz is achievable if the input source impedance is less than 1 kΩ.

Table 1–1. Maximum I/O CLK Frequency

V_{CC}	Maximum Input Resistance (Max)	Source Impedance	I/O CLK
2.7 V	5 K	1 kΩ	2.39 MHz
		100 Ω	2.81 MHz
4.5 V	1 K	1 kΩ	7.18 MHz
		100 Ω	10 MHz

1.5 I/O Interface Connector Provisions

The connector interface is versatile allowing different connection arrangements depending on the user selected interface. A 12-position single inline male connector, J5, is hard wired to the input/output signals of the TLV1544 through the SN74HC244. J6 is a dual row, 24 position header, so any dual row 100 mil center connector can be used up to 24 pins. J5 and J6 are separated by a jumper row that allows J6 to be user configured for the appropriate external interface. The schematic shows the signal arrangement for J5. Either J5 or J6 can easily be used with the corresponding male ribbon cable plug.

The two rows of plated-through holes, designated as JPA shorting jumpers, allow the on board signals to connect externally in a variety of user defined selections. Using these jumpers, the TLV1544EVM I/O signals can be conveniently connected to an existing hardware (DSP EVMs, microprocessor EVM, micro-controller EVMs, etc.) by appropriate jumper placement.

When using J6, the clock lines should have a ground line on either side in the ribbon cable to minimize cross-talk. If possible every other conductor in the ribbon cable should be grounded.

1.6 Timing and Signal Requirements

The signal timing necessary is shown in Chapter 4, Figures 4–2 through 4–5 for the various processor options.

1.7 TLV1544EVM Operational Procedure

Some signal setup or software is required for the TLV1544EVM. The TLV1544 data sheet provides the timing requirements and the application report (literature number SLAA025) supplies an example of software using the TMS320C50 DSP. Once the input requirements are completed, the operating procedures for the TLV1544EVM are as follows.

❏ Connect ±7 to ±10 V and ground to the V+, V–, and GND terminals of J1. These terminals are marked on the bottom side of the EVM. Ensure that JP6 is shorted to establish zero volts as the operating point for the bipolar operational amplifier.

SW1 can select 5-V V_{CC} or 2.7-V V_{CC}. The 2.7 volt operation should be used only with a host interface that provides 3-V nominal or less input signals to the EVM.

❏ For most DSP operation, JP5 is open and for most microprocessor operation, JP5 is shorted. The INV CLK terminal condition is controlled by this jumper and therefore, the clocking edge that is used for data input.

❏ The analog input that is connected to the TLV1544 is determined by software and any input can be selected for testing. The four channels are configured as follows:

Analog Input
A0   Potentiometer with operational amplifier buffer
A1   ±10 V supply voltage follower
A2   Uses external input unbuffered
A3   Uses external input unbuffered

Normally, through the software, the full scale, mid scale, and zero scale could be checked first. Then A0 can be selected and checked with the potentiometer adjustment.

❏ Connect the appropriate voltage reference as follows. Place a short on JP2, position 2 toward TP11 designation, to connect REF– terminal to ground.

JP1 Designation Reference Voltage
1   On board absolute reference (4.086 V at 5 V V_{CC} or 2.5 V at 2.7 V V_{CC})
3   V_{CC}

When SW1 is changed the onboard absolute reference is automatically changed to the proper value for the V_{CC} selected.

❏ The I/O signals can be monitored at J7.

❏ The additional analog inputs can be used for application of external signals. Select the desired analog input for board checkout. Ensure that JP3, JP4, and JP6 are shorted with a jumper connection.

Chapter 2

Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

2.1 PCB Layout

The EVM is constructed on a 4-layer, 3-inch x 5.25-inch, 0.062-inch thick PCB using FR-4 material. Figures 2–1 through 2–5 show the individual layers.

Figure 2–1. PCB Layout
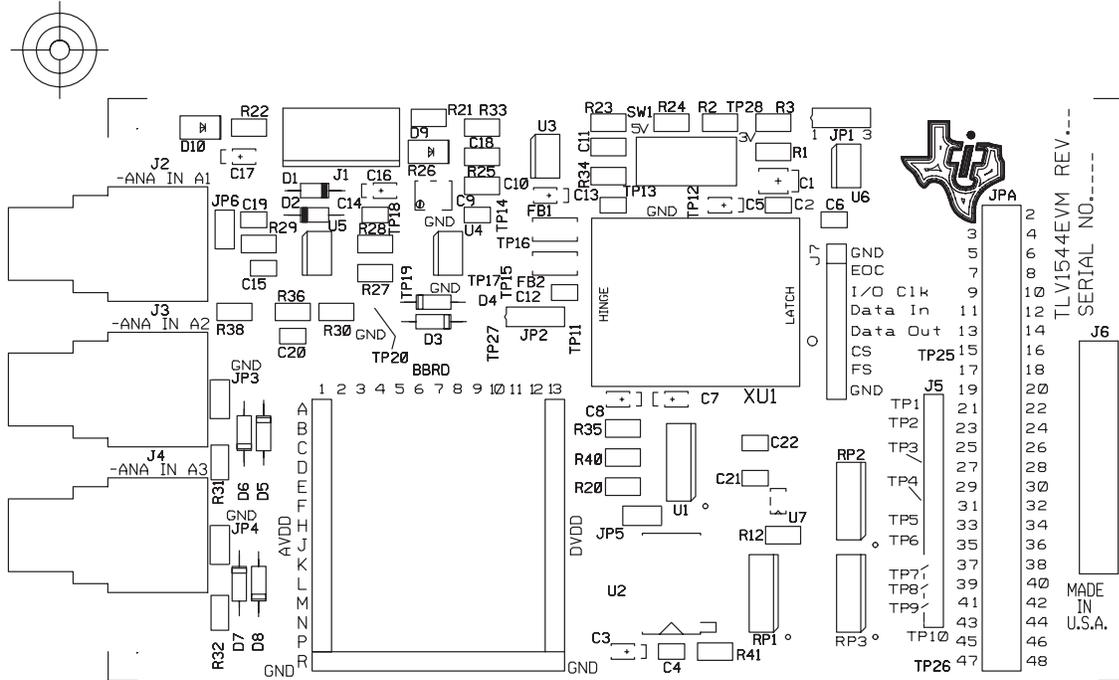
SILKSCREEN TOP

Figure 2–2. PCB Layout

LAYER 1 – COMPONENT SIDE
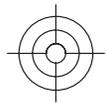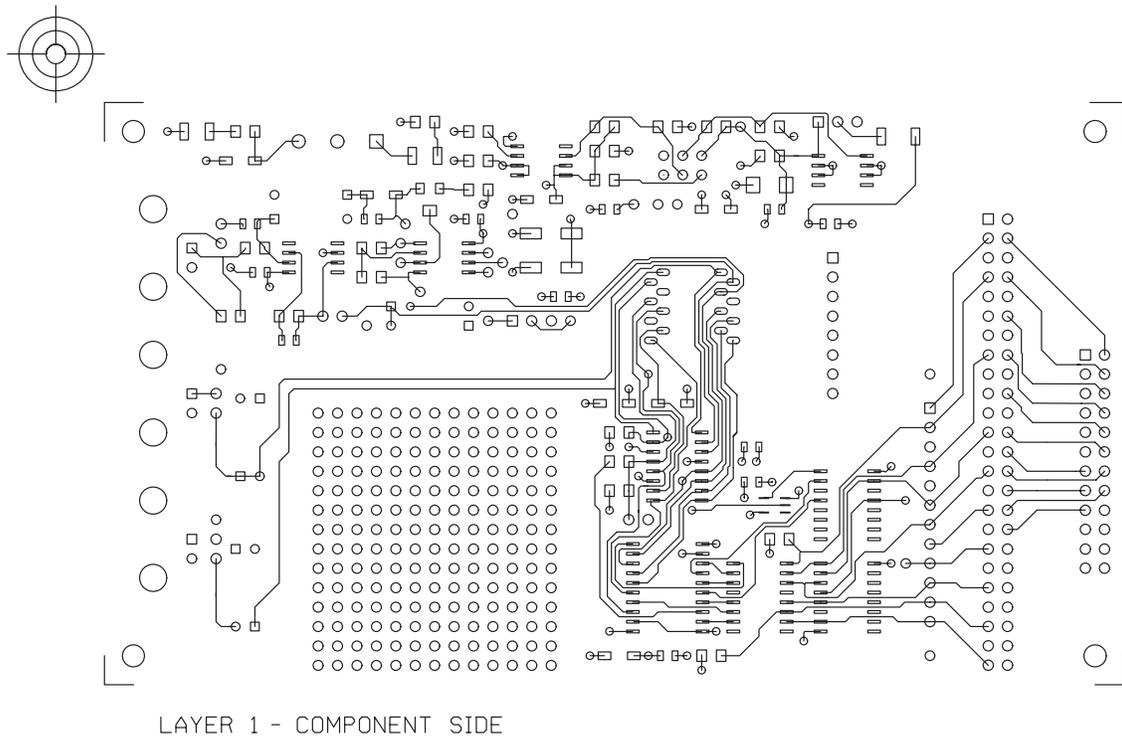
Figure 2–3. PCB Layout
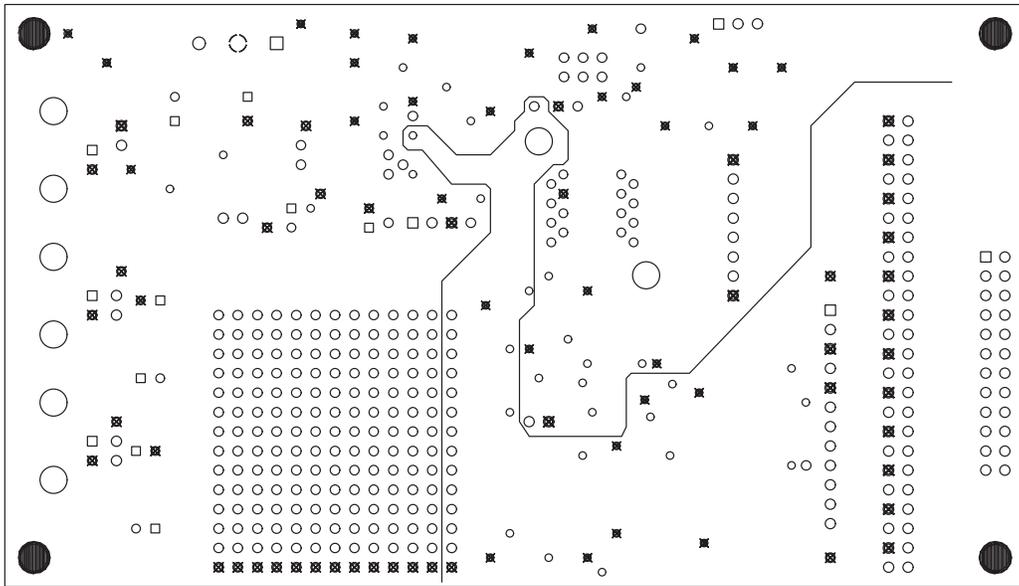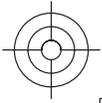
LAYER 2 - GROUND PLANE

Physical Description

Figure 2–4. PCB Layout
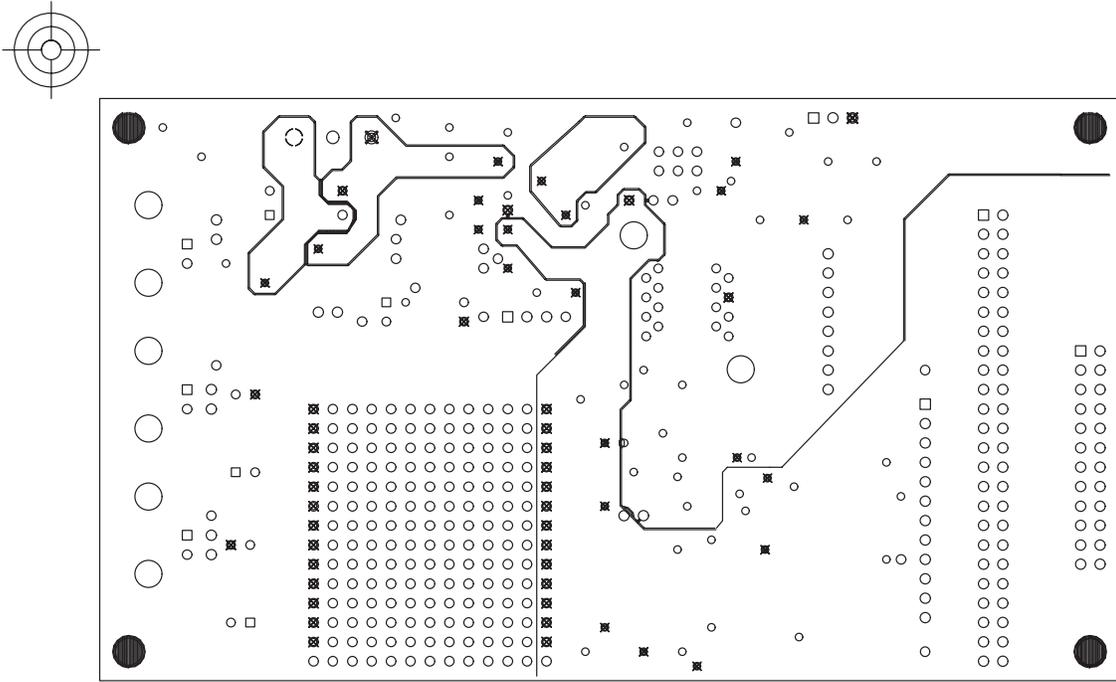
LAYER 3 - POWER PLANE
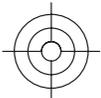
Figure 2–5. PCB Layout
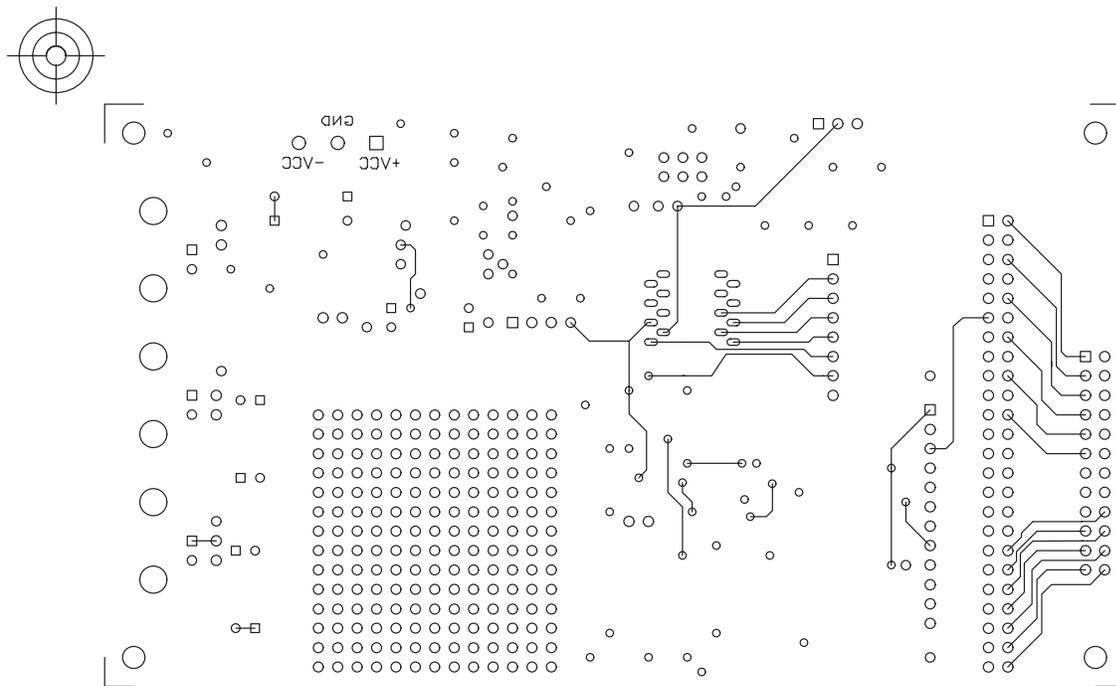
LAYER 4 - SOLDER SIDE
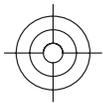
2.2 Component List

Table 2–1 lists the components used in constructing the EVM.

Table 2–1. Component List

Reference Designator	Description	Manufacturer	Part Number
R1	178 Ω, 1%, 1206 SMD	Panasonic	ERJ-8ENF1780
R21, R22	1 kΩ, 1%, 1206 SMD	Panasonic	ERJ-8ENF1001
R2	6.34 kΩ, 1%, 1206 SMD	Panasonic	ERJ-8ENF6341
R3, R25, R27, R28, R35, R36, R38	10 kΩ, 1%, 1206 SMD	Panasonic	ERJ-8ENF1002
RP1	100-Ω resistor array	Bourns	4816P-T01-101
RP2	33-Ω resistor array	Bourns	4816P-T01-330
R12, R20, R35, R41	20 kΩ, 1%, 1206 SMD	Panasonic	ERJ-8ENF2002
R40	2 kΩ, 1%, 1206 SMD	Panasonic	ERJ-8ENF2001
R23	562 kΩ, 1%, 1206 SMD	Panasonic	ERJ-8ENF5623
R24	169 kKΩ, 1%, 1206 SMD	Panasonic	ERJ-8ENF1693
R29	100 Ω, 1%, 1206 SMD	Panasonic	ERJ-8ENF1000
R26	10-kΩ potentiometer, multi-turn, SMD	Bourns	3224W-1-103D
R30, R31, R32	0 Ω, 1206 SMD	Bourns	CR1206-J-OOOE
R34	357 kΩ, 1%, 1206 SMD	Panasonic	ERJ-8ENF3573
C1	10 μF, 16V	Panasonic	ECST1CX106R
C3, C5, C10, C16, C17	4.7 μF	Panasonic	ECST1CY475R
C2, C12, C13, C22	0.01 μF, 0805	Panasonic	ECUV1H103KBG
C4, C6, C9, C14, C15, C21	0.1 μF, 0805 SMD	Panasonic	ECUV1C104KBX
C7, C8	1 μF, 16 V	Pansonic	ECST1CC105R
C11, C18	0.1 μF, 1206 SMD	Panasonic	ECUV1H104KBW
C19, C20	100 pF, 0805	Panasonic	ECUV1H101JCG
D1, D2	IN4148	Phillips DO-35 Pkg.	1N4148
D3–D8, D11	Schottky	SGS	BAT81
D9, D10	Red LED	Dialite	AND5RA
FB1, FB2	Ferrite bead	Fair-Rite	27-44-44447
J1	3-terminal connector	Lumberg	KRMZ3 (ALL'D P/N 742-0083)
J2–J4	BNC, panel mount	Amp	227121-7
J5	12-pin connector, single row, male	Berg	68705-212
J6	24-hole, 100 mil centers, double row, header		
J7	Connector, 8 pin, male	Berg	68705-208
JP1, JP2	3 required	Berg	68000-236
JP3–JP6	2 required	Berg	68000-236

Table 2–1. Component List (Continued)

| Reference Designator	Description	Manufacturer	Part Number
U1	10-bit serial out ADC	TI	TLV1544CD
U2	Octal buffer and line driver	TI	SN74AHC244DW
U3	Low dropout adjustable regulator	TI	TPS7101QD
U4	5-V rail-to-rail op amp	TI	TLV2432AID
U5	Bipolar op amp	TI	TLE2027ACD
U6	Adjustable voltage reference	TI	TL1431CD
U7	Micro inverter	TI	SN74AHC1G04DBVR
XU1	(For reference only) Socket, IC, 16 pin, Not on board, To use, U1 must be removed	Yamaichi	IC51-0162-1042
SW1	DPDT switch, board mount	Augat/Alcoswitch	STS220PC
TP25, TP26	Test point, 0.025 sq.	Samtec	TWS-101-07-5-5

Circuit Description

This chapter contains the EVM schematic diagram and discusses the various functions on the EVM.

3.1 Schematic Diagram

Figure 3–1 shows the schematic diagram for the EVM. The following paragraphs describe the EVM circuits.

Figure 3–1. EVM Schematic Diagram
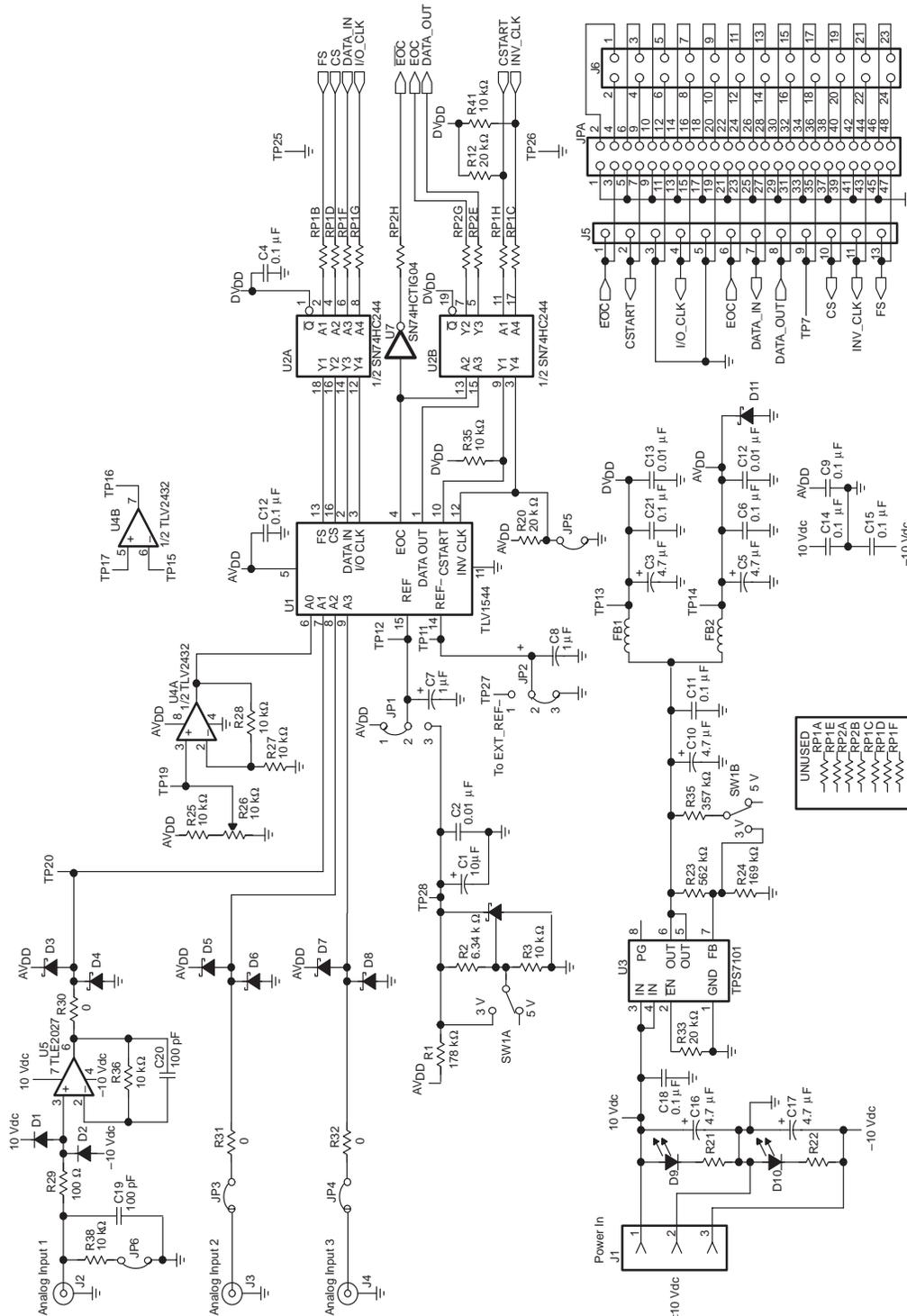
3.2 Circuit Function

The following paragraphs describe the function of individual circuits.

3.2.1 Inputs

The ADC has four analog inputs; A0, A1, A2, and A3. The EVM connects to these inputs as follows:

❑ A0. One op amp of a single-supply TLV2232 dual op amp drives the A0 input with an onboard-adjustable dc voltage.

❑ A1. A TLE2027 dual-supply op amp connected as a voltage follower drives the A1 input. The op amp receives external input through J2.

❑ A2, A3. These are available for user-defined inputs. The external inputs to these channels are applied through J3 and J4 respectively.

### 3.2.2 A0 – Voltage Variable Analog Input (Potentiometer)

Potentiometer R26 controls the dc voltage to ADC input A0 through one section of the TLV2432, a non-inverting gain of 2 amplifier. Resistors R25 and R26 form a voltage divider from AV_{CC} with the R26 wiper to the noninverting input. Adjusting R26, the 10-kΩ potentiometer, through the adjustment range changes the op amp input voltage from 0 to $V_{CC/2}$. Since the amplifier has a gain of two, the input voltage to A0 ranges from 0 to 5 volts. Measurements made with this analog channel are ratiometric, since the input voltage varies with changes in the supply voltage. The full scale output of the TLV2432 will be approximately 10 counts below the nominal full scale digital output of all ones if the analog V_{CC} is used as the reference voltage input.

3.2.3 A1 – External Input With Voltage Follower Buffer

Input A1 of the TLC1544 input port connects through U5, a TLE2027 voltage follower. J2 provides the external input for the voltage follower. With an input power supply of ±7 volts or greater, this amplifier configuration produces an extremely linear signal from 0 to 5 volts because this signal range does not approach the nonlinearity close to the supply rails. Input A1 lead is protected from voltages above and below the ADC supply by diodes, D3 and D4. Diodes D1 and D2 with resistor R29 protect the TLE2027 noninverting input from voltages at J2 in excess of the supply rails. R30 is set to 0 ohms but can be changed to provide additional current limit protection.

When using this amplifier with direct coupling, the noninverting input signal should have a quiescent value of $V_{CC/2}$ for proper midpoint biasing for the ADC. If capacitor coupling is used between the source and J2, then JP6 should be removed so that the Vcc/2 reference can be established with an equal value 10-k resistor divider or the divider can be buffered with the unused op amp in U4. Figure 3-2 shows this technique.

Figure 3–2. Generation of AVdd/2 with Buffer for Channel A1 Input Biasing with JP6 Removed
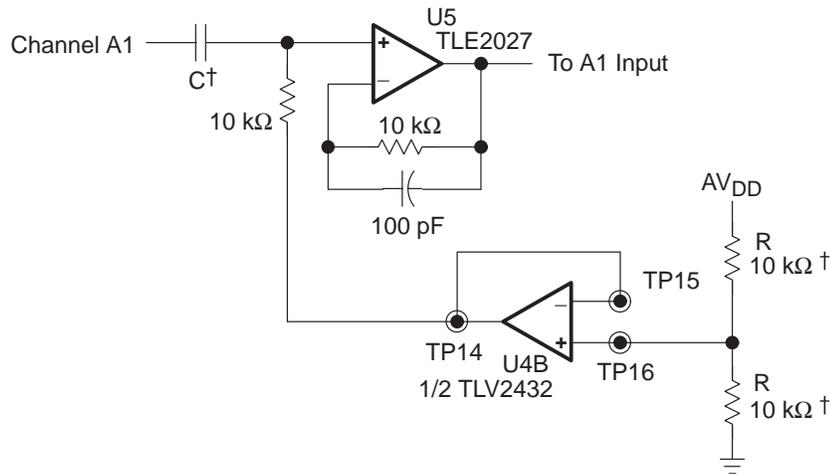
† These components are not part of the TLV1544 EVM and must be added externally.

3.2.4 Unbuffered Analog Inputs

The BNC connectors, J3 and J4, provide two unbuffered inputs which go to the edge of the breadboard area. These inputs are protected by diodes D5, D6, D7, and D8 to prevent damage from moderate voltages in excess of the supply rails. Jumpers JP3 and JP4 are used to directly connect these inputs to ADC inputs A2 and A3 . Other signal conditioning can be placed in the breadboard area and those outputs connected to A2 or A3 through an open JP3 or JP4. R31 and R32 are set to 0 ohms but can be changed to provide additional current limit protection.

When using the unbuffered inputs, the driving source impedance must be low for proper slew rate of the input signal. The source must provide enough current into 50 pF to arrive at final voltage value within the device specified sampling time. Also, if the source noise is not below the 10 bit level, this noise could cause jitter in the least significant bit.

3.2.5 Power

A balanced voltage input of ±10 volts maximum (±7 volts minimum) and ground should be supplied to the EVM through connector J1 with the plus supply voltage applied to J1-1, the minus supply to J1-3, and ground to J1-2. The op amp, U5, uses the bipolar supplies. The rest of the EVM uses regulated 5 volts from the positive supply through the TPS7101 low dropout regulator. Switch SW1 can switch the output voltage of the regulator from nominally 5-volt to 2.7-volt operation. The regulator output voltage is divided into the digital supply (DVdd) and analog supply (AVdd) through ferrite beads and individual filter capacitors. The 5-volt or 2.7-volt output powers U1, U2, U4, U6 and U7.

The ±7 to ±10 volts is applied to the TLE2027 while only the plus supply voltage is also applied to the TPS7101 low-dropout regulator. The TPS7101 regulates

for a 5-volt or 2.7-volt V_{CC} such that ADC evaluation can be done at either VDD through switch SW1. SW1 adjusts the TL1431 voltage reference to accommodate the change in V_{CC}; SW1 also changes the SN74HC244 V_{CC} to 2.7 volts. The micro inverter can be used to accommodate inversion for software interrupt processing.

3.2.6 Voltage Reference Generation

Two jumpers control the reference voltage for the ADC. JP1 supplies a 5-volt reference in position 3 with a 5 volt supply and 2.7 volt reference with the 2.7 volt supply selected. (pins 2 and 3 shorted together). A nominal 4.086-volt reference is obtained with the jumper in position 1 (pins 1 and 2 shorted together or a 2.5 volt reference with the 2.7 volt supply). This absolute reference is generated by the TL1431 through the resistor divider of R2 and R3. R2 is shorted when the ADC is operated at 2.7 volt Vcc giving the voltage reference of 2.5 volts. JP2 should be connected to ground in position 1 toward the TP11 designator (shorting pins 2 and 3 together). The jumper can be changed to position 2 toward the TP27 designator (pins 1 and 2 shorted together), which removes the ground connection such that a positive voltage can be applied to TP27 as the REF– input. Care must be exercised when using this reference method to provide a clean, noise free voltage at the REF– terminal of the ADC. The voltage differential between REF+ and REF – should always be equal to or greater than 2.5 volts for proper operation within the TLV1544 specified limits.

Ratiometric measurements are the measurements made on signals that vary with the supply voltage. If an input signal voltage is used that varies proportionately with the supply voltage, such as the potentiometer input to A0, the signal is a ratio of the absolute value of the supply. Therefore, connecting the reference to the supply provides a nominal conversion result independent of supply voltage variations.

3.2.7 Test Connector

Test connector J7 provides a convenient point for measuring device signal.The device test points as listed in Table 3–1.

Table 3–1. Test Connector J7

J7 Pin	TLV1544 pin	Function
1	GND	GND
2	4	EOC
3	3	I/O CLK
4	2	DATA IN
5	1	DATA OUT
6	16	$\overline{\text{CS}}$
7	13	FS
8	GND	GND

3.2.8 Jumper Arrangement

The EVM evaluation can begin with the following shorting plug arrangement.

❑ JP1 connected to AVdd (2 and 3 shorted)
❑ JP2 connected to ground (2 and 3 shorted)
❑ JP3 shorted
❑ JP4 shorted
❑ JP5 open
❑ JP6 shorted

Operation

This chapter describes the basic operation of the EVM with a host DSP or processor.

Topic   **Page**

4.1 TLV1544 Overview

The following paragraphs describe the TLV1544 10-bit ADC.

4.1.1 Description

The TLV1544 is a CMOS 10-bit switched-capacitor successive approximation ADC. Figure 4–1 shows the functional block diagram for the device.

The device has a chip-select ($\overline{CS}$), input-output clock (I/O CLK), data input (DATA IN) and serial data output (DATA OUT). An additional frame sync (FS) input initiates data transfer when using a DSP and connects to the DSP serial port FSX pin. $\overline{INV}$ $\overline{CLK}$ state allows DSP or SPI™ and QSPI™ timing.

The $\overline{CSTART}$ is used for delayed sampling.

Figure 4–1. Functional Block Diagram
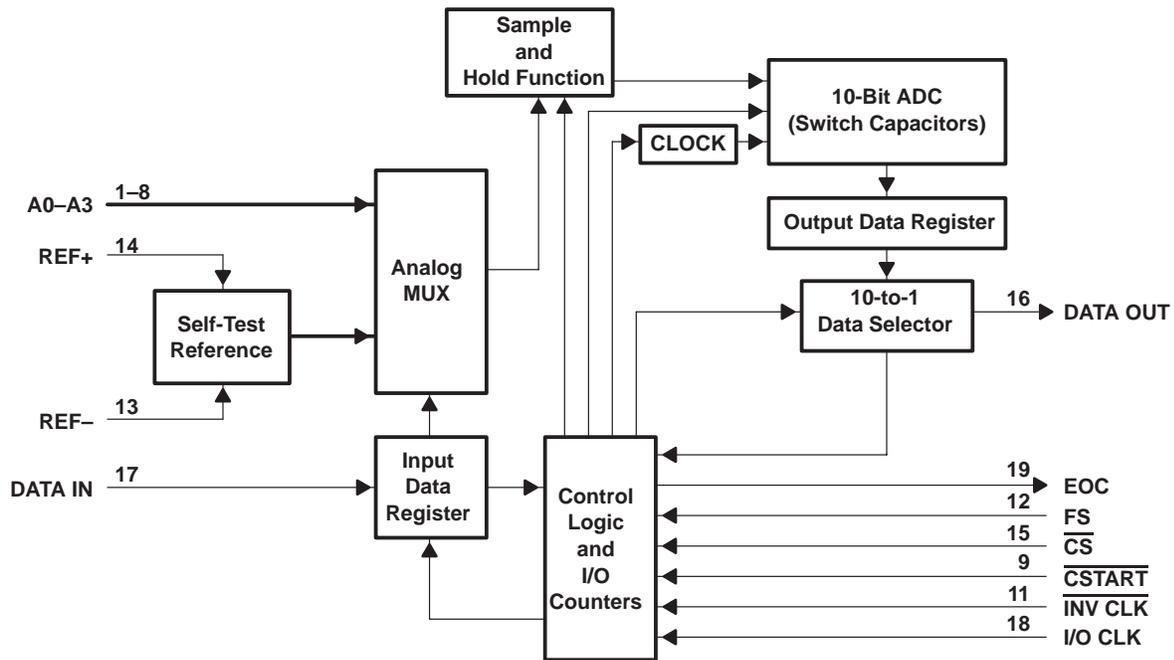
Terminals shown are for the DB package.

4.1.2 Timing Diagrams

Figures 4–2 through 4–5 show the system signal timing diagrams. These timing diagrams show the four basic signal I/O signal sets required for microprocessor and DSP timing.

Figure 4–2. Microprocessor Interface Timing (Normal Sample Mode, $\overline{INV\ CLK}$ = High)
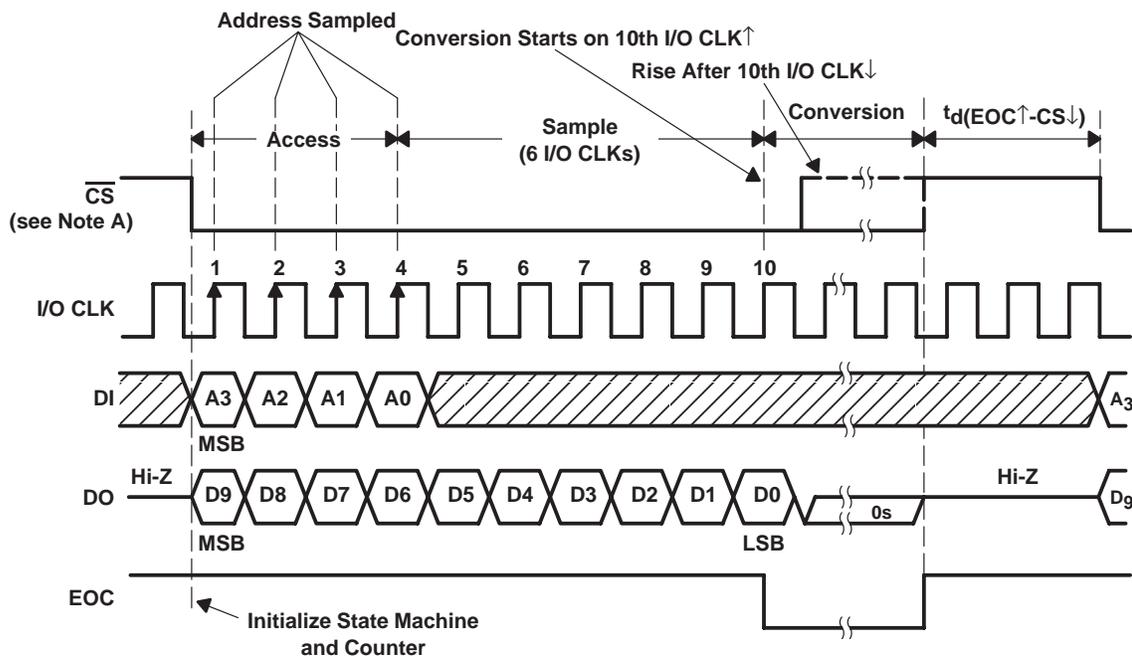
NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{CS}$ setup time elapses.

Figure 4–3. Microprocessor Interface Timing (Normal Sample Mode, $\overline{INV\ CLK}$ = Low)
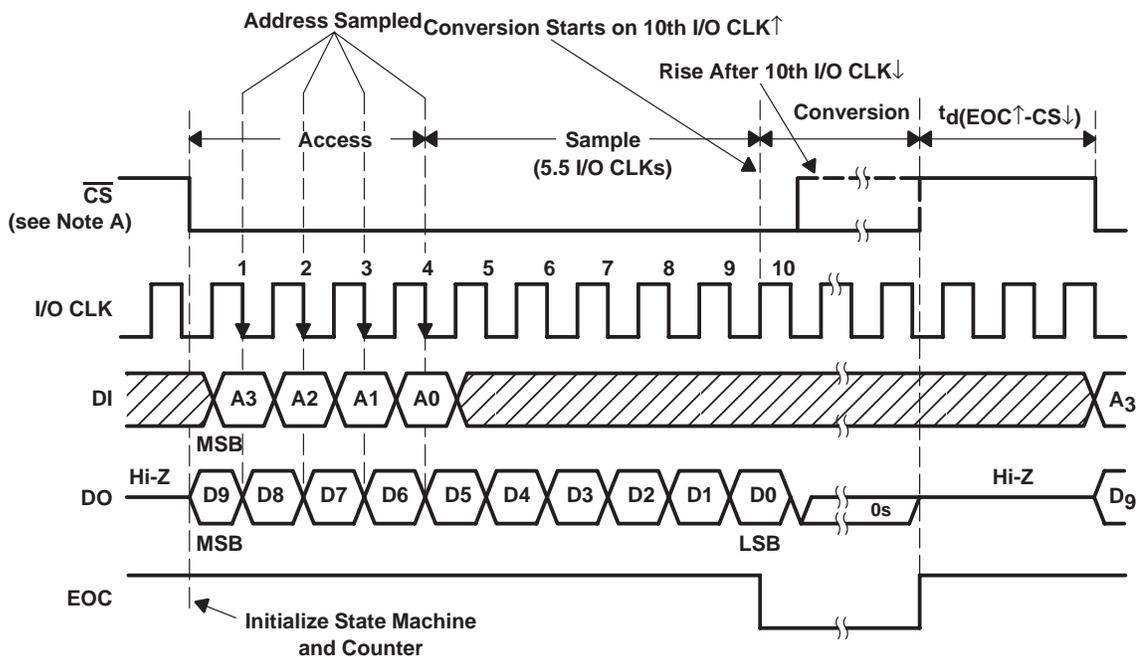
NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{CS}$ setup time has elapsed.

Figure 4–4. DSP Interface Timing (16-Clock Transfer, Normal Sample Mode, $\overline{INV\ CLK}$ = High)


NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{CS}$ setup time elapses.

Operation

Figure 4–5. DSP Interface Timing (16-Clock Transfer, Normal Sample Mode, $\overline{INV\ CLK}$ = Low)
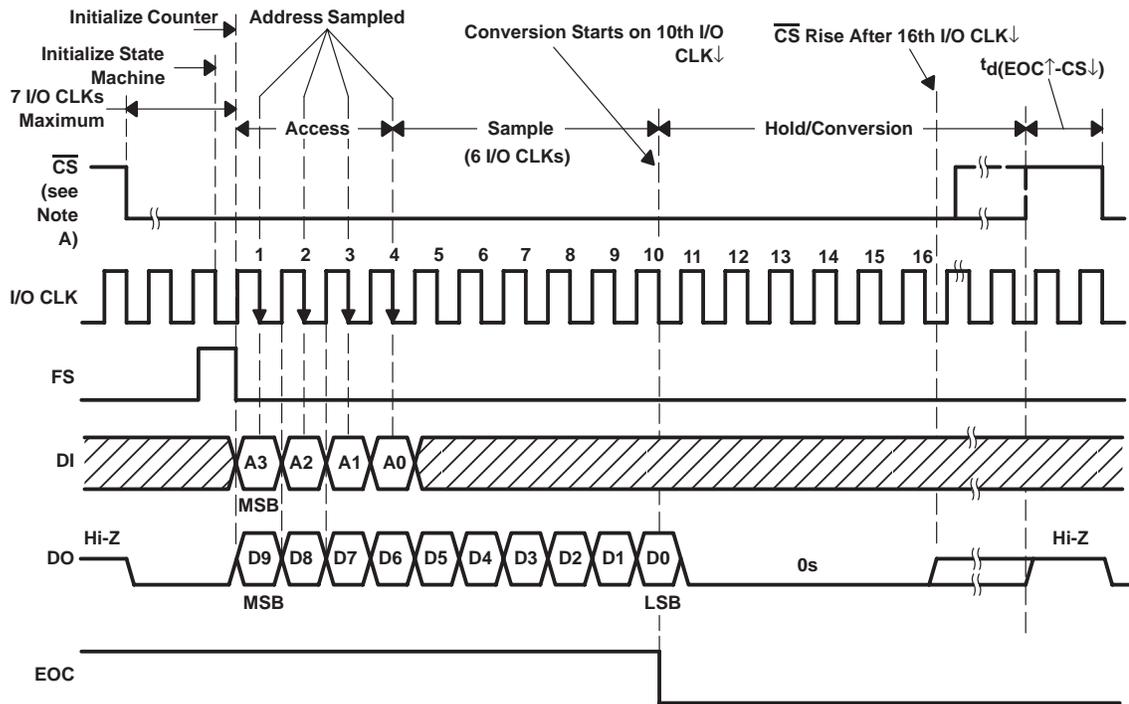
NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{CS}$ setup time elapses.

4.1.3   TLV1544 Signal State for Microprocessor and DSP

Table 4–1 lists the signal state in the microprocessor mode or the DSP mode of operation.

Table 4–1. TLV1544 Serial Interface Modes

I/O	Interface Mode	
	Microprocessor Action	**DSP Action**
CS↓	Initializes counter	Samples state of FS
CS↑	Resets state machine and disable I/O	Disables I/O
FS	Connects to V_{CC}	Connects to DSP FSX output. Initializes the state machine at each CLK↓ after FS↑. Starts a new cycle at each CLK↑ following the initialization (initializes the counter).
I/O CLK	Starts sampling of the analog input started at fourth I/O CLK↑. Conversion started at tenth I/O CLK↑.	Starts sampling of the analog input at fourth I/O CLK↓. Starts sampling of the analog input at tenth I/O CLK↓.
DATA IN	Samples input data on I/O CLK↑ ($\overline{INV\ CLK}$ high). Samples input data on I/O CLK↓ ($\overline{INV\ CLK}$ low).	Samples input data at I/O CLK↓ ($\overline{INV\ CLK}$ high). Samples input data at I/O CLK↑ ($\overline{INV\ CLK}$ low).
DATA OUT	Makes MSB available on $\overline{CS}\downarrow$. Changes remaining data on I/O CLK↓.	Makes MSB available FS↓. Changes remaining data at each following I/O CLK↑ after FS↓.

4.1.4 TLV1544 Terminal Functions

Table 4–2 explains the terminal functions for the TLV1544.

Table 4–2. Terminal Functions

Name	Terminal No. D	No. DB	I/O	Description
A0–A3 A4–A7	6–9 –	1–4 5–8	I	Analog inputs. The analog inputs are internally multiplexed. (For a source imped-ance greater than 1 kΩ, the asynchronous start should be used to increase the sampling time.)
$\overline{CS}$	16	15	I	Chip select. A high-to-low transition on $\overline{CS}$ resets the internal counters and controls and enables DATA IN, DATA OUT, and I/O CLK within the maximum setup time. A low-to-high transition disables DATA IN, DATA OUT, and I/O CLK within the setup time.
$\overline{CSTART}$	10	9	I	Sampling/conversion start control. $\overline{CSTART}$ controls the start of the sampling of an analog input from a selected multiplex channel. A high-to-low transition starts the sampling of the analog input signal. A low-to-high transition puts the sample-and-hold function in hold mode and starts the conversion. $\overline{CSTART}$ is independent from I/O CLK and works when $\overline{CS}$ is high. The low $\overline{CSTART}$ duration controls the duration of the sampling cycle for the switched capacitor array. $\overline{CSTART}$ is tied to V_{CC} if not used.
DATA IN	2	17	I	Serial data input. The 4-bit serial data selects the desired analog input and test voltage to be converted next in a normal cycle. These bits can also set the conversion rate and enable the power-down mode. When operating in the micro-processor mode, the input data is presented MSB first and is shifted in on the first four rising ($\overline{INV\ CLK} = V_{CC}$) or falling ($\overline{INV\ CLK}$ = GND) edges of I/O CLK (after $\overline{CS}\downarrow$). When operating in the DSP mode, the input data is presented MSB first and is shifted in on the first four falling ($\overline{INV\ CLK} = V_{CC}$) or rising ($\overline{INV\ CLK}$ = GND) edges of I/O CLK (after FS$\downarrow$). After the four input data bits have been read into the input data register, DATA IN is ignored for the remainder of the current conversion period.
DATA OUT	1	16	O	3-state serial output of the A/D conversion result. DATA OUT is in the high-impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low or after FS$\downarrow$ (in DSP mode). With a valid $\overline{CS}$ signal, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB or LSB value of the previous conversion result. DATA OUT changes on the falling (microprocessor mode) or rising (DSP mode) edge of I/O CLK.
EOC	4	19	O	End of conversion. EOC goes from a high to a low logic level on the tenth rising (microprocessor mode) or tenth falling (DSP mode) edge of I/O CLK and remains low until the conversion is complete and data is ready for transfer. EOC can also indicate that the converter is busy.
FS	13	12	I	DSP frame synchronization input. FS indicates the start of a serial data frame into or out of the device. FS is tied to V_{CC} when interfacing the device with a micropro-cessor.
GND	11	10		Ground return for internal circuitry. All voltage measurements are with respect to GND, unless otherwise noted.
$\overline{INV\ CLK}$	12	11	I	Inverted clock input. $\overline{INV\ CLK}$ is tied to GND when an inverted I/O CLK is used as the source of the input clock. This affects both microprocessor and DSP inter-faces. $\overline{INV\ CLK}$ is tied to V_{CC} if I/O CLK is not inverted. $\overline{INV\ CLK}$ can also invoke a built-in test mode.

Table 4–2. Terminal Functions (Continued)

Name	Terminal No. D	Terminal No. DB	I/O	Description
I/O CLK	3	18	I	Input/output clock. I/O CLK receives the serial I/O clock input in the two modes and performs the following four functions in each mode:
				Microprocessor mode
				• When $\overline{INVCLK}$ = V_{CC}, I/O CLK clocks the four input data bits into the input data register on the first four rising edges of I/O CLK after $\overline{CS}\downarrow$ with the multiplexer address available after the fourth rising edges. When $\overline{INV\ CLK}$ = GND, input data bits are clocked in on the first four falling edges instead.
				• On the fourth falling edge of I/O CLK, the analog input voltage on the selected multiplex input begins charging the capacitor array and continues to do so until the tenth rising edge of I/O CLK except in the extended sampling cycle where the duration of $\overline{CSTART}$ determines when to end the sampling cycle.
				• Output data bits change on the first ten falling I/O clock edges regardless of the condition of $\overline{INV\ CLK}$.
				• I/O CLK transfers control of the conversion to the internal state machine on the tenth rising edge of I/O CLK regardless of the condition of $\overline{INV\ CLK}$.
				Digital signal processor (DSP) mode
				• When $\overline{INV\ CLK}$ = V_{CC}, I/O CLK clocks the four input data bits into the input data register on the first four falling edges of I/O CLK after FS$\downarrow$ with the multiplexer address available after the fourth falling edges. When $\overline{INV\ CLK}$ = GND, input data bits are clocked in on the first four rising edges instead.
				• On the fourth rising edge of I/O CLK, the analog input voltage on the selected multiplex input begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLK except in the extended sampling cycle where the duration of $\overline{CSTART}$ determines when to end the sampling cycle.
				• Output data MSB shows after $\overline{FS}\downarrow$ and the rest of the output data bits change on the first ten rising I/O CLK edges regarless of the condition of $\overline{INV\ CLK}$.
				• I/O CLK transfers control of the conversion to the internal state machine on the tenth falling edge of I/O CLK regardless of the condition of $\overline{INV\ CLK}$.
REF+	15	14	I	Upper reference voltage (nominally V_{CC}). The maximum input voltage range is determined by the difference between the voltages applied to REF+ and REF–.
REF–	14	13	I	Lower reference voltage (nominally ground)
V_{CC}	5	20	I	Positive supply voltage

4.2   Microprocessor Serial Interface

Input data bits from DATA IN are clocked in on the first four rising edges of the I/O CLK sequence if $\overline{\text{INV CLK}}$ is held high when the device is in microprocessor interface mode. Input data bits are clocked in on the first four falling edges of the I/O CLK sequence if $\overline{\text{INV CLK}}$ is held low. The MSB of the previous conversion appears on DATA OUT on the falling edge of $\overline{\text{CS}}$. The remaining nine bits are shifted out on the next nine edges (depending on the state of $\overline{\text{INV CLK}}$) of I/O CLK. Ten bits of data are transmitted to the host through DATA OUT.

A minimum of 9.5 clock pulses is required for the conversion to begin. On the tenth clock rising edge, the EOC output goes low and returns to the high logic level when the conversion is complete, and then the result can be read by the host. On the tenth clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero if the I/O CLK transfer is more than ten clocks long.

$\overline{\text{CS}}$ is inactive (high) between serial I/O CLK transfers. Each transfer takes at least ten I/O CLK cycles. The falling edge of $\overline{\text{CS}}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{\text{CS}}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{\text{CS}}$ disables I/O CLK and DATA IN within a setup time. A conversion does not begin until the tenth I/O CLK rising edge.

A high-to-low transition on $\overline{\text{CS}}$ within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the output data register holds the previous conversion result). $\overline{\text{CS}}$ should not be taken low close to completion of conversion because the output data can be corrupted.

4.3 DSP Interface

The TLV1544 can also interface with a DSP, from the TMS320 family for example, through a serial port. The analog-to-digital converter (ADC) serves as a slave device where the DSP supplies FS and the serial I/O CLK. Transmit and receive operations are concurrent. The falling edge of FS must occur no later than seven I/O CLK periods after the falling edge of $\overline{CS}$.

DSP I/O cycles differ from microprocessor I/O cycles in the following ways:

❏ When interfaced with a DSP, the output data MSB shows after $\overline{FS}\downarrow$ and the rest of the output data changes on the rising edge of I/O CLK, and input data is sampled on the first four falling edges of I/O CLK after FS falling when $\overline{INV\ CLK}$ is high, or the first four rising edges of I/O CLK after FS falling when $\overline{INV\ CLK}$ is low. This operation is the opposite when interfaced with a microprocessor.

❏ A new DSP I/O cycle is started on the rising edge of I/O CLK after the rising edge of FS. The internal state machine is reset on each falling edge of I/O CLK when FS is high. This operation is opposite when interfaced with a microprocessor.

❏ The TLV1544 supports a 16-clock cycle when interfaced with a DSP. The output data is padded with six trailing zeros when it is operated in DSP mode.

4.4 TLV1544 to TMS320C50

Figure 4–6 is the schematic diagram showing the hardware connections between the TLV1544 and the TMS320C50.

Figure 4–6. Schematic Diagram

NOTE: Software programs using interrupt processing may need the inverter and the connection shown in dotted lines. In programs using wait states, EOC is not required.

Grounding Considerations

This appendix contains general information on grounding techniques for a printed circuit board using the TLV1544.

A.1 Printed Circuit Board Grounding Considerations

When designing analog circuits that share a ground with digital and high current power supplies, the voltage drop along the high current paths must be considered. This voltage drop is a result of the current flowing through the greater than zero resistance of the current path, or high frequency current transients flowing through a greater than zero inductance of a current path.

If the signal ground is connected to the power supply ground at an improper location, an excessive voltage drop may occur in the signal ground and appears as part of the signal, causing an error.

The solution for low frequency analog signals is to establish a single ground point on the PC board and connect all low frequency grounds to that point. By using this method, currents flowing along any one path to ground do not produce error voltages in any other ground path.

Analyzing the current flow paths within the analog section gives an indication of which components can be lumped together to a common ground path and which should be separate. One half LSB error with a reference of 4.1 volts would be approximately 0.5 mV, so the ground trace resistance would have to be greater than 0.5 ohms with 1 mA of ground current.

When input source signals are low current, a common ground trace may be appropriate. Higher input current sources, however should always have a separate ground trace to the most robust ground point location, usually at the ground entrance to the PCB.

Even though the TLV1544 operating current is low, some high speed current transients are present, usually caused by output digital switching requiring a ground plane or wide ground return trace to the central board entry ground for these signals. All signal paths and their respective ground returns must be examined to minimize signal loop area.

The power inputs and V_{CC} lines must also be analyzed in the same manner and detail that the ground returns are.