SN65518, SN75518
VACUUM FLUORESCENT DISPLAY DRIVERS

SLDS004B – MARCH 1983 – REVISED MAY 1990

- **Each Device Drives 32 Lines**
- **60-V Output Voltage Swing Capability**
- **25-mA Output Source Current Capability**
- **High-Speed Serially Shifted Data Input**
- **Latches on All Driver Outputs**

description

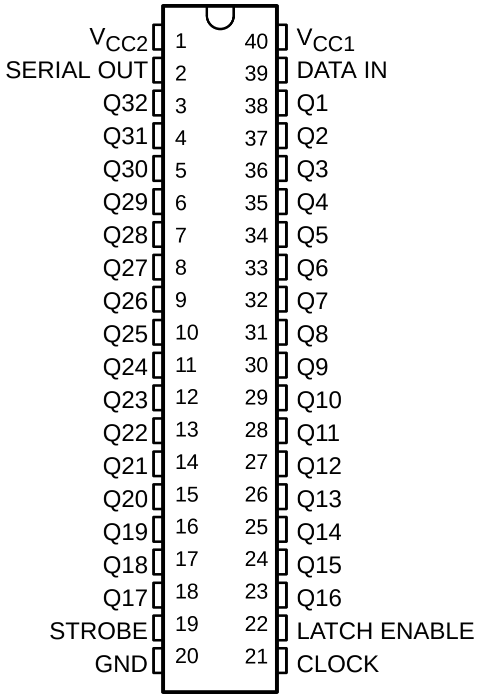
The SN65518 and SN75518 are monolithic BIDFET† integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display.

Each device consists of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. While LATCH ENABLE is high, parallel data is transferred to the output buffers through a 32-bit latch. Data present in the latch during the high-to-low transition of LATCH ENABLE is latched. When STROBE is low, all Q outputs are enabled. When STROBE is high, all Q outputs are low.

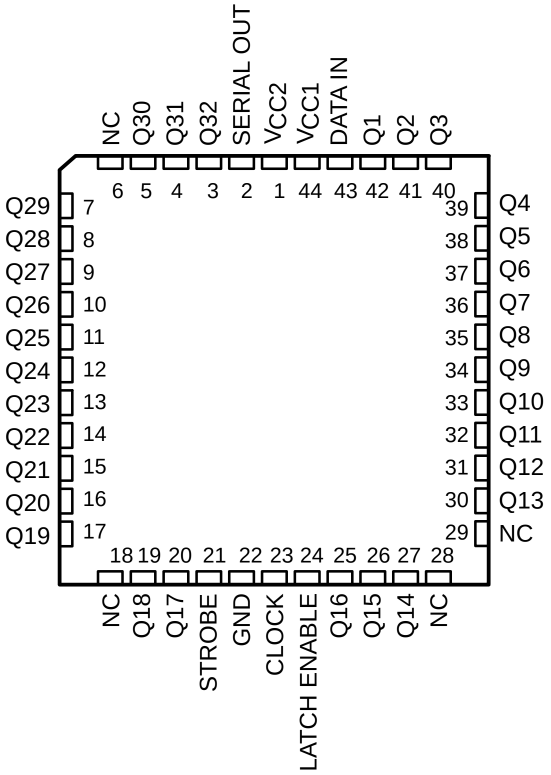
Serial data output from the shift register may be used to cascade additional devices. This output is not affected by LATCH ENABLE or STROBE.

The SN65518 is characterized for operation from –40°C to 85°C. The SN75518 is characterized for operation from 0°C to 70°C.

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

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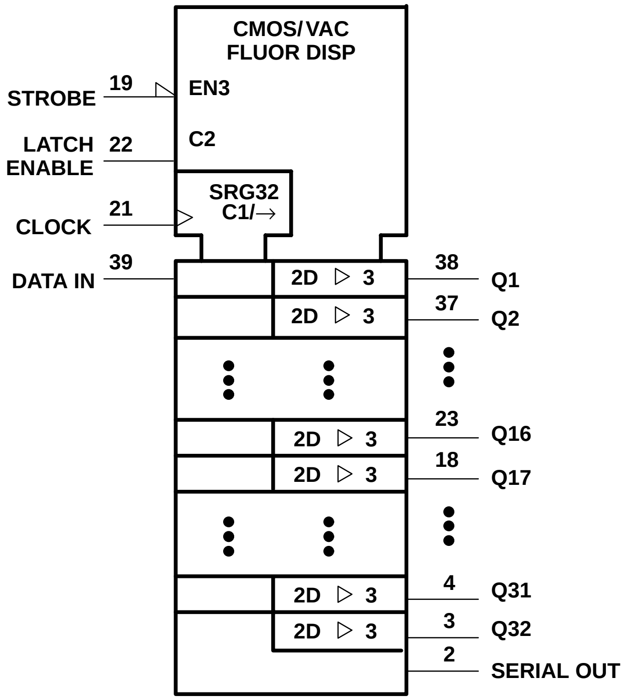
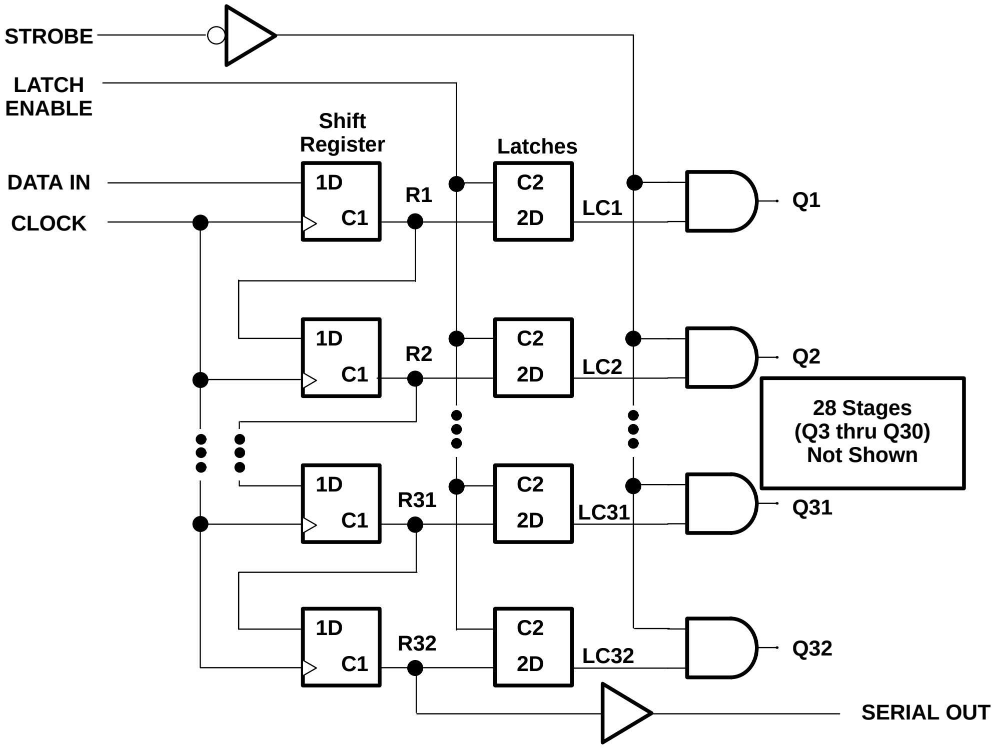
† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

logic diagram (positive logic)



FUNCTION TABLE

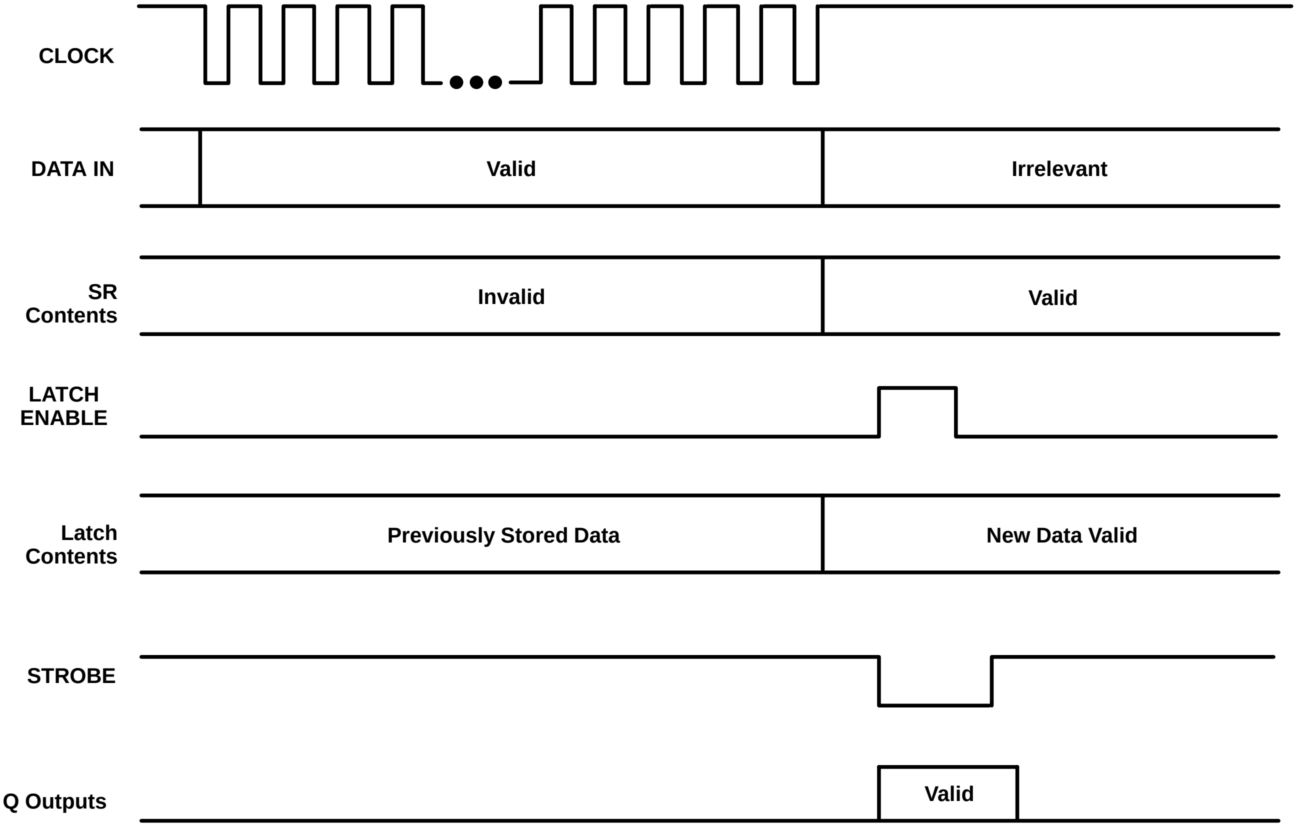
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R32	LATCHES LC1 THRU LC32	OUTPUTS	
	CLOCK	LATCH ENABLE	STROBE			SERIAL	Q1 THRU Q32
Load	↑ No ↑	X X	X X	Load and shift[†] No change	Determined by LATCH ENABLE[‡]	R32	Determined by STROBE
Latch	X X	L H	X X	As determined above	Stored data New data	R32	Determined by STROBE
Strobe	X X	X X	H L	As determined above	Determined by LATCH ENABLE[‡]	R32	All L LC1 thru LC32, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.

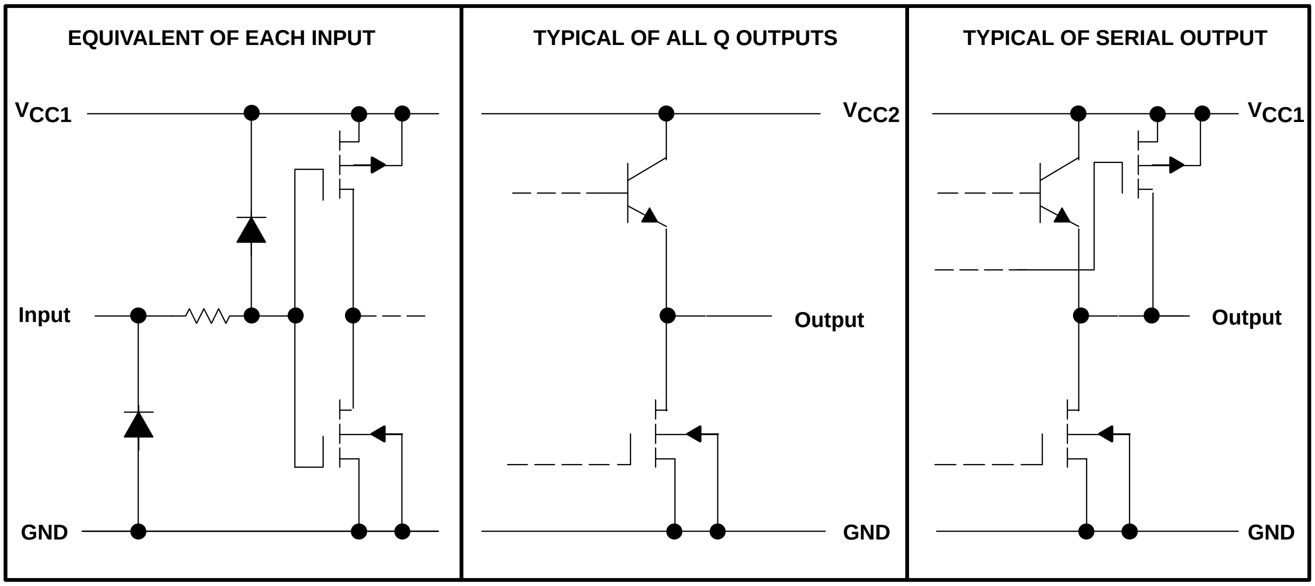
[†] R32 and the serial output take on the state of R31, R31 takes on the state of R30, ... R2 takes on the state of R1, and R1 takes on the state of the data input.

[‡] New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1)	15 V
Supply voltage, V_{CC2}	70 V
Input voltage, V_I	V_{CC1}
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65518	–40°C to 85°C
SN75518	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1700 mW	13.6 mW/°C	1088 mW	884 mW
N	1250 mW	10.0 mW/°C	800 mW	650 mW

recommended operating conditions, T_A = 25°C (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{CC1}		4.5	15	V
Supply voltage, V_{CC2}		0	60	V
High-level input voltage, V_{IH} (see Figure 1)	V_{CC1} = 4.5 V	3.5		V
	V_{CC1} = 15 V	12		
Low-level input voltage, V_{IL} (see Figure 1)		–0.3	0.8	V
High-level output current, I_{OH}			–25	mA
Low-level output current, I_{OL}			2	mA
Clock frequency, f_{clock} (see Figure 2)	V_{CC1} = 10 V to 15 V	0	5	MHz
	V_{CC1} = 4.5 V	0	1	
Pulse duration, CLOCK high, $t_{w(CKH)}$	V_{CC1} = 10 V to 15 V	100		ns
	V_{CC1} = 4.5 V	500		
Pulse duration, CLOCK low, $t_{w(CKL)}$	V_{CC1} = 10 V to 15 V	100		ns
	V_{CC1} = 4.5 V	500		
Setup time, DATA IN before CLOCK↑, t_{su}	V_{CC1} = 10 V to 15 V	75		ns
	V_{CC1} = 4.5 V	150		
Hold time, DATA IN after CLOCK↑, t_h	V_{CC1} = 10 V to 15 V	75		ns
	V_{CC1} = 4.5 V	150		
Operating free-air temperature, T_A	SN65518	–40	85	°C
	SN75518	0	70	

electrical characteristics over recommended ranges of operating free-air temperature and V_{CC1}, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –12 mA				–1.5	V
V_{OH}	High-level output voltage	Q outputs	I_{OH} = –25 mA		57.5	58		V
		SERIAL OUT	V_{CC1} = 5 V,	I_{OH} = –20 µA	4.5	4.9	5	
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 1 mA				5	V
		SERIAL OUT	I_{OL} = 20 µA			0.06	0.8	
I_{IH}	High-level input current		V_{CC1} = 15 V,	V_I = 15 V		0.1	1	µA
I_{IL}	Low-level input current		V_{CC1} = 15 V,	V_I = 0 V		–0.1	–1	µA
I_{CC1}	Supply current		V_{CC1} = 4.5 V			1.8	4	mA
			V_{CC1} = 15 V			2	5	
I_{CC2}	Supply current	SN65518	Outputs high,	T_A = –40°C			12	mA
		SN65518, SN75518	Outputs high,	T_A = 0°C to MAX		7	10	
			Outputs low			0.01	0.5	

† All typical values are at T_A = 25°C.

switching characteristics, V_{CC2} = 60 V, C_L = 50 pF, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
t_d	Delay time, CLOCK to DATA OUT		V_{CC1} = 4.5 V	C_L = 15 pF, See Figure 4		600	ns
			V_{CC1} = 15 V			150	
t_{DHL}	Delay time, high-to-low-level Q output	From LATCH ENABLE	V_{CC1} = 4.5 V	See Figure 5		1.5	µs
		From STROBE		See Figure 6		1	
		From LATCH ENABLE	V_{CC1} = 15 V	See Figure 5		0.5	
		From STROBE		See Figure 6		0.5	
t_{DLH}	Delay time, low-to-high-level Q output	From LATCH ENABLE	V_{CC1} = 4.5 V	See Figure 5		1.5	µs
		From STROBE		See Figure 6		1	
		From LATCH ENABLE	V_{CC1} = 15 V	See Figure 5		0.25	
		From STROBE		See Figure 6		0.25	
t_{THL}	Transition time, high-to-low-level Q output		V_{CC1} = 4.5 V	See Figure 6		3	µs
			V_{CC1} = 15 V			1.5	
t_{TLH}	Transition time, low-to-high-level Q output		V_{CC1} = 4.5 V	See Figure 6		2.5	µs
			V_{CC1} = 15 V			0.75	

RECOMMENDED OPERATING CONDITIONS

INPUT VOLTAGE
vs
SUPPLY VOLTAGE V_{CC1}

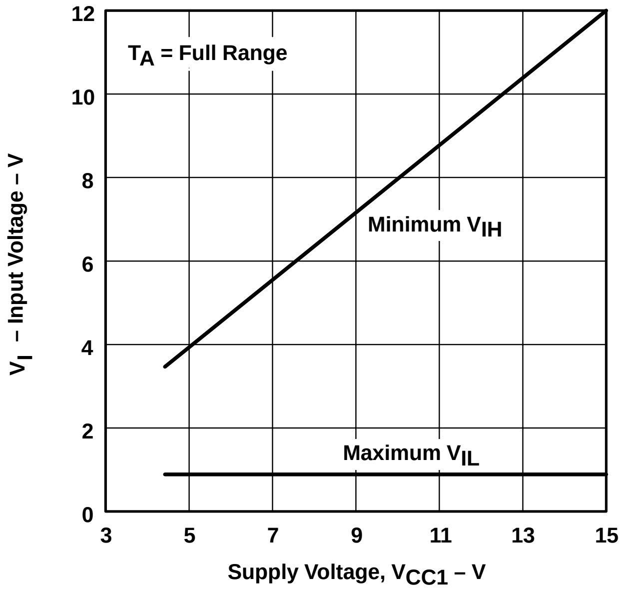


Figure 1

MAXIMUM CLOCK FREQUENCY
vs
SUPPLY VOLTAGE V_{CC1}

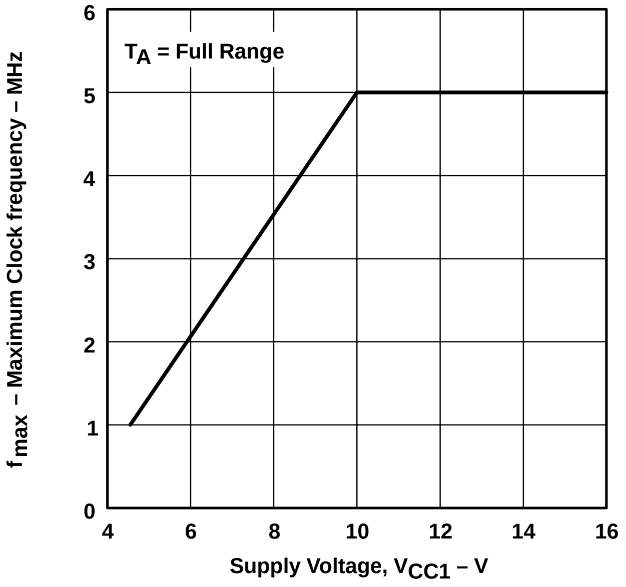


Figure 2

PARAMETER MEASUREMENT INFORMATION†

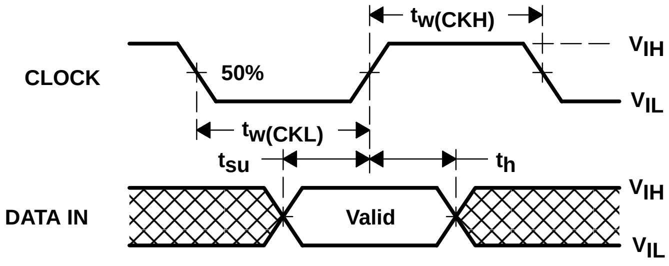


Figure 3. Input Timing Waveforms

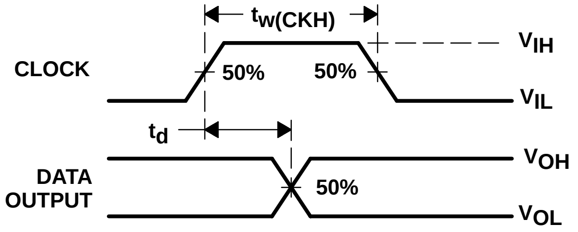


Figure 4. Data Output Switching Times

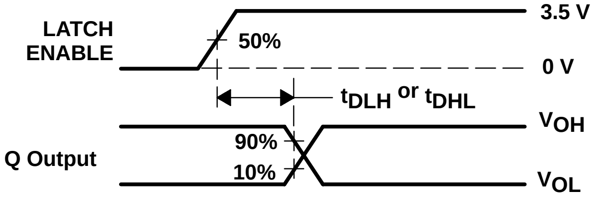


Figure 5. Q Output Switching Times

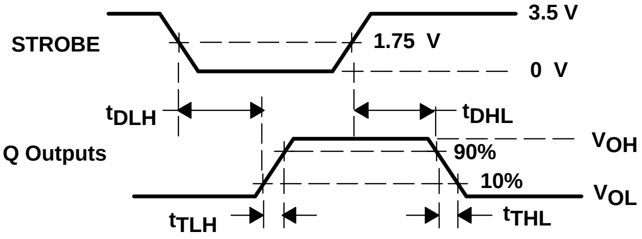


Figure 6. Switching Time Voltage Waveforms

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† For testing purposes, all input pulses have maximum rise and fall times of 30 ns.

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