- Each Device Drives 12 Lines
- 60-V Output Voltage Swing Capability
- 25-mA Output Source Current Capability
- High-Speed Serially-Shifted Data Input
- TTL-Compatible Inputs
- Latches on All Driver Outputs

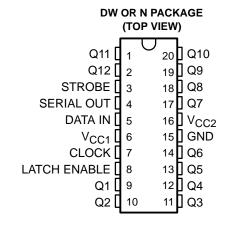
description

The SN65512B and SN75512B are monolithic BIDFET[†] integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display.

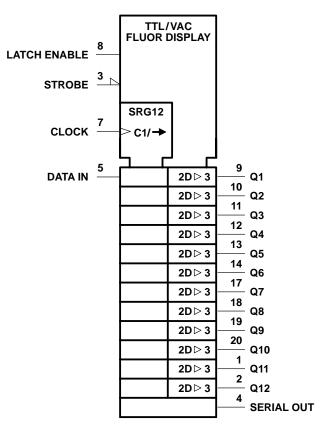
All device inputs are diode-clamped pnp inputs and assume a high logic level when open circuited. The nominal input threshold voltage is 1.5 V. Outputs are totem-pole structures formed by an npn emitter-follower and double-diffused MOS (DMOS) transistors.

The device consists of a 12-bit shift register, 12 latches, and 12 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 12 latches. The active-low STROBE input enables all Q outputs. Serial data output from the shift register can be used to cascade shift registers. This output is not affected by LATCH ENABLE or STROBE.

The SN65512B is characterized for operation from -40°C to 85°C. The SN75512B is characterized for operation from 0°C to 70°C.



logic symbol‡

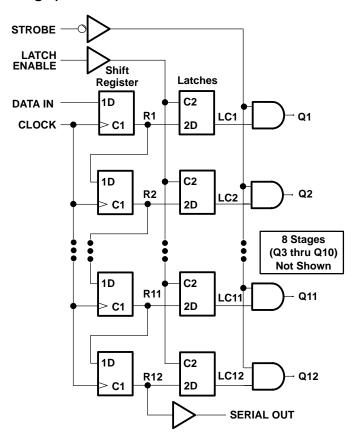


[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

†BIDFET - Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.



logic diagram (positive logic)



FUNCTION TABLE

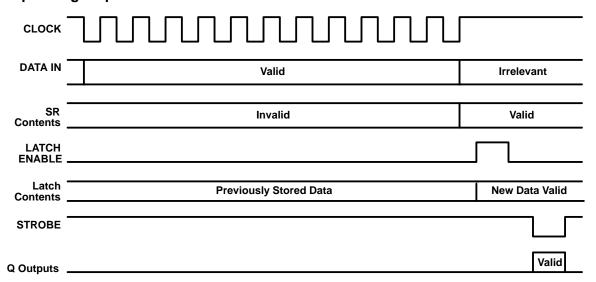
	CONTROL INPUTS CLOCK LATCH STROBE		SHIFT REGISTER	LATCHES	OUTPUTS			
FUNCTION			STROBE	R1 THRU R12	LC1 THRU LC12	SERIAL	Q1 THRU Q12	
Load	↑ No ↑	Х	Х	Load and shift [†] No change	Determined by LATCH ENABLE [‡]	R12	Determined by STROBE	
Latch	Х	L H	Х	As determined above	Stored data New data	R12	Determined by STROBE	
Strobe	Х	Х	H L	As determined above	Determined by LATCH ENABLE‡	R12	All LC LC1 thru LC12, respectively	

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition

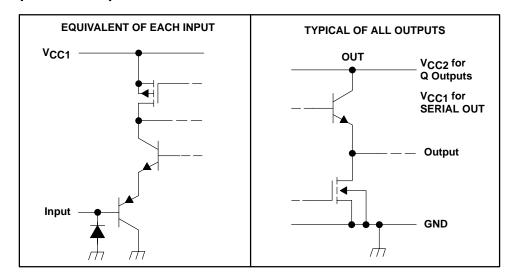
[†]R12 takes on the state of R11, R11 takes on the state of R10, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

[‡] New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematics of inputs and outputs



SN65512B, SN75512B VACUUM FLUORESCENT DISPLAY DRIVERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC1} (see Note 1)	15 V
Supply voltage, V _{CC2}	70 V
Input voltage, V _I	
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T _A : SN65512B	–40°C to 85°C
SN75512B	0°C to 70°C
Storage temperature range, T _{stq}	65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_{\mbox{\scriptsize A}} \leq 25^{\circ}\mbox{\scriptsize C}$ POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 125°C POWER RATING		
DW	1125 mW	9.0 mW/°C	720 mW	585 mW		
N	1150 mW	9.2 mW/°C	736 mW	589 mW		

recommended operating conditions

			SN65	512B	SN75512B		UNIT				
			MIN	MAX	MIN	MAX	UNII				
Supply voltage, V _{CC1}			5	15	5	15	V				
Supply voltage, V _{CC2}			0	60	0	60	60 V				
High-level input voltage, VIH			2		2		V				
Low-level input voltage, V _{IL}				0.8		8.0	3 V				
High-level output current, IOH				-25		-25	mA				
Low-level output current, IOL	V _{CC1} = 10 V			5		5	mA				
Clock frequency, f _{clock}	V _{CC1} = 15 V,	T _A = 25°C	0	4	0	4	MHz				
Clock frequency, fclock	$V_{CC1} = 5 V$,	T _A = 25°C	0	1	0	1					
Pulse duration, CLOCK high or low, t _w	$V_{CC1} = 15 \text{ V},$	$T_A = 25^{\circ}C$	100		100		ns				
uise duration, CLOCK high or low, tw	$V_{CC1} = 5 V$,	$T_A = 25^{\circ}C$	500		500						
Setup time DATA IN valid before CLOCK \$ 1 (see Figure 1)	$V_{CC1} = 15 \text{ V},$	$T_A = 25^{\circ}C$	100		100		ns				
Setup time, DATA IN valid before CLOCK ↑, t _{SU} (see Figure 1)	$V_{CC1} = 5 V$,	T _A = 25°C	250		250		115				
Hold time DATA IN volid ofter CLOCK 1 (con Figure 1)	$V_{CC1} = 15 \text{ V},$	T _A = 25°C	50		50		ns				
Hold time, DATA IN valid after CLOCK ↑, th (see Figure 1)	$V_{CC1} = 5 V$,	T _A = 25°C	250	·	250		115				
Operating free-air temperature, TA			-40	85	0	70	°C				

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electrical characteristics over recommended operating free-air temperature range, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT	
٧ıK	Input clamp voltage		I _I = -12 mA				-1.5	V	
Va		Q outputs	$I_{OH} = -25 \text{ mA},$	V _{CC1} = 10 V	57.5	58		V	
VOH	High-level output voltage	SERIAL OUT	$I_{OH} = -200 \mu A$	V _{CC1} = 10 V	9	9.5		v	
V _{OL}	Low-level output voltage	Q outputs	$I_{OL} = 5 \text{ mA},$	V _{CC1} = 10 V		2.6	5	V	
		SERIAL OUT	$I_{OL} = 200 \mu A$,	V _{CC1} = 10 V		0.05	0.2	v	
lн	High-level input current		V _{CC1} = 15 V,	V _I = 5 V		0.01	1	μΑ	
I _I L	I _{IL} Low-level input current			V _I = 0.8 V		-25	-150	μΑ	
L - Cumply oursest from \/ -		V15.V	V _I = 5 V		80	500	μΑ		
ICC1	Supply current from V _{CC1}		V _{CC1} = 15 V	V _I = 0.8 V		2	6	mA	
laaa	Supply current from V _{CC2}		V _{CC1} = 15 V	All outputs high		10	100	μΑ	
ICC2				STROBE at 2 V		0.8	3	mA	

[†] All typical values are at V_{CC1} = 5 V, T_A = 25°C.

switching characteristics, V_{CC1} = 10 V, V_{CC2} = 60 V, T_A = 25°C

	PARAMETER	TEST CON	MIN	MAX	UNIT	
tPHL	Propagation delay time, high-to-low level output		See Figure 2		300	ns
tpLH	Propagation delay time, low-to-high level output	C _L = 30 pF,			300	ns
tTHL	Transition time, high-to-low level output				500	ns
^t TLH	Transition time, low-to-high level output				500	ns

PARAMETER MEASUREMENT INFORMATION

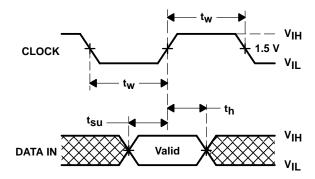


Figure 1. Input Timing Voltage Waveforms

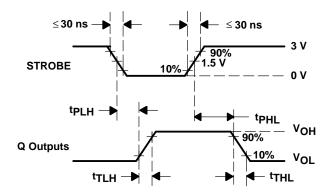


Figure 2. Switching Time Voltage Waveforms

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