

SN751506, SN751516 DC PLASMA DISPLAY DRIVERS

SLDS034 – DECEMBER 1986 – REVISED JULY 1989

- Each Device Drives 32 Lines
- 180-V Open-Drain Parallel Outputs
- 220-mA Parallel Output Sink Current Capability
- CMOS-Compatible Inputs
- Strobe Input Provided
- Serial Data Output for Cascade Operation
- Inputs Have Built-In Electrostatic Discharge Protection

description

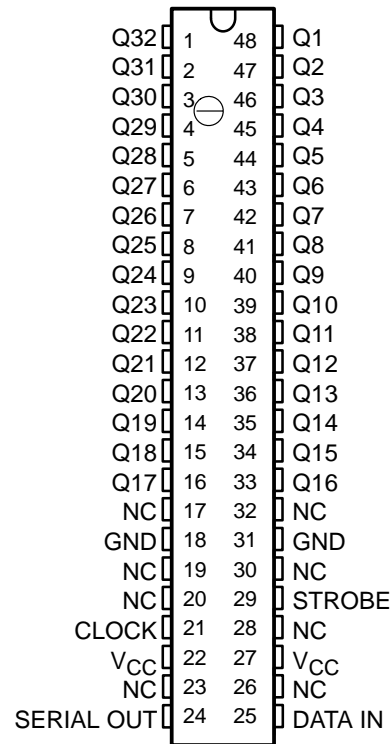
The SN751506 and the SN751516 are monolithic integrated circuits designed to drive the scan lines of a dc plasma panel display. The SN751516 pin sequence is reversed from the SN751506 for ease in printed-circuit-board layout.

Each device consists of a 32-bit shift register and 32 OR gates. Serial data is entered into the shift register on the high-to-low transition of the clock input. When STROBE is low, all Q outputs are in the off state. Outputs are open-drain JFET transistors with a breakdown voltage in excess of 180 V. The outputs have a 220-mA sink current capability in the on state. Only one Q output should be allowed to be in the on state at a time.

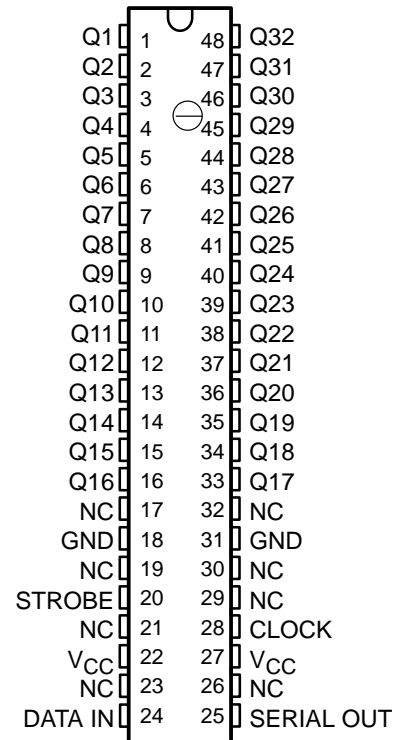
SERIAL OUT from the shift register can be used to cascade shift registers. This output is not affected by the STROBE input. All inputs are CMOS compatible with ESD protection built in.

The SN751506 and SN751516 are characterized for operation from 0°C to 70°C.

SN751506 . . . FT PACKAGE
(TOP VIEW)



SN751516 . . . FT PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

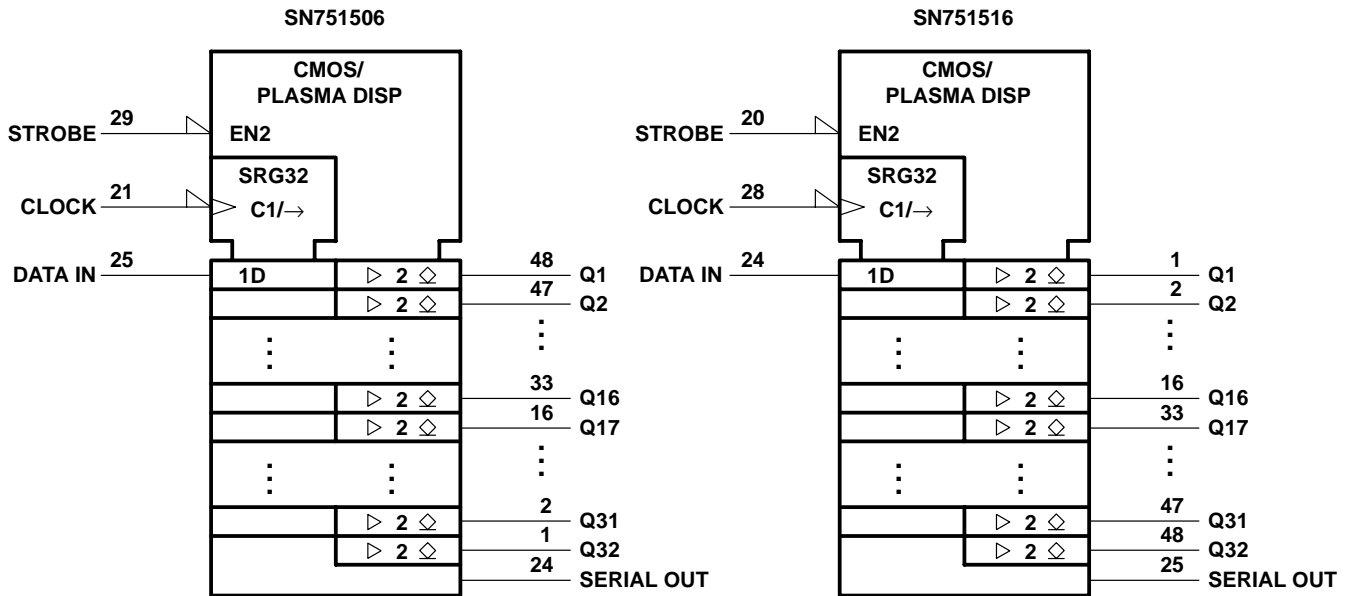
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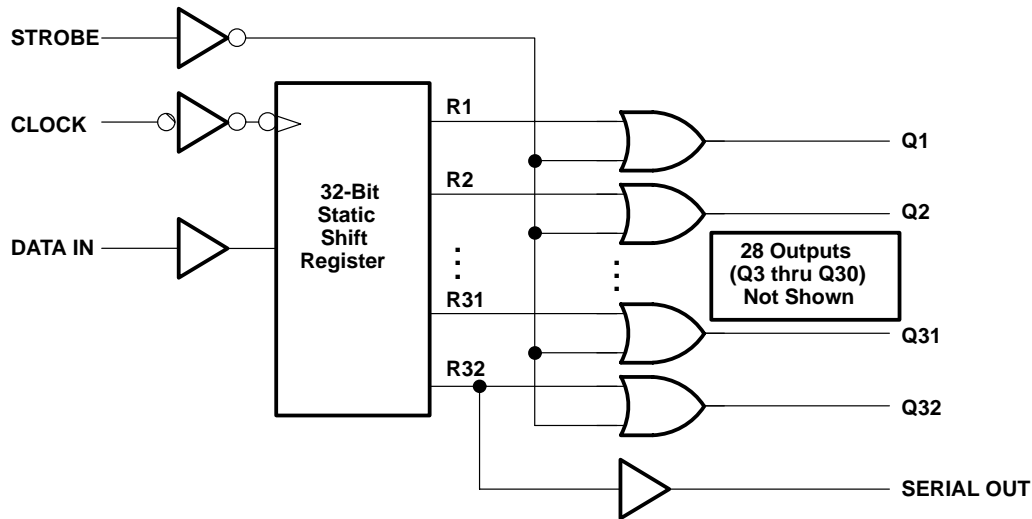
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logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



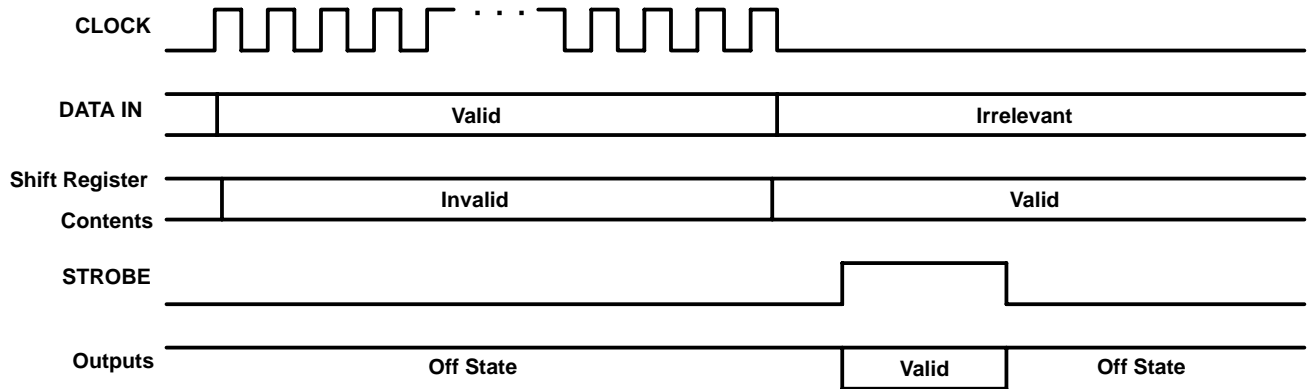
FUNCTION TABLE

FUNCTION	CONTROL INPUTS		SHIFT REGISTERS R1 THRU R32	OUTPUTS	
	CLOCK	STROBE		SERIAL	Q1 THRU Q32
Load	↓	X	Load and shift‡	R32	Determined by STROBE
	No ↓	X	No change	R32	
Strobe	X	L	As determined above	R32	All high impedance R1 through R32
	X	H		R32	

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition.

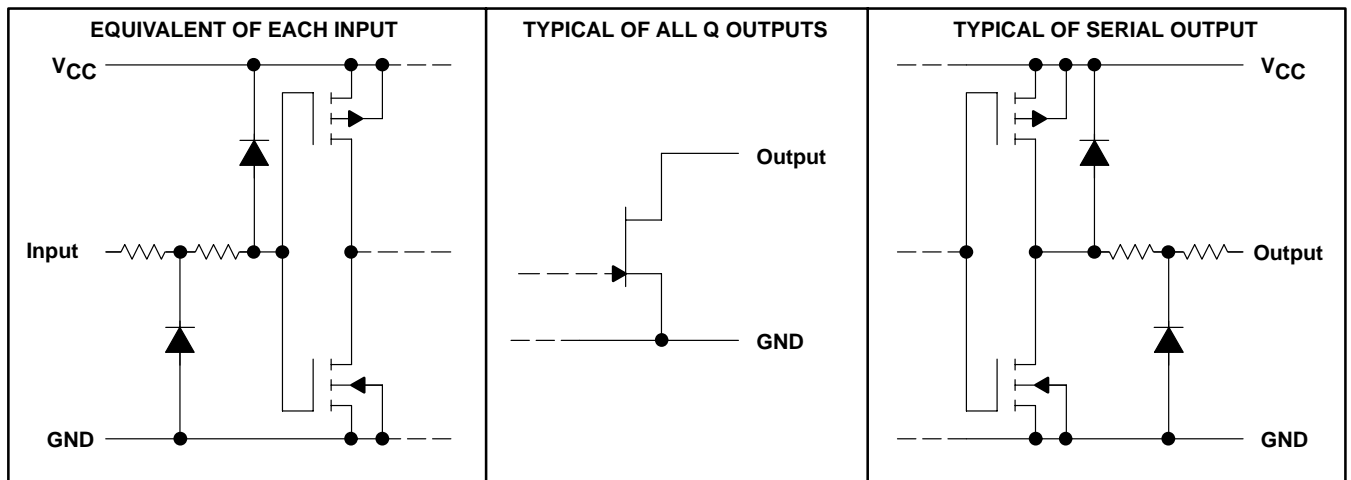
‡ R32 takes on the state of R31, R31 takes on the state of R30, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



† Only 1 bit in 32 should be low in the input data.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1)	–0.4 V to 7 V
On-state Q output voltage range, V_O	–0.4 V to 125 V
Off-state Q output voltage range, V_O	–0.4 V to 180 V
Input voltage range, V_I	–0.4 V to $V_{CC} + 0.4$ V
Serial output voltage range	–0.4 V to $V_{CC} + 0.4$ V
Q output on-state time duration (see Note 2)	100 μ s
Q output duty cycle (see Note 2)	1/200
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 3)	1025 mW
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

- NOTES: 1. Voltage values are with respect to GND.
 2. Only one Q output should be on at a time.
 3. For operation above 25°C free-air temperature, derate linearly to 656 mW at 70°C at the rate of 8.2 mW/°C.

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recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4	5	6	V
Peak on-state Q output voltage, $V_{O(on)}$				110	V
High-level input voltage, V_{IH}	$V_{CC} = 4\text{ V}$	3.2			V
	$V_{CC} = 6\text{ V}$	4.8			
Low-level input voltage, V_{IL}	$V_{CC} = 4\text{ V}$			0.8	V
	$V_{CC} = 6\text{ V}$			1.2	
Output current, I_O ($T_A = 25^\circ\text{C}$)				220	mA
Clock frequency, f_{clock}				200	kHz
Pulse duration, CLOCK high or low, $t_w(\text{CLK})$		1.5†			μs
Pulse duration, DATA, $t_w\text{D}$		5			μs
Pulse duration, STROBE, $t_w(\text{STRB})$		2			μs
Setup time, DATA IN before CLOCK \downarrow , t_{su}		1			μs
Hold time, DATA IN after CLOCK \downarrow , t_h		1.2			μs
Operating free-air temperature, T_A		0		70	$^\circ\text{C}$

† The minimum clock period is 5 μs .

electrical characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	SERIAL OUT	$I_{OH} = -0.1\text{ mA}$	4.5		V
V_{OL}	Low-level output voltage	Q outputs	$I_{OL} = 180\text{ mA}$	6	10	V
		SERIAL OUT	$I_{OL} = 0.1\text{ mA}$		0.5	
$I_{O(off)}$	Off-state output current	Q outputs	$V_{OH} = 110\text{ V}$		1	μA
I_{OL}	Low-level output current	Q outputs	$V_{OL} = 16\text{ V}$	220		mA
I_{IH}	High-level input current	$V_I = V_{CC}$			1	μA
I_{IL}	Low-level input current	$V_I = 0$			-1	μA
C_i	Input capacitance				15	pF
I_{CC}	Supply current	All Q outputs off			1	mA
		One Q output on		20	40	

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, CLOCK to SERIAL OUT	$C_L = 15\text{ pF}$		0.2	0.5	μs
t_{DHL}	Delay time, high-to-low-level Q output from STROBE or CLOCK inputs	$C_L = 150\text{ pF}$, $R_L = 470\ \Omega$, See Figures 2 and 3		0.2‡	0.6	μs
t_{DLH}	Delay time, low-to-high-level Q output from STROBE or CLOCK inputs			0.35‡	1	μs
t_{THL}	Transition time, high-to-low-level Q output			0.1	0.3	μs
t_{TLH}	Transition time, low-to-high-level Q output			0.35	1	μs

‡ Typical values are for clock inputs. Typical values from STROBE will be less.



PARAMETER MEASUREMENT INFORMATION

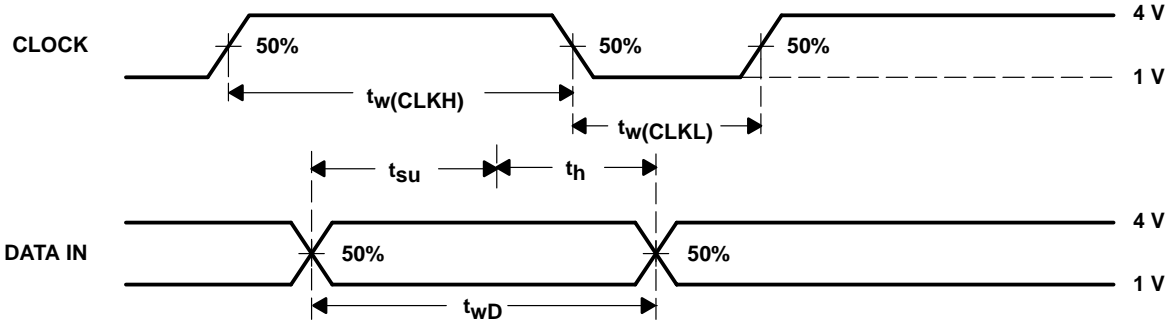


Figure 1. Input Timing Voltage Waveforms

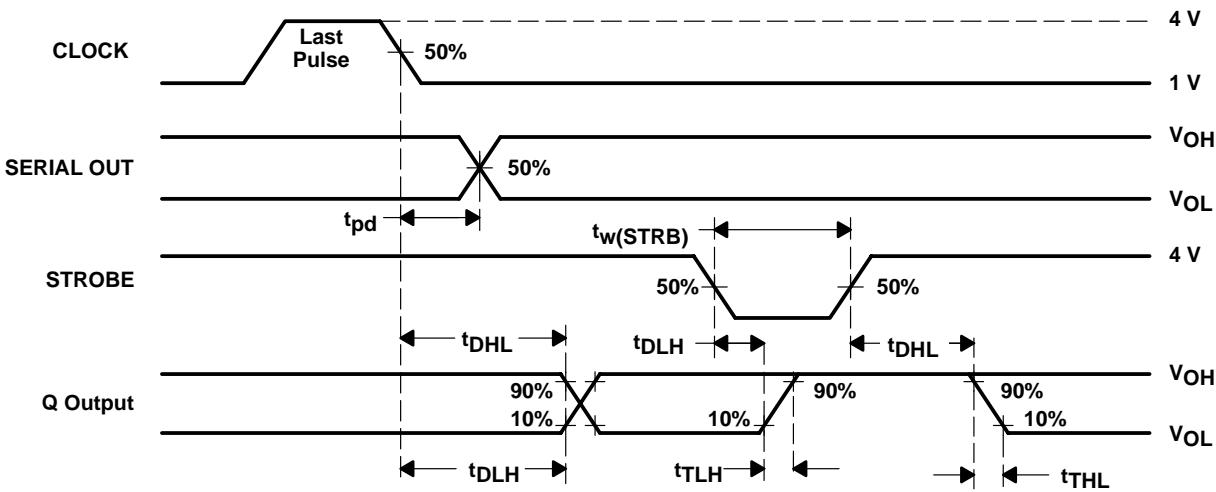
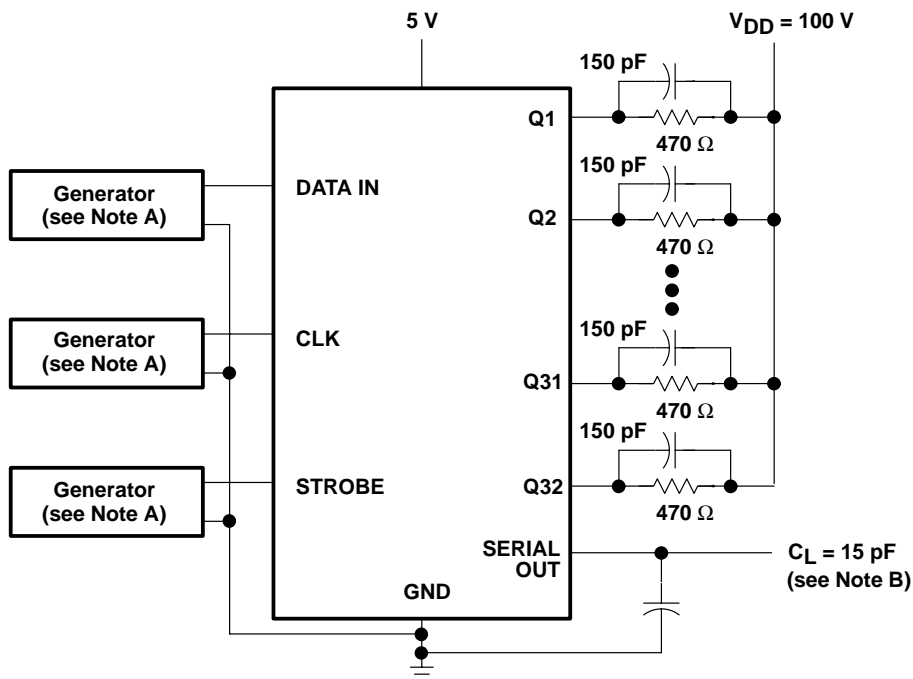


Figure 2. Switching Characteristics

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Input pulses are supplied by generators having the following characteristics: $t_w = 1.25 \mu s$, $PRR \leq 200 \text{ kHz}$, $t_r \leq 30 \text{ ns}$, $t_f \leq 30 \text{ ns}$, $Z_0 = 50 \Omega$.
- B. C_L includes probe and jig capacitance.

Figure 3. Test Circuit

TYPICAL CHARACTERISTICS

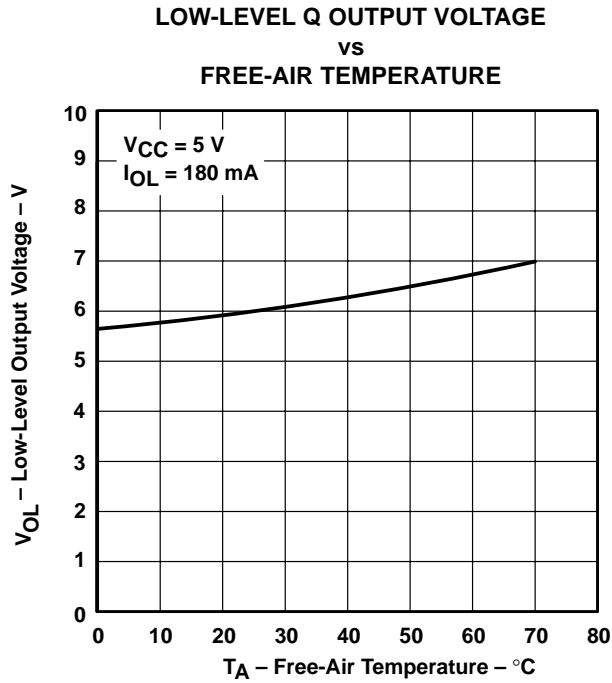


Figure 4

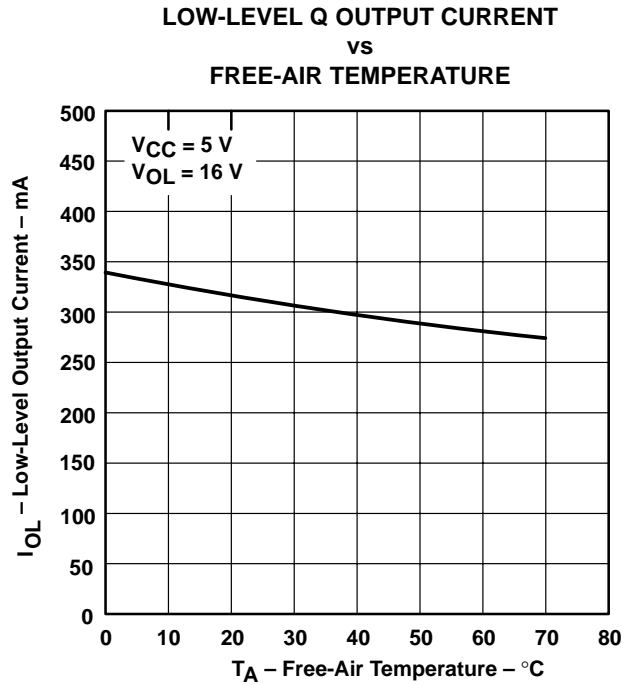


Figure 5

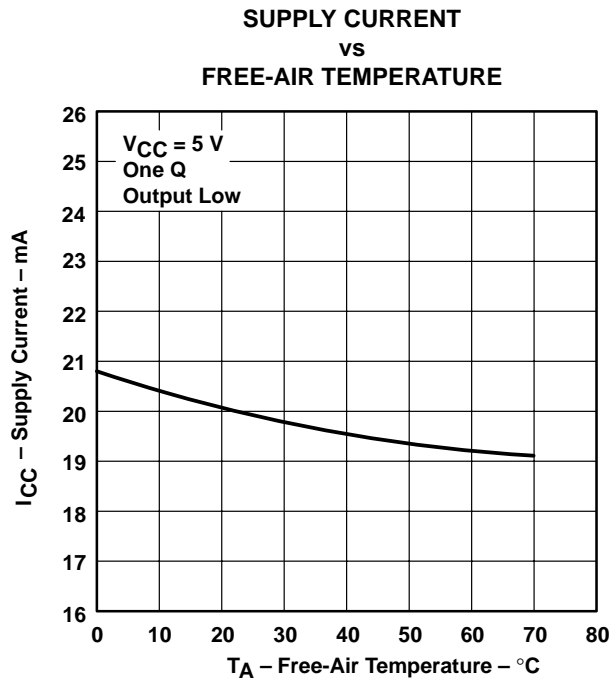


Figure 6

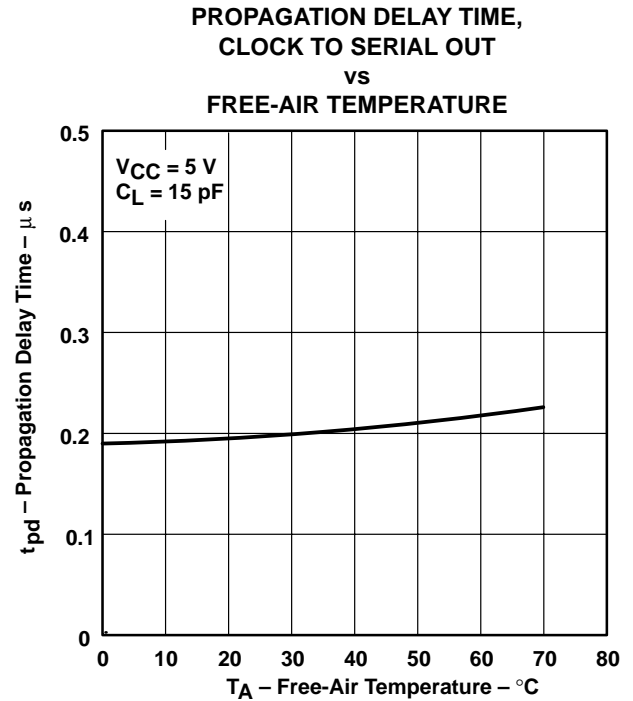


Figure 7

TYPICAL CHARACTERISTICS

DELAY TIME,
HIGH-TO-LOW-LEVEL Q OUTPUT
vs
FREE-AIR TEMPERATURE

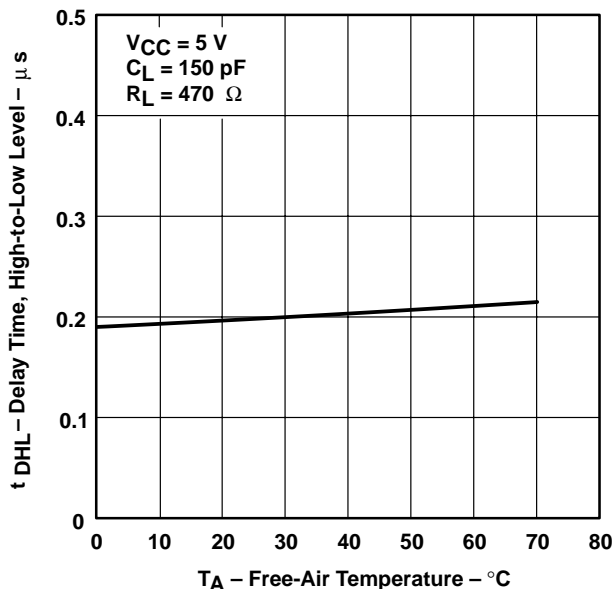


Figure 8

DELAY TIME,
LOW-TO-HIGH-LEVEL Q OUTPUT
vs
FREE-AIR TEMPERATURE

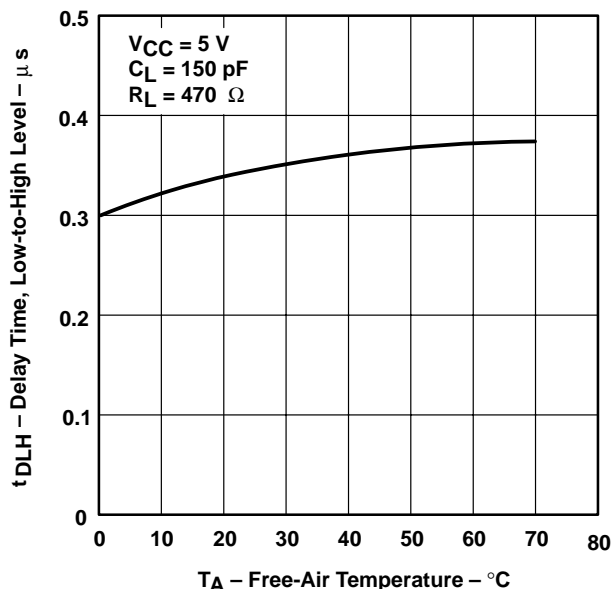


Figure 9

TRANSITION TIME,
HIGH-TO-LOW-LEVEL
vs
FREE-AIR TEMPERATURE

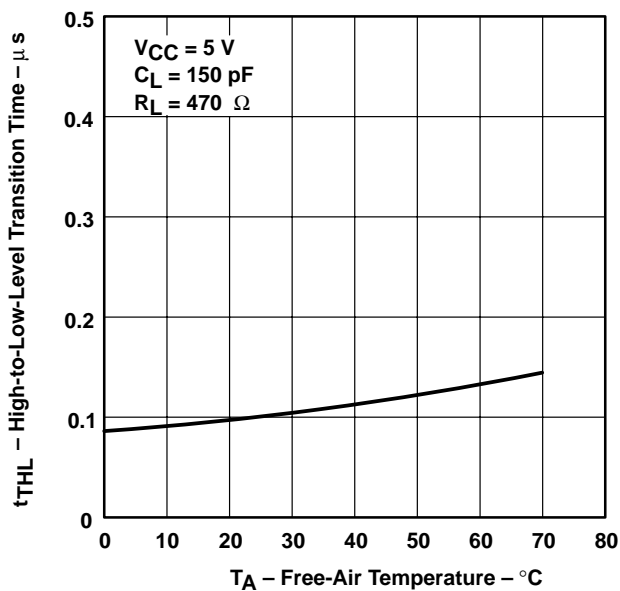


Figure 10

TRANSITION TIME,
LOW-TO-HIGH-LEVEL Q OUTPUT
vs
FREE-AIR TEMPERATURE

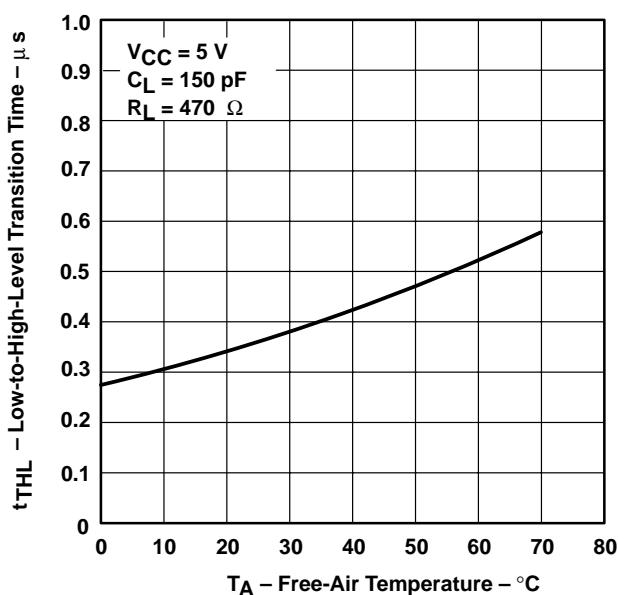


Figure 11

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