

TPIC6273 POWER LOGIC OCTAL D-TYPE LATCH

SLIS011A – APRIL 1992 – REVISED OCTOBER 1995

- Low $r_{DS(on)}$. . . 1.3 Ω Typ
- Avalanche Energy . . . 75 mJ
- Eight Power DMOS Transistor Outputs of 250-mA Continuous Current
- 1.5-A Pulsed Current Per Output
- Output Clamp Voltage up to 45 V
- Low Power Consumption

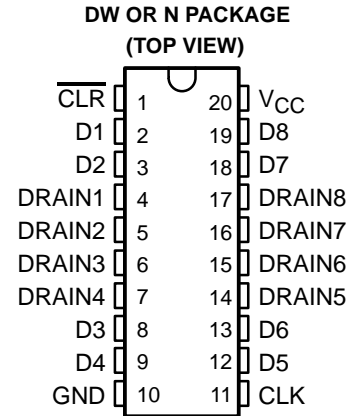
description

The TPIC6273 is a monolithic high-voltage high-current power logic octal D-type latch with DMOS transistor outputs designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

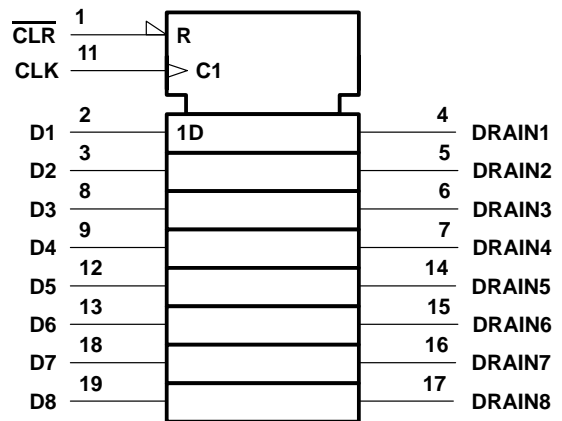
The TPIC6273 contains eight positive-edge-triggered D-type flip-flops with a direct clear input. Each flip-flop features an open-drain power DMOS transistor output.

When clear (\overline{CLR}) is high, information at the D inputs meeting the setup time requirements is transferred to the DRAIN outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input (CLK) is at either the high or low level, the D input signal has no effect at the output. An asynchronous \overline{CLR} is provided to turn all eight DMOS-transistor outputs off.

The TPIC6273 is characterized for operation over the operating case temperature range of -40°C to 125°C .



logic symbol†



† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

**FUNCTION TABLE
(each channel)**

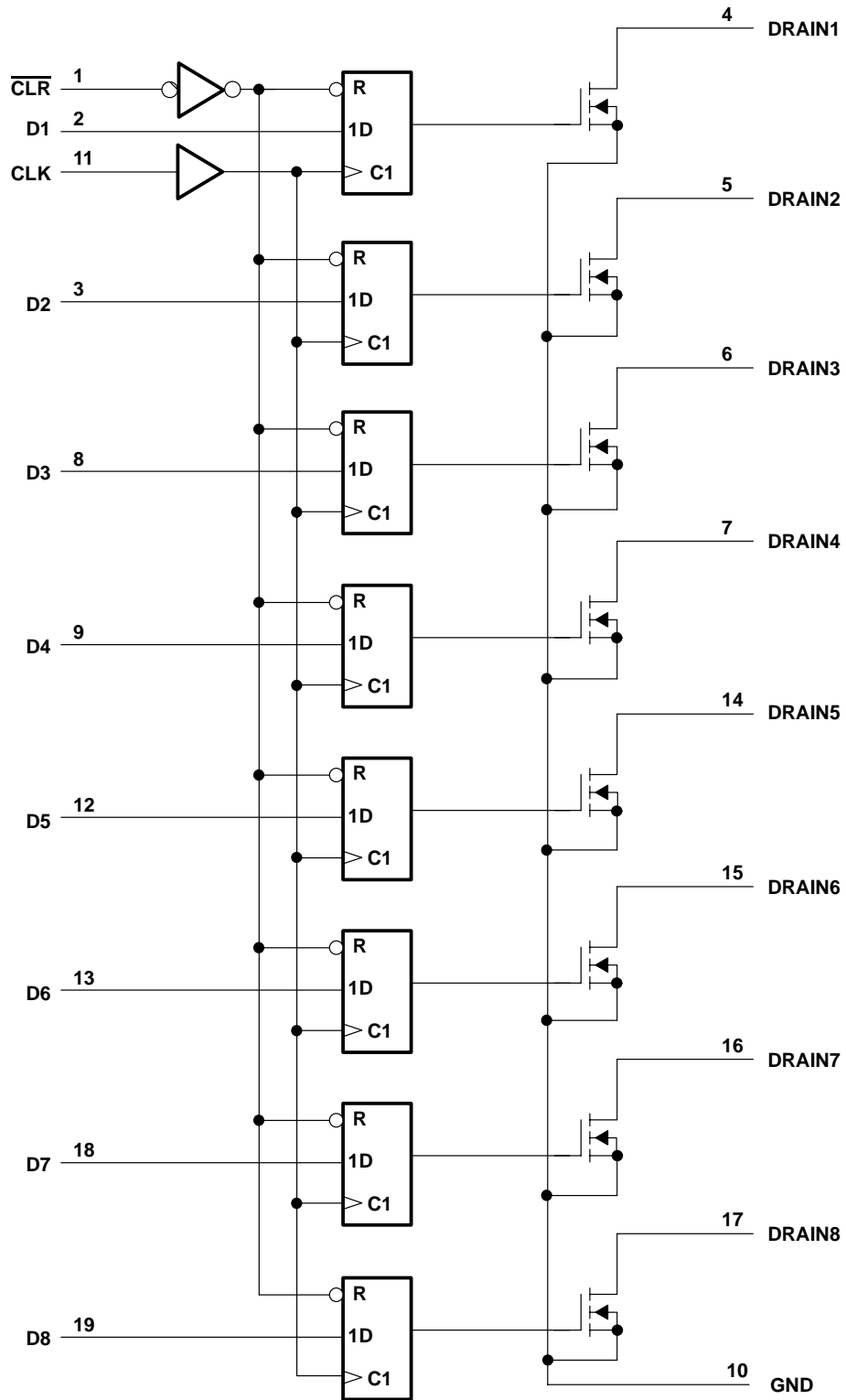
INPUTS			OUTPUT
\overline{CLR}	CLK	D	DRAIN
L	X	X	H
H	\uparrow	H	L
H	\uparrow	L	H
H	L	X	Latched

H = high level, L = low level, X = irrelevant

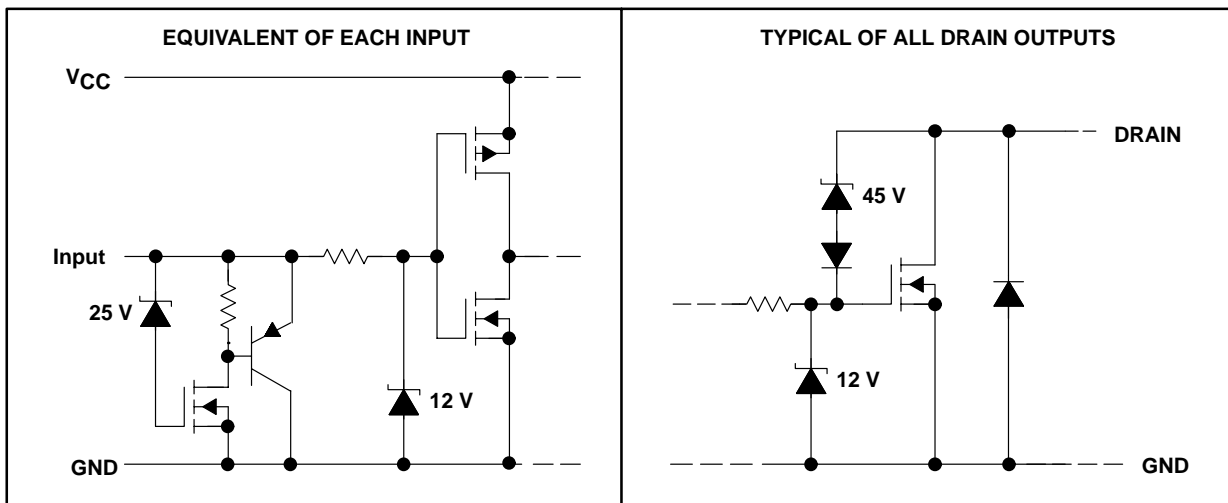
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logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	-0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	45 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current	2 A
Pulsed drain current, each output, all outputs on, I_{Dn} , $T_A = 25^\circ\text{C}$ (see Note 3)	750 mA
Continuous drain current, each output, all outputs on, I_{Dn} , $T_A = 25^\circ\text{C}$	250 mA
Peak drain current single output, I_{DM} , $T_A = 25^\circ\text{C}$ (see Note 3)	2 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	75 mJ
Avalanche current, I_{AS} (see Note 4)	1 A
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	-40°C to 150°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values are with respect to GND.
 2. Each power DMOS source is internally connected to GND.
 3. Pulse duration $\leq 100 \mu\text{s}$, duty cycle $\leq 2\%$
 4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 100 mH, $I_{AS} = 1 \text{ A}$ (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 125^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
N	1150 mW	9.2 mW/°C	230 mW

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recommended operating conditions over recommended operating temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}	0.15 V_{CC}		V
Pulsed drain output current, $T_C = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$ (see Notes 3 and 5)	-1.8	1.5	A
Setup time, D high before $\text{CLK}\uparrow$, t_{su} (see Figure 2)	10		ns
Hold time, D high after $\text{CLK}\uparrow$, t_h (see Figure 2)	15		ns
Pulse duration, t_w (see Figure 2)	25		ns
Operating case temperature, T_C	-40	125	$^\circ\text{C}$

electrical characteristics, $V_{CC} = 5\text{ V}$, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$ Drain-source breakdown voltage	$I_D = 1\text{ mA}$	45			V
V_{SD} Source-drain diode forward voltage	$I_F = 250\text{ mA}$, See Note 3		0.85	1	V
I_{IH} High-level input current	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$			1	μA
I_{IL} Low-level input current	$V_{CC} = 5.5\text{ V}$, $V_I = 0$			-1	μA
I_{CC} Logic supply current	$I_O = 0$, All inputs low		15	100	μA
I_N Nominal current	$V_{DS(on)} = 0.5\text{ V}$, $I_N = I_D$, $T_C = 85^\circ\text{C}$ See Notes 5, 6, and 7		250		mA
I_{DSX} Off-state drain current	$V_{DS} = 40\text{ V}$		0.05	1	μA
	$V_{DS} = 40\text{ V}$, $T_C = 125^\circ\text{C}$		0.15	5	
$r_{DS(on)}$ Static drain-source on-state resistance	$I_D = 250\text{ mA}$, $V_{CC} = 4.5\text{ V}$		1.3	2	Ω
	$I_D = 250\text{ mA}$, $T_C = 125^\circ\text{C}$, $V_{CC} = 4.5\text{ V}$ See Notes 5 and 6 and Figures 8 and 9		2	3.2	
	$I_D = 500\text{ mA}$, $V_{CC} = 4.5\text{ V}$		1.3	2	

switching characteristics, $V_{CC} = 5\text{ V}$, $T_C = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output from CLK	$C_L = 30\text{ pF}$, $I_D = 250\text{ mA}$, See Figures 1, 2, and 10		625		ns
t_{PHL} Propagation delay time, high-to-low-level output from CLK			150		ns
t_r Rise time, drain output			675		ns
t_f Fall time, drain output			400		ns
t_a Reverse-recovery-current rise time	$I_F = 250\text{ mA}$, $di/dt = 20\text{ A}/\mu\text{s}$, See Notes 5 and 6 and Figure 3		100		ns
t_{rr} Reverse-recovery time			300		

- NOTES: 3. Pulse duration $\leq 100\ \mu\text{s}$, duty cycle $\leq 2\%$
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at $T_C = 85^\circ\text{C}$.

thermal resistance

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$ Thermal resistance, junction-to-ambient	DW package		111	$^\circ\text{C}/\text{W}$
	N package	All 8 outputs with equal power	108	



PARAMETER MEASUREMENT INFORMATION

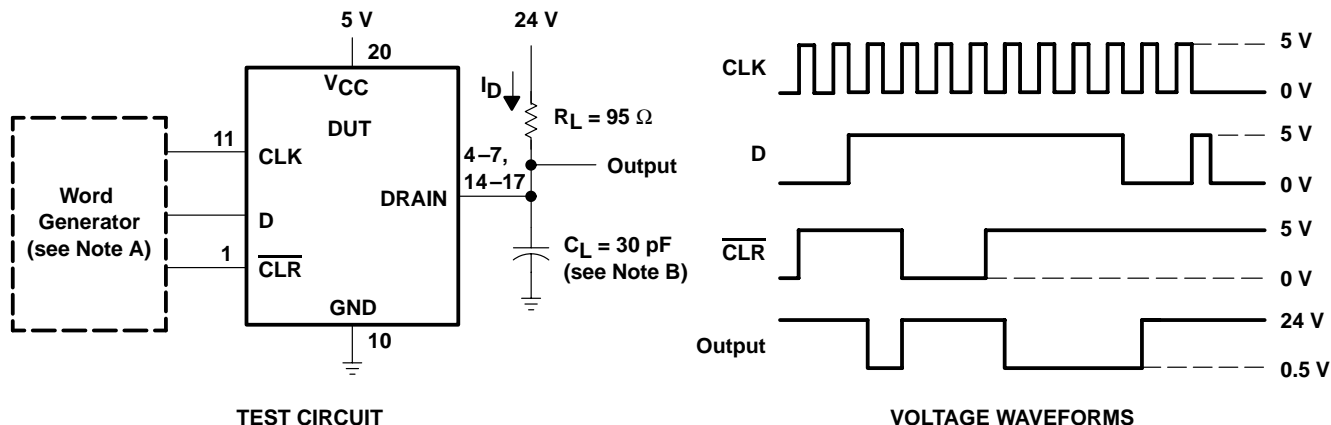


Figure 1. Resistive Load Normal Operation

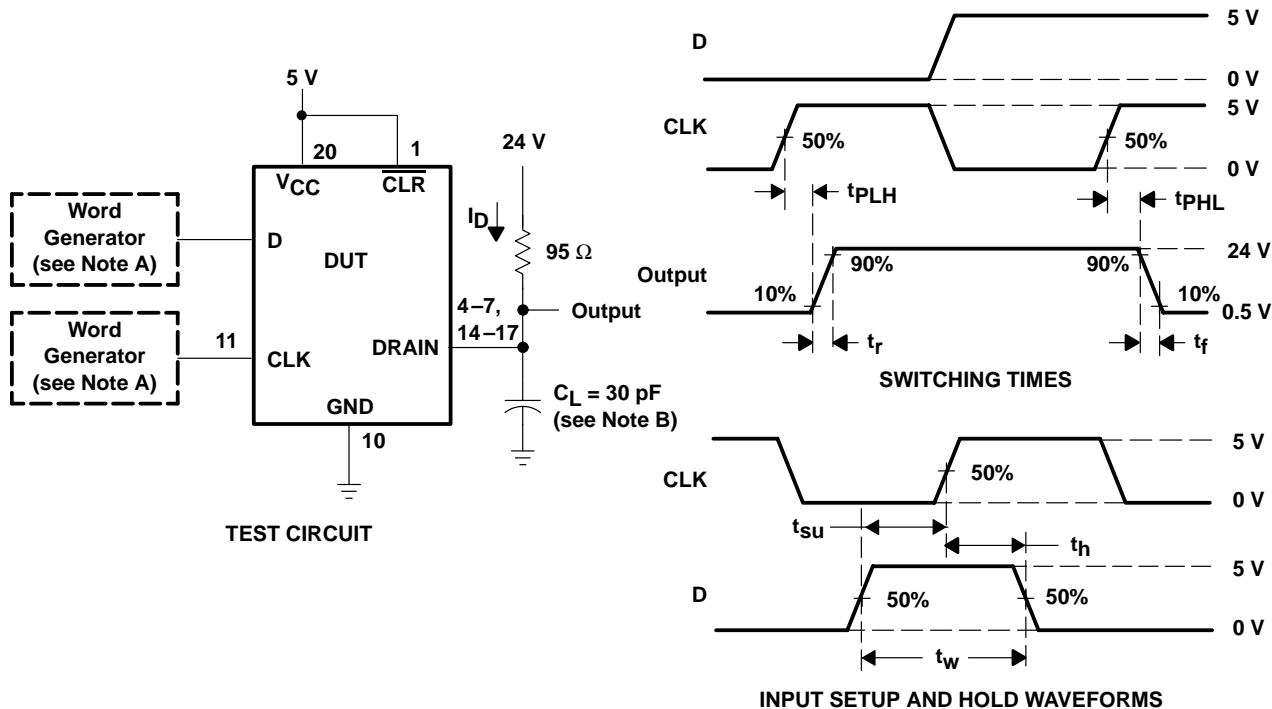


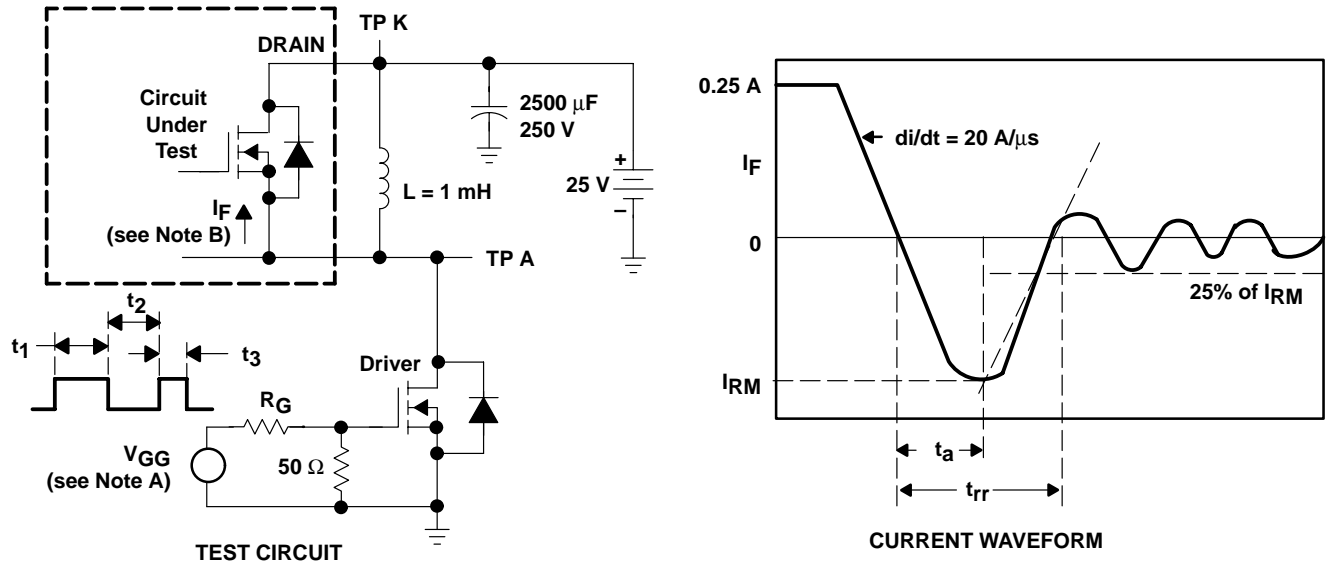
Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

- NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 KHz, $Z_O = 50$ Ω .
B. C_L includes probe and jig capacitance.

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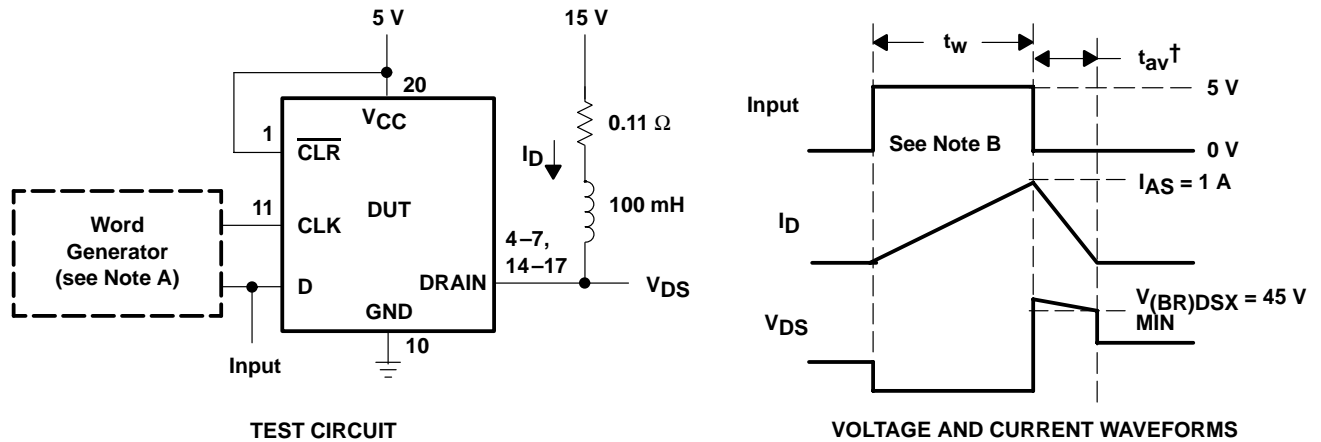
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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The V_{GG} amplitude and R_G are adjusted for $di/dt = 20 \text{ A}/\mu\text{s}$. A V_{GG} double-pulse train is used to set $I_F = 0.25 \text{ A}$, where $t_1 = 10 \mu\text{s}$, $t_2 = 7 \mu\text{s}$, and $t_3 = 3 \mu\text{s}$.
 B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



† Non-JEDEC symbol for avalanche ftime.

- NOTES: A. The word generator A has the following characteristics: $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$, $Z_O = 50 \Omega$.
 B. Input pulse duration, t_w , is increased until peak current $I_{AS} = 1 \text{ A}$.
 Energy test is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 75 \text{ mJ}$, where t_{av} = avalanche time.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

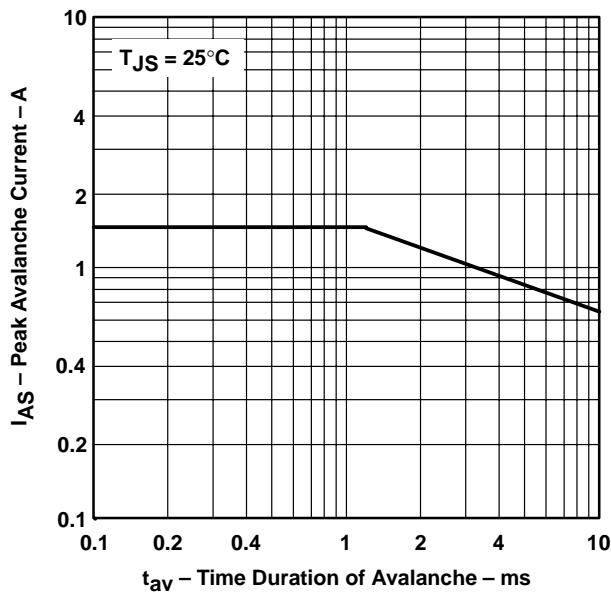


Figure 5

MAXIMUM CONTINUOUS
DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

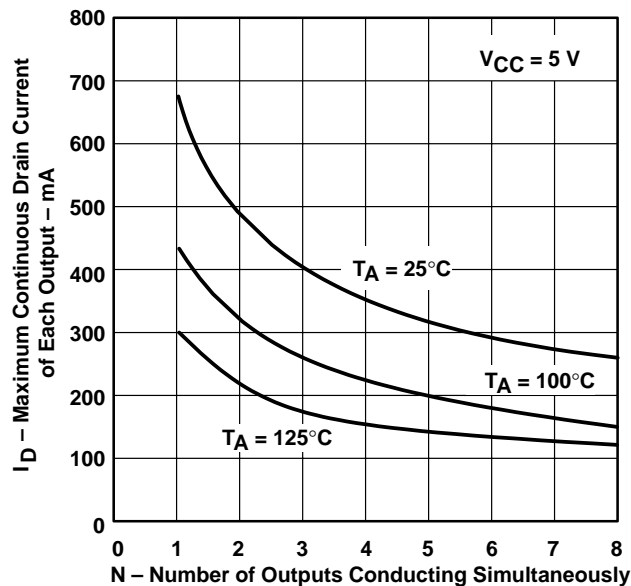


Figure 6

MAXIMUM PEAK DRAIN CURRENT
OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

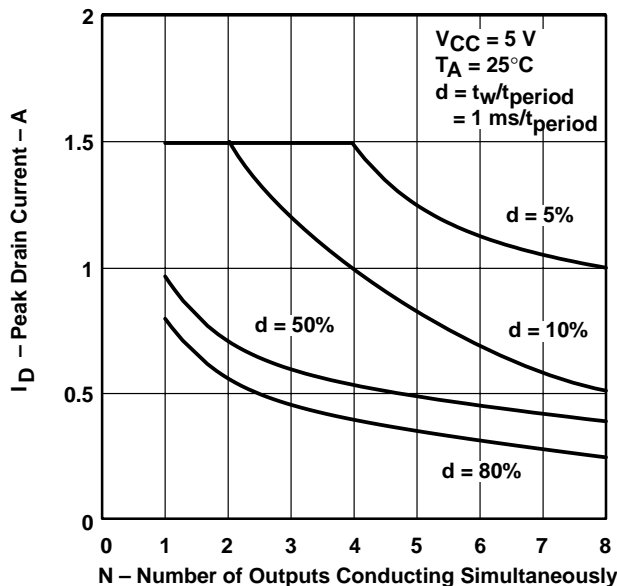
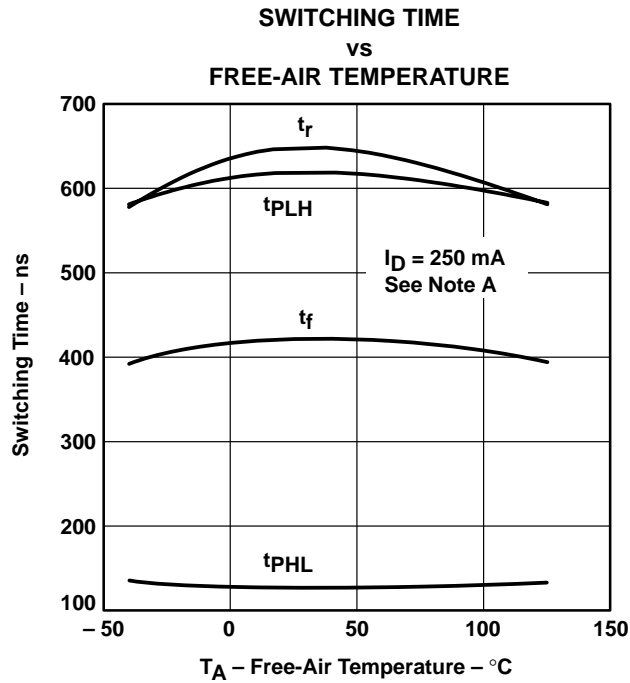
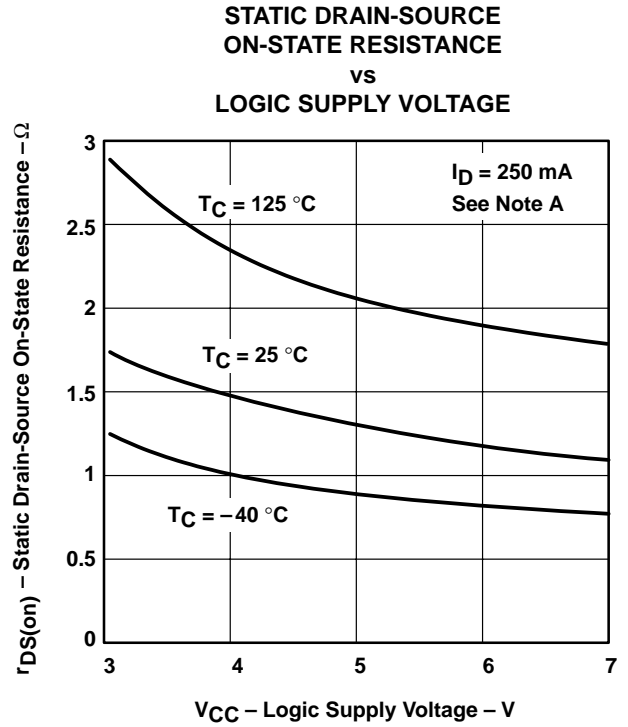
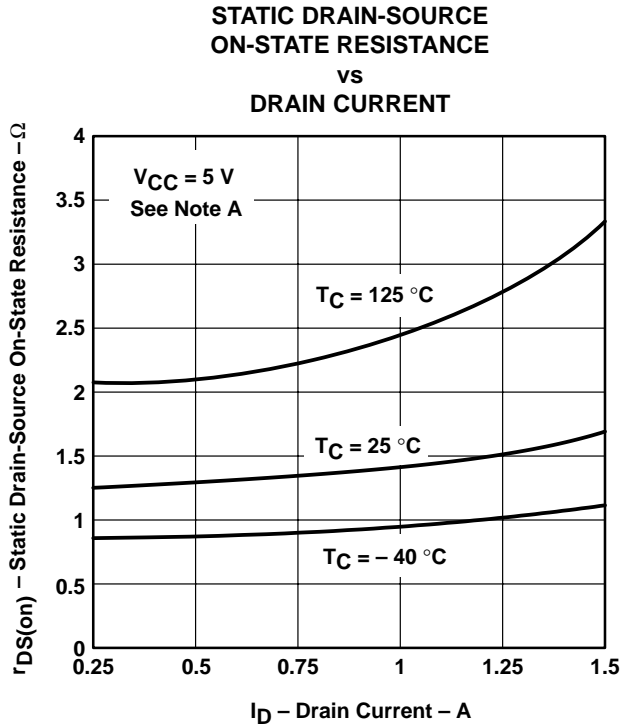


Figure 7

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TYPICAL CHARACTERISTICS



NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

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