- **Low $r_{DS(on)}$ . . . 0.4 Ω Typ**
- **High-Voltage Outputs . . . 60 V**
- **Pulsed Current . . . 5 A Per Channel**
- **Fast Commutation Speed**

D PACKAGE
(TOP VIEW)

SOURCE1	1	8	GATE1
GATE2	2	7	GND
SOURCE2	3	6	DRAIN
SOURCE3	4	5	GATE3
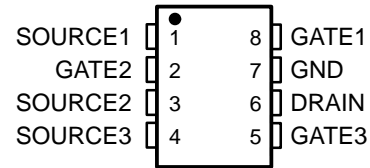
description

The TPIC3302 is a monolithic power DMOS array that consists of three electrically isolated N-channel enhancement-mode DMOS transistors configured with a common drain and open sources. The TPIC3302 is offered in a standard eight-pin small-outline surface-mount (D) package.

The TPIC3302 is characterized for operation over the case temperature range of −40°C to 125°C.

schematic
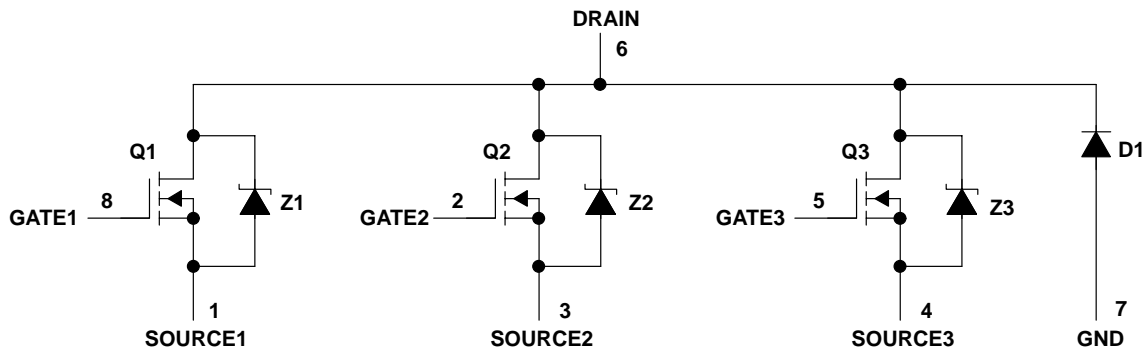
absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage, V_{GS}	±20 V
Continuous drain current, each output, all outputs on, T_C = 25°C	1 A
Continuous source-to-drain diode current	1 A
Pulsed drain current, each output, T_C = 25°C (see Note 1 and Figure 6)	5 A
Single-pulse avalanche energy, T_C = 25°C, E_{AS} (see Figure 4)	9 mJ
Continuous total power dissipation at (or below) T_C = 25°C	0.95 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

TEXAS INSTRUMENTS

TPIC3302
3-CHANNEL COMMON-DRAIN POWER DMOS ARRAY

SLIS021B – APRIL 1994 – REVISED JULY 1995

electrical characteristics, $T_C = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	$I_D = 250\ \mu A$,	$V_{GS} = 0$	60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	$I_D = 1\ mA$,	$V_{DS} = V_{GS}$	1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1)	Drain-to-GND current = 250 μA		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	$I_D = 1\ A$, See Notes 2 and 3	$V_{GS} = 10\ V$,		0.4	0.475	V
V_F	Forward on-state voltage, GND-to-drain	$I_D = 1\ A$, See Notes 2 and 3			2		V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	$I_S = 1\ A$, See Notes 2 and 3	$V_{GS} = 0$,		0.9	1.1	V
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = 48\ V$, $V_{GS} = 0$	$T_C = 25°C$		0.05	1	μA
			$T_C = 125°C$		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	$V_{GS} = 16\ V$,	$V_{DS} = 0$		10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	$V_{SG} = 16\ V$,	$V_{DS} = 0$		10	100	nA
I_{lkg}	Leakage current, drain-to-GND	$V_R = 48\ V$	$T_C = 25°C$		0.05	1	μA
			$T_C = 125°C$		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	$V_{GS} = 10\ V$, $I_D = 1\ A$, See Notes 2 and 3 and Figures 6 and 7	$T_C = 25°C$		0.4	0.475	Ω
			$T_C = 125°C$		0.63	0.7	
g_{fs}	Forward transconductance	$V_{DS} = 10\ V$, See Notes 2 and 3	$I_D = 0.5\ A$,	0.85	1.02		S
C_{iss}	Short-circuit input capacitance, common source				115	145	pF
C_{oss}	Short-circuit output capacitance, common source	$V_{DS} = 25\ V$, f = 1 MHz	$V_{GS} = 0$,		60	75	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				30	40	

NOTES: 2. Technique should limit $T_J – T_C$ to 10°C maximum, pulse duration ≤5 ms.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, $T_C = 25°C$

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{rr(SD)}$	Reverse-recovery time	$I_S = 0.5\ A$,	$V_{GS} = 0$,	$V_{DS} = 48\ V$,		35		ns
Q_{RR}	Total diode charge	di/dt = 100 A/μs,		See Figure 1		0.03		μC

GND-to-drain diode characteristics, $T_C = 25°C$ (see schematic, D1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	$I_F = 0.5\ A$,	$V_{DS} = 48\ V$,		90		ns
Q_{RR}	Total diode charge	di/dt = 100 A/μs,	See Figure 1		0.2		μC

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resistive-load switching characteristics, T_C = 25°C

	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time					21	42	
$t_{d(off)}$	Turn-off delay time	V_{DD} = 25 V,	R_L = 50 Ω,	t_{en} = 10 ns,		20	40	ns
t_r	Rise time	t_{dis} = 10 ns,	See Figure 2			5	10	
t_f	Fall time					13	26	
Q_g	Total gate charge					3.1	3.8	
$Q_{gs(th)}$	Threshold gate-to-source charge	V_{DS} = 48 V, See Figure 3	I_D = 0.5 A,	V_{GS} = 10 V,		0.4	0.5	nC
Q_{gd}	Gate-to-drain charge					1.3	1.6	
L_D	Internal drain inductance					5		
L_S	Internal source inductance					5		nH
R_g	Internal gate resistance					0.25		Ω

thermal resistance

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power, See Note 4		130		°C/W
$R_{\theta JP}$	Junction-to-pin thermal resistance			44		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink
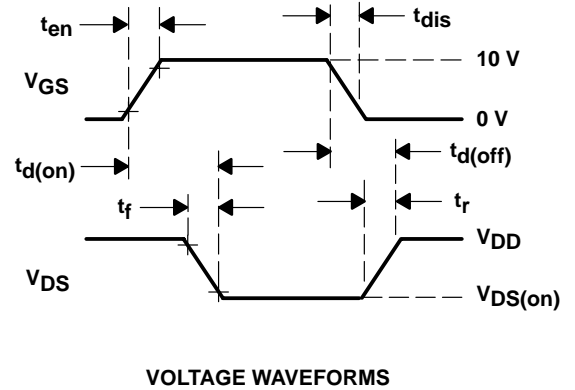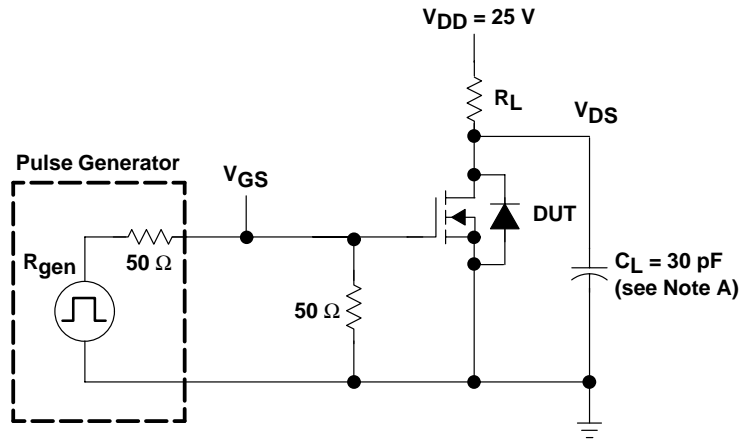
PARAMETER MEASUREMENT INFORMATION
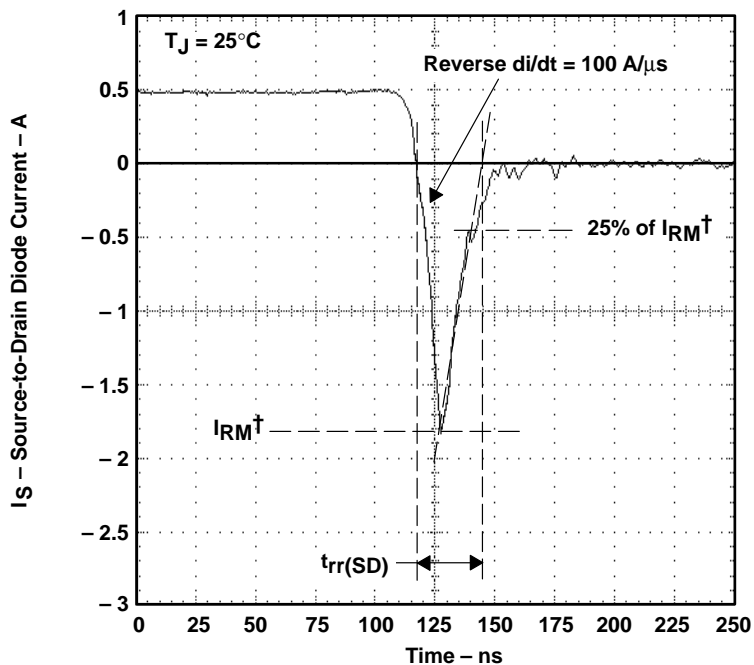
† I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

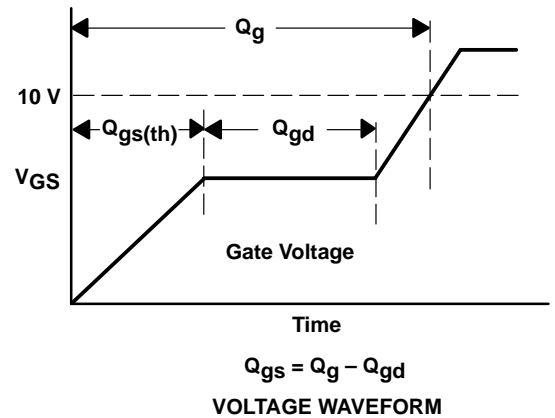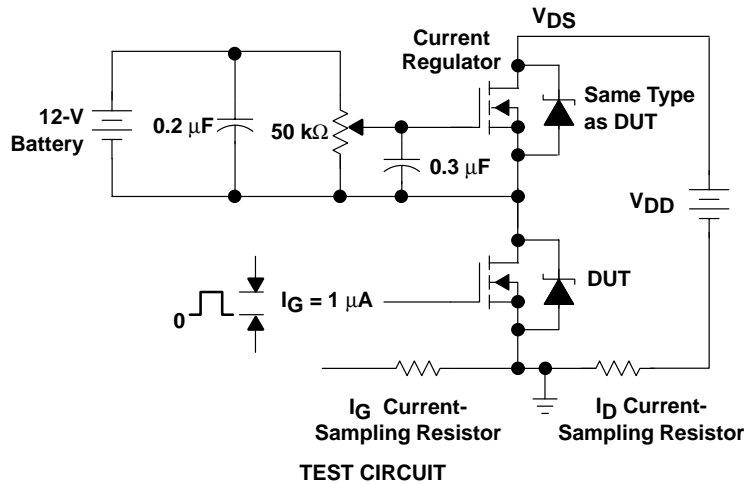## PARAMETER MEASUREMENT INFORMATION

NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

$$Q_{gs} = Q_g - Q_{gd}$$

VOLTAGE WAVEFORM

Figure 3. Gate-Charge Test Circuit and Voltage Waveform

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PARAMETER MEASUREMENT INFORMATION

V_{DD} = 25 V

420 μH

V_{DS}

I_D

Pulse Generator
(see Note A)

V_{GS}

50 Ω

DUT

R_{gen}

50 Ω

TEST CIRCUIT

t_w t_{av}

15 V

V_{GS} 0 V

I_{AS}
(see Note B)

I_D 0 V

$V_{(BR)DSX}$ = 60 V Min

V_{DS}

0 V

VOLTAGE AND CURRENT WAVEFORMS
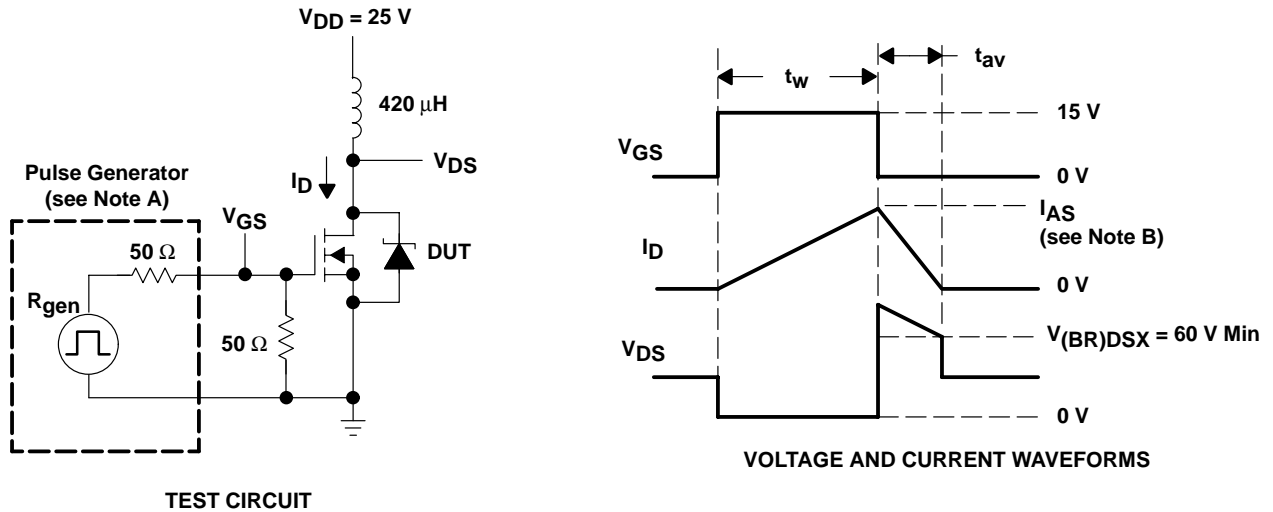
NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.
        B. Input pulse duration (t_w) is increased until peak current I_{AS} = 5 A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 9$ mJ.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms
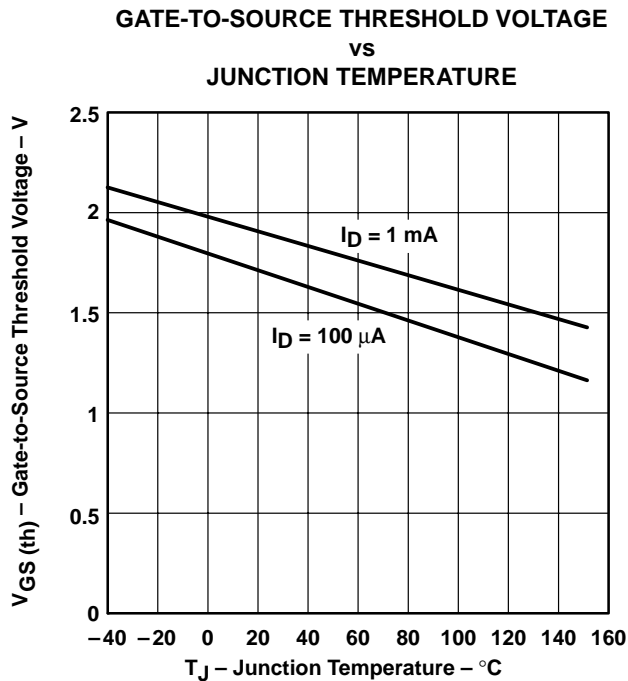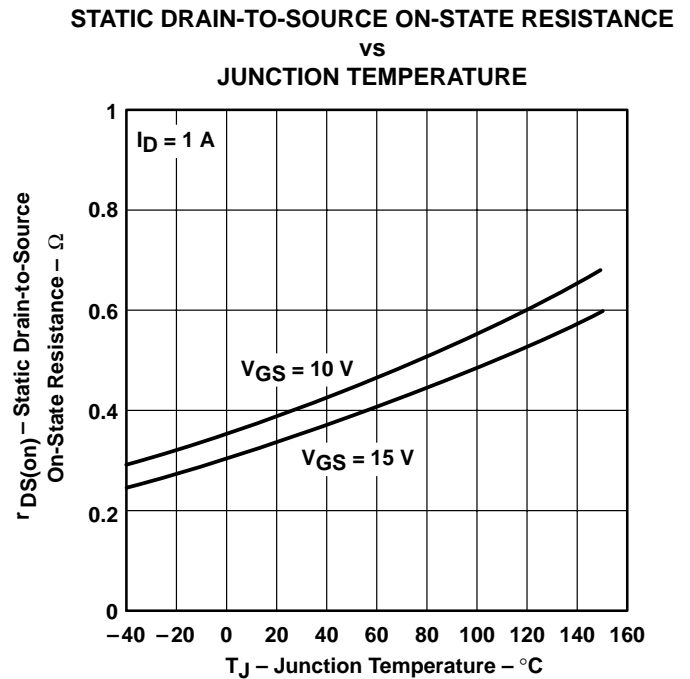
TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

I_D = 1 mA

I_D = 100 μA

$V_{GS(th)}$ – Gate-to-Source Threshold Voltage – V

T_J – Junction Temperature – °C

Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

I_D = 1 A

V_{GS} = 10 V

V_{GS} = 15 V

$r_{DS(on)}$ – Static Drain-to-Source On-State Resistance – Ω

T_J – Junction Temperature – °C

Figure 6

![Texas Instruments logo] **TEXAS INSTRUMENTS**

TYPICAL CHARACTERISTICS

**STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
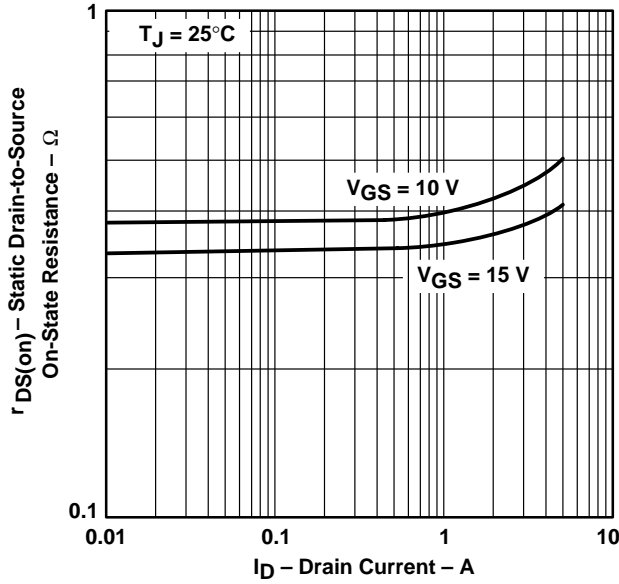vs
DRAIN CURRENT**

Figure 7

**DRAIN CURRENT
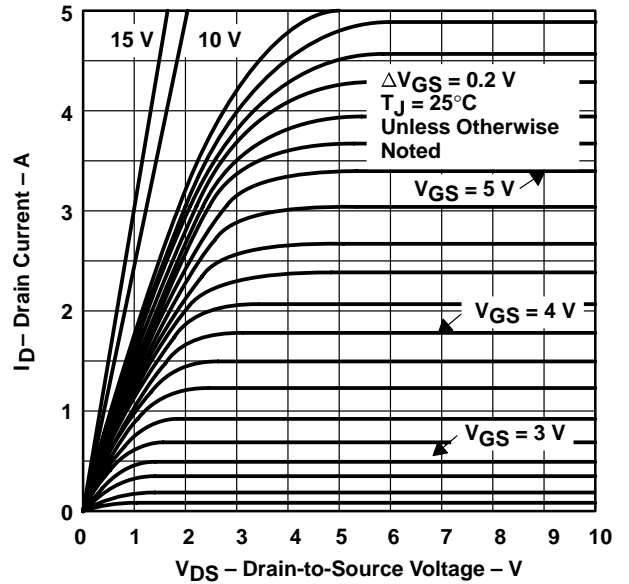vs
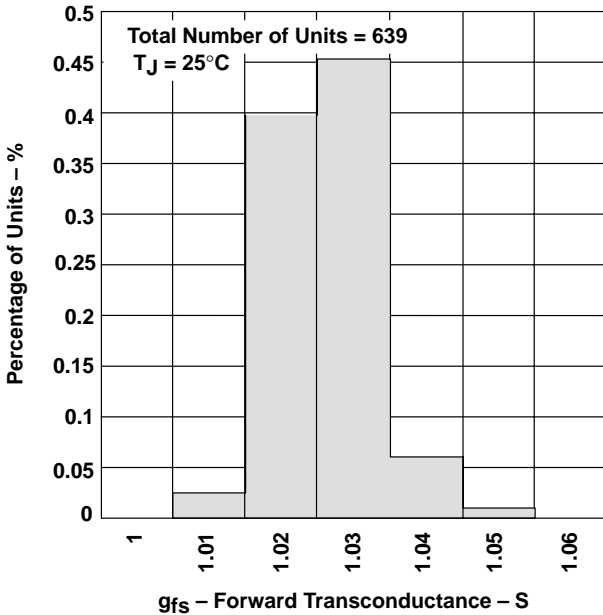DRAIN-TO-SOURCE VOLTAGE**

Figure 8

**DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE**

Figure 9
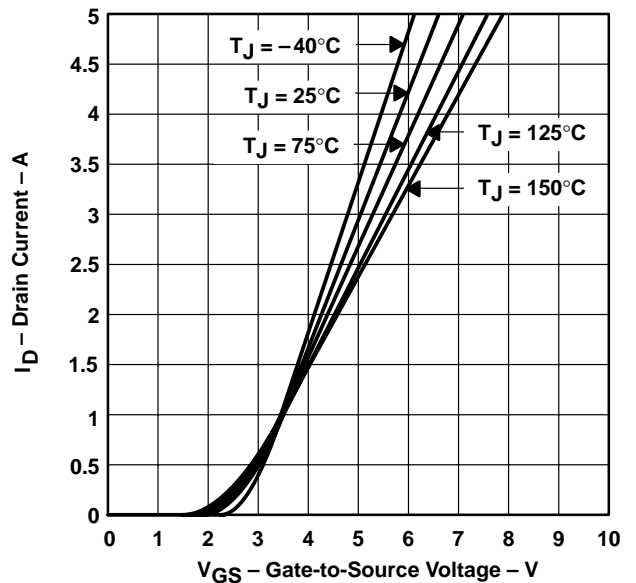
**DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE**

Figure 10

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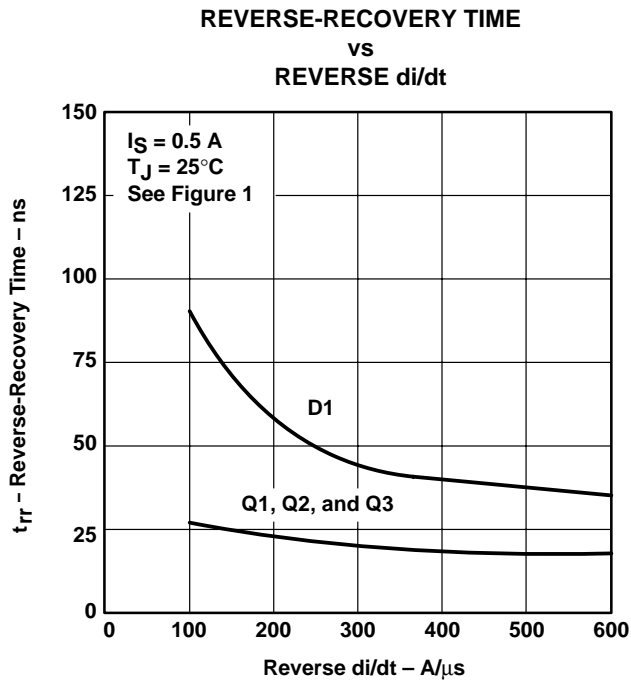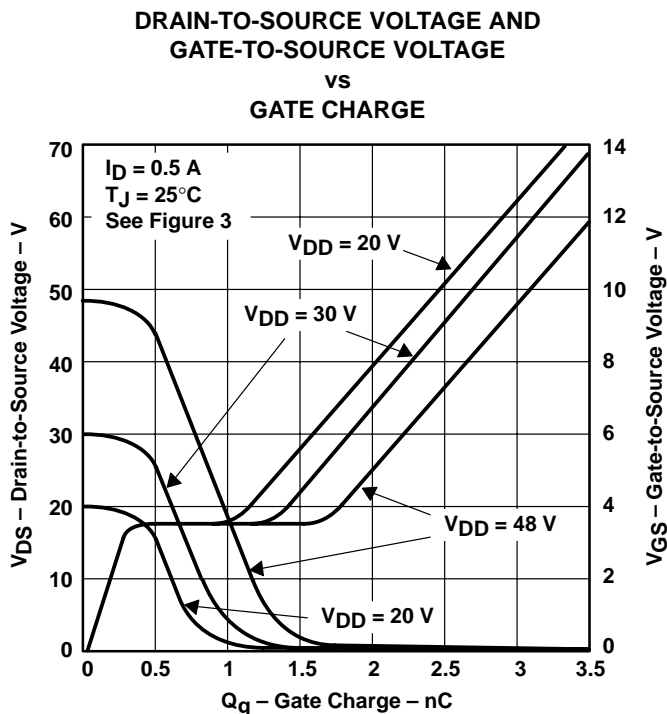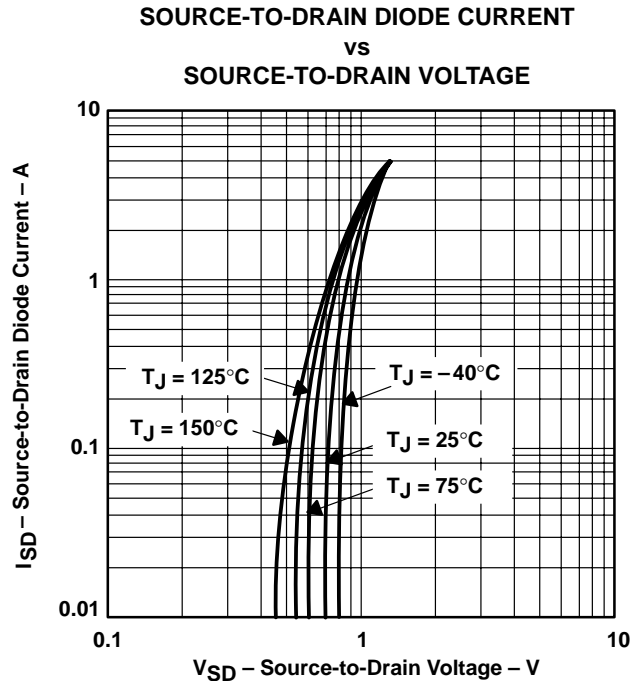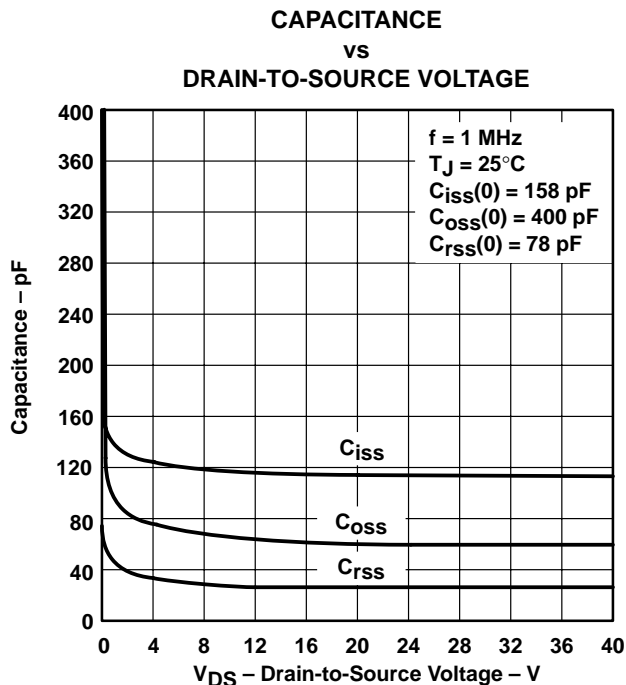
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TYPICAL CHARACTERISTICS

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE

Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

Figure 12

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

Figure 13

REVERSE-RECOVERY TIME
vs
REVERSE di/dt

Figure 14

![Texas Instruments logo]
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THERMAL INFORMATION

**MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE**

$T_C = 25°C$

$1 \mu s†$

$10 ms†$

$1 ms†$

$500 \mu s†$

DC Conditions

I_D – Maximum Drain Current – A

V_{DS} – Drain-to-Source Voltage – V
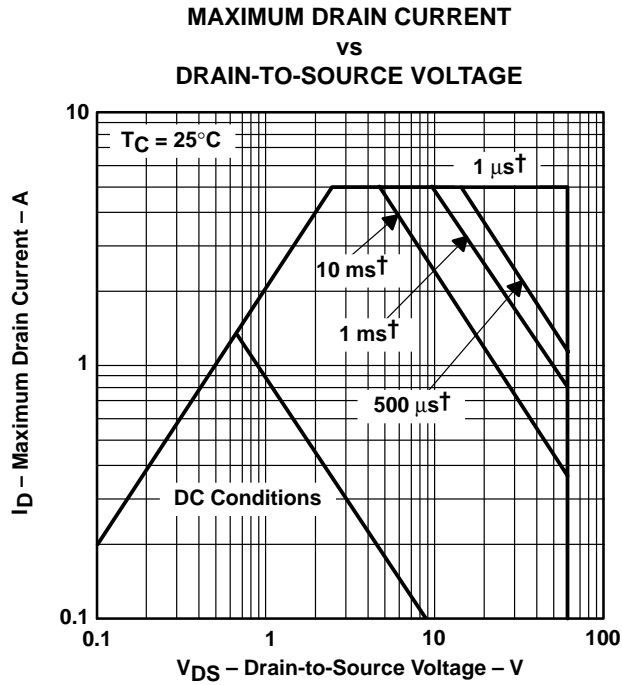
† Less than 0.1 duty cycle

Figure 15

**MAXIMUM PEAK-AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE**

See Figure 4

$T_C = 25°C$

$T_C = 125°C$

I_{AS} – Maximum Peak-Avalanche Current – A

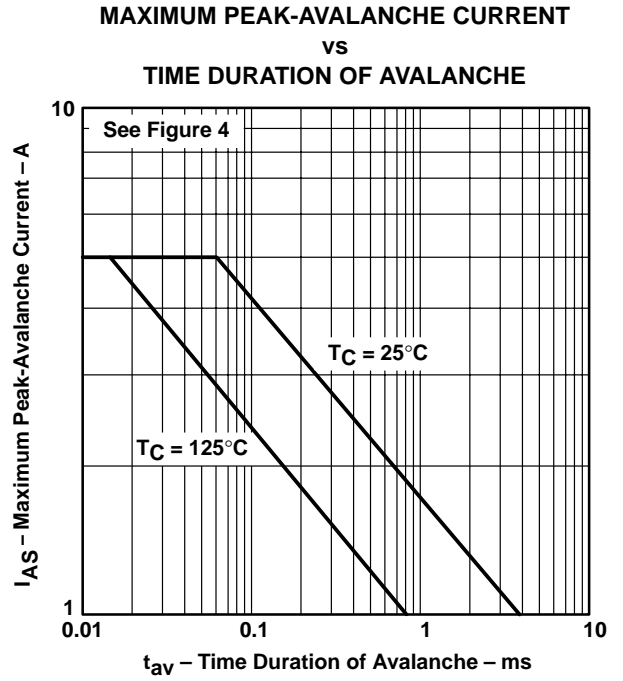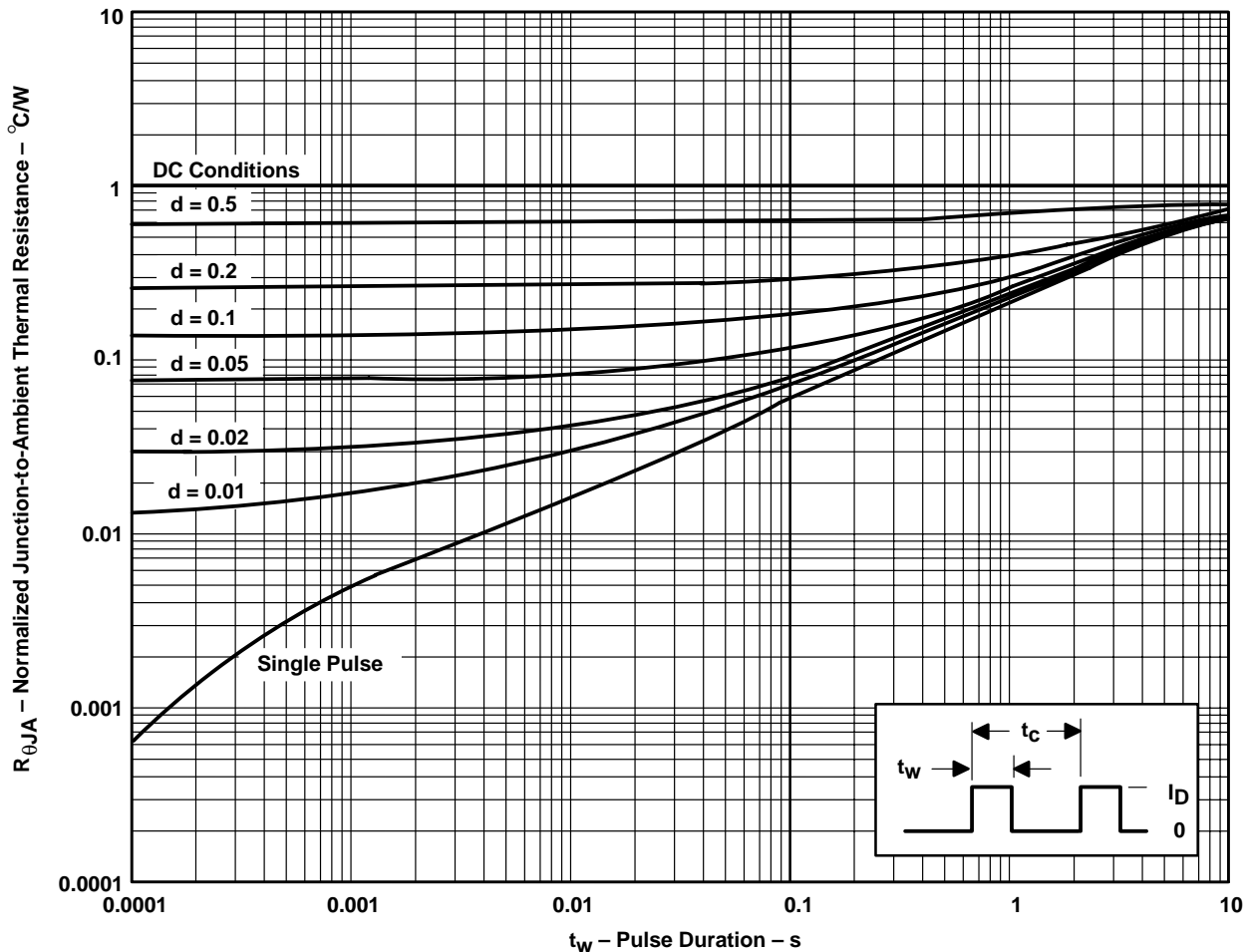t_{av} – Time Duration of Avalanche – ms

Figure 16

THERMAL INFORMATION

D PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION

† Device mounted on FR4 printed-circuit board with no heat sink

NOTES: $Z_{\theta A}(t) = r(t) \, R_{\theta JA}$

   t_W = pulse duration
   t_C = cycle time
   d = duty cycle = t_W/t_C

Figure 17

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