

TPIC5421L H-BRIDGE GATE-PROTECTED LOGIC-LEVEL POWER DMOS ARRAY

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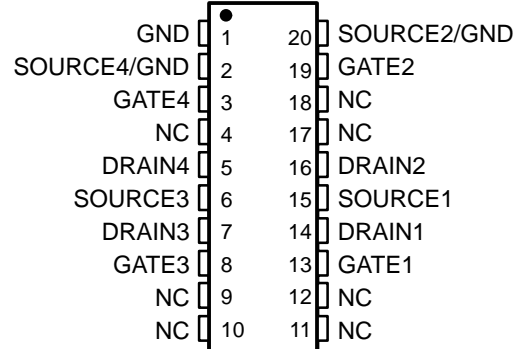
- Low $r_{DS(on)}$. . . 0.4 Ω Typ
- Voltage Output . . . 60 V
- Input Protection Circuitry . . . 18 V
- Pulsed Current . . . 3 A Per Channel
- Extended ESD Capability . . . 4000 V
- Direct Logic-Level Interface

description

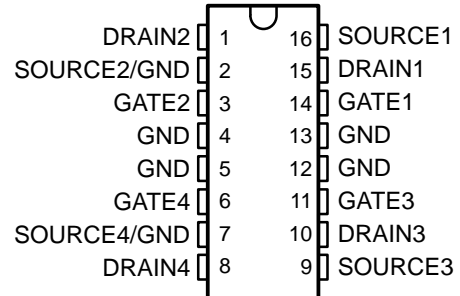
The TPIC5421L is a monolithic gate-protected logic-level power DMOS array that consists of four electrically isolated N-channel enhancement-mode DMOS transistors, two of which are configured with common source. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-k Ω resistor.

The TPIC5421L is offered in a 20-pin wide-body surface-mount (DW) package and a 16-pin thermally-enhanced dual-in-line (NE) package and is characterized for operation over the case temperature of -40°C to 125°C .

DW PACKAGE
(TOP VIEW)

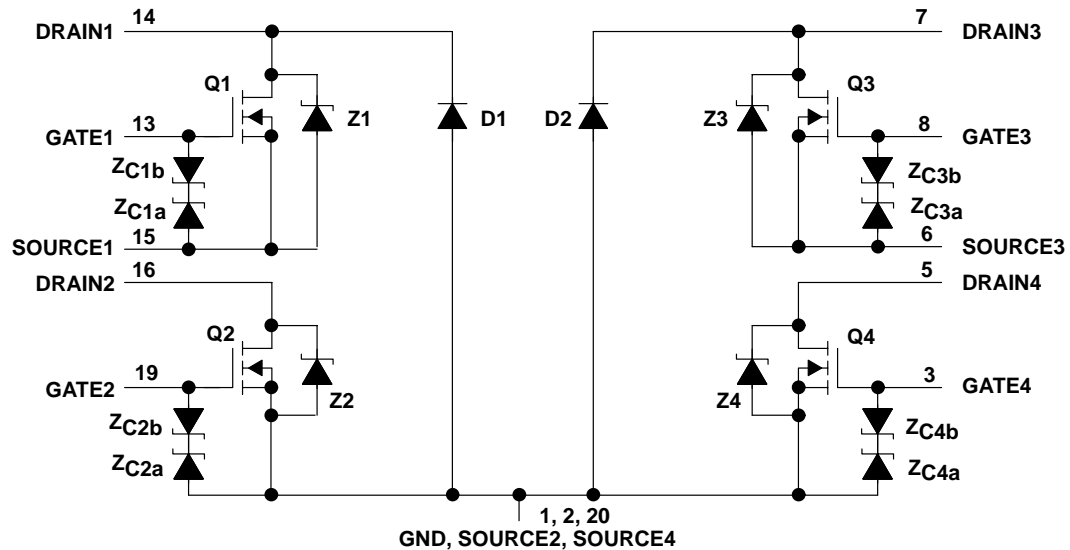


NE PACKAGE
(TOP VIEW)



NC – No internal connection

schematic



NOTE A: For correct operation, no terminal may be taken below GND.
Pin numbers shown are for the DW package.

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absolute maximum ratings over operating case temperature range (unless otherwise noted)[†]

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q1, Q3)	100 V
Drain-to-GND voltage (Q2, Q4)	60 V
Gate-to-source voltage range, V_{GS}	–9 V to 18 V
Continuous drain current, each output, $T_C = 25^\circ\text{C}$: NE package	1.5 A
DW package	1 A
Continuous source-to-drain diode current, $T_C = 25^\circ\text{C}$	1 A
Pulsed drain current, each output, I_{max} , $T_C = 25^\circ\text{C}$ (see Note 1 and Figure 15)	3 A
Continuous gate-to-source zener-diode current, $T_C = 25^\circ\text{C}$	± 50 mA
Pulsed gate-to-source zener-diode current, $T_C = 25^\circ\text{C}$	± 500 mA
Single-pulse avalanche energy, E_{AS} , $T_C = 25^\circ\text{C}$ (see Figures 4 and 16)	180 mJ
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

DISSIPATION RATING TABLE

PACKAGE	$T_C \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25^\circ\text{C}$	$T_C = 125^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
NE	2075 mW	16.6 mW/°C	415 mW

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electrical characteristics, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	$I_D = 250\ \mu\text{A}$,	$V_{GS} = 0$	60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	$I_D = 1\ \text{mA}$, See Figure 5	$V_{DS} = V_{GS}$	1.5	1.85	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	$I_{GS} = 250\ \mu\text{A}$		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	$I_{SG} = 250\ \mu\text{A}$		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND current = $250\ \mu\text{A}$		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	$I_D = 1\ \text{A}$, See Notes 2 and 3	$V_{GS} = 5\ \text{V}$		0.4	0.475	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	$I_S = 1\ \text{A}$, $V_{GS} = 0$ (Z1, Z2, Z3, Z4), See Notes 2 and 3 and Figure 12			0.9	1.1	V
V_F	Forward on-state voltage, GND-to-drain	$I_D = 1\ \text{A}$ (D1, D2), See Notes 2 and 3			4.6		V
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = 48\ \text{V}$, $V_{GS} = 0$	$T_C = 25^\circ\text{C}$		0.05	1	μA
			$T_C = 125^\circ\text{C}$		0.5	10	
I_{GSSF}	Forward-gate current, drain short circuited to source	$V_{GS} = 15\ \text{V}$,	$V_{DS} = 0$		20	200	nA
I_{GSSR}	Reverse-gate current, drain short circuited to source	$V_{SG} = 5\ \text{V}$,	$V_{DS} = 0$		10	100	nA
I_{lkg}	Leakage current, drain-to-GND	$V_{DGND} = 48\ \text{V}$	$T_C = 25^\circ\text{C}$		0.05	1	μA
			$T_C = 125^\circ\text{C}$		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	$V_{GS} = 5\ \text{V}$, $I_D = 1\ \text{A}$, See Notes 2 and 3 and Figures 6 and 7	$T_C = 25^\circ\text{C}$		0.4	0.475	Ω
			$T_C = 125^\circ\text{C}$		0.65	0.68	
g_{fs}	Forward transconductance	$V_{DS} = 15\ \text{V}$, See Notes 2 and 3 and Figure 9	$I_D = 0.5\ \text{A}$	1.25	1.4		S
C_{iss}	Short-circuit input capacitance, common source	$V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$,	$V_{GS} = 0$, See Figure 11		220	275	pF
C_{oss}	Short-circuit output capacitance, common source				120	150	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				100	125	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.

3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{rr}	Reverse-recovery time	I _S = 0.5 A, V _{GS} = 0, See Figures 1 and 14	V _{DS} = 48 V, di/dt = 100 A/μs,	Z1 and Z3	55		ns
				Z2 and Z4	150		
				D1 and D2	200		
Q _{RR}	Total diode charge			Z1 and Z3	0.06		μC
				Z2 and Z4	0.3		
				D1 and D2	0.7		

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resistive-load switching characteristics, $T_C = 25^\circ\text{C}$

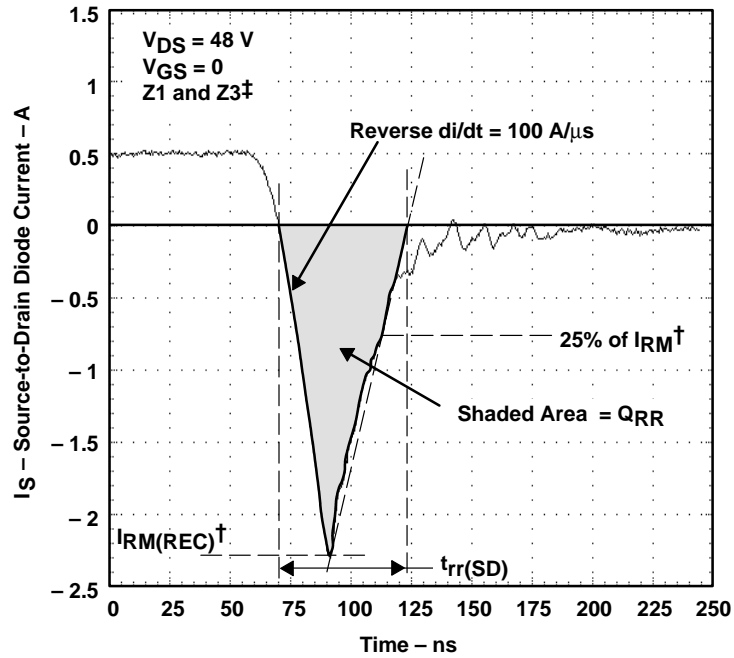
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 25\text{ V},$ $R_L = 25\ \Omega,$ $t_{r1} = 10\text{ ns},$ See Figure 2		25	50	ns
$t_{d(off)}$	Turn-off delay time			20	40	
t_{r2}	Rise time			21	42	
t_{f2}	Fall time			9	18	
Q_g	Total gate charge	$V_{DS} = 48\text{ V},$ See Figure 3 $I_D = 0.5\text{ A},$ $V_{GS} = 5\text{ V},$		3.9	5	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.55	0.8	
Q_{gd}	Gate-to-drain charge			2.5	3.6	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	DW package	See Notes 4 and 6	90		$^\circ\text{C/W}$
		NE package		60		
$R_{\theta JB}$	Junction-to-board thermal resistance	DW package	See Notes 4 and 6	53		
$R_{\theta JP}$	Junction-to-pin thermal resistance	DW package	See Notes 5 and 6	30		
		NE package		25		

NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.
5. Package mounted in intimate contact with infinite heatsink.
6. All outputs with equal power

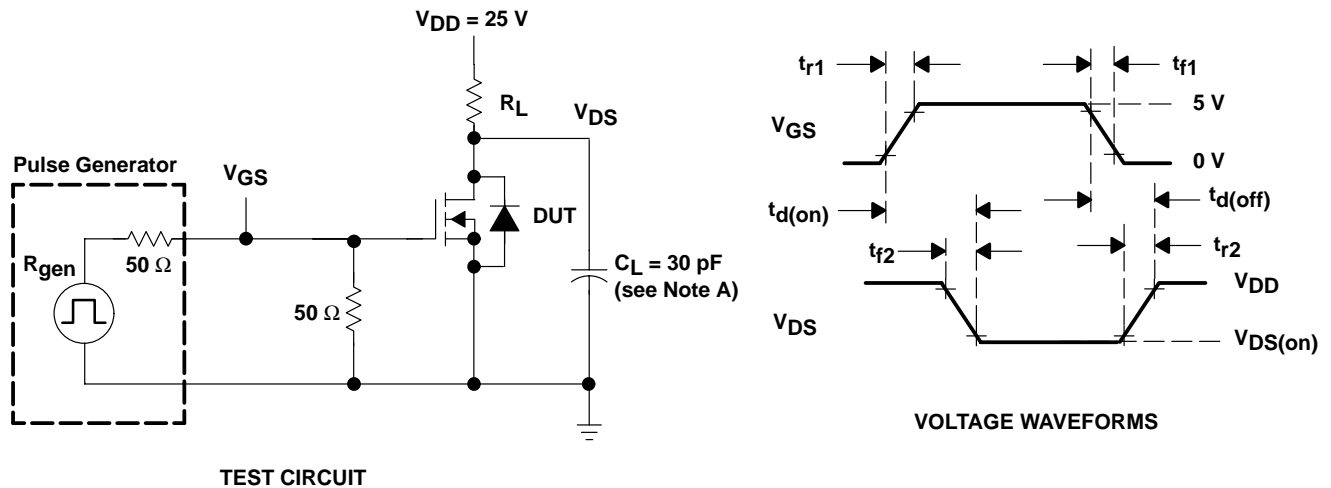
PARAMETER MEASUREMENT INFORMATION



† $I_{RM(REC)}$ = maximum recovery current

‡ The above waveform is representative of Z2, Z4, D1, and D2 in shape only.

Figure 1. Reverse-Recovery-Current Waveforms of Source-to-Drain Diode



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION

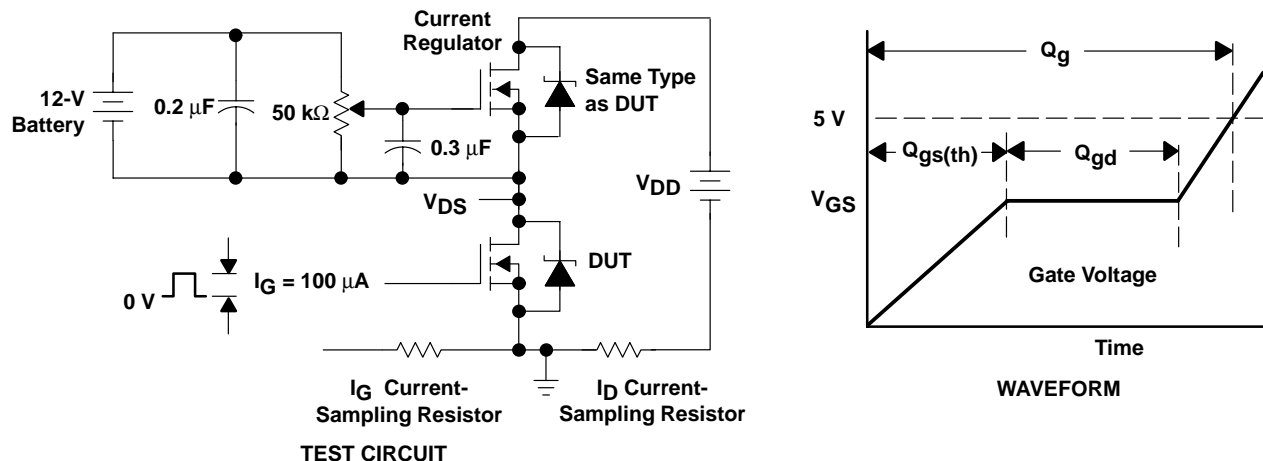
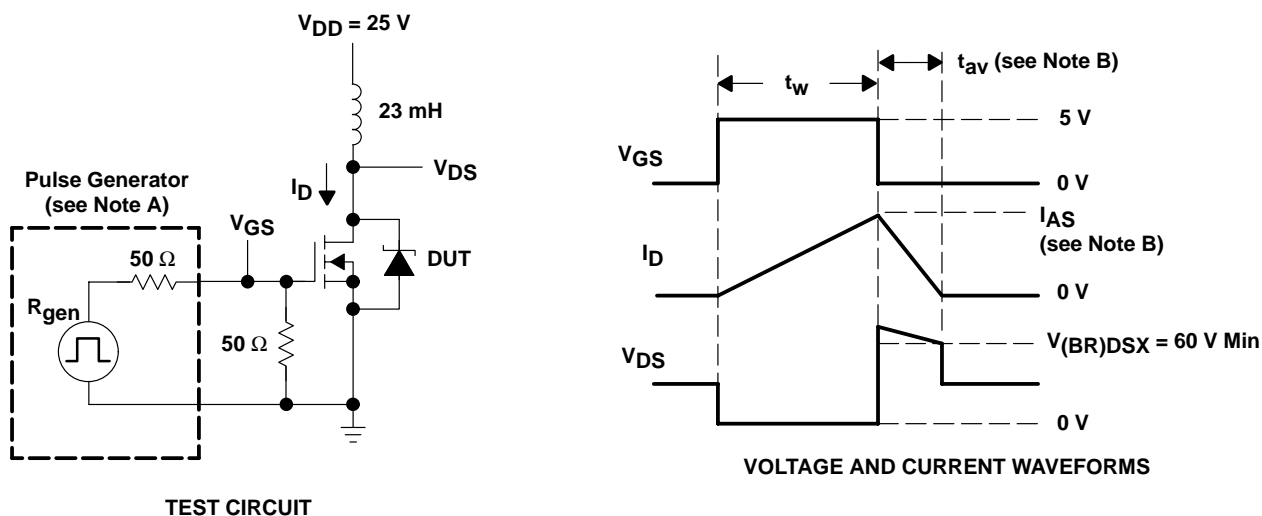


Figure 3. Gate-Charge Test Circuit and Waveform



- NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_0 = 50 \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 3$ A.

$$\text{Energy test level is defined as } E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 180 \text{ mJ,}$$

where t_{av} = avalanche time

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

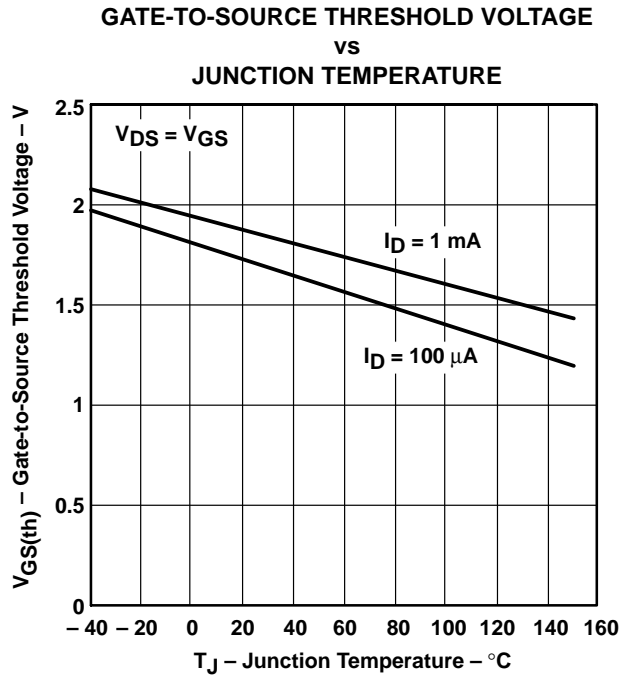


Figure 5

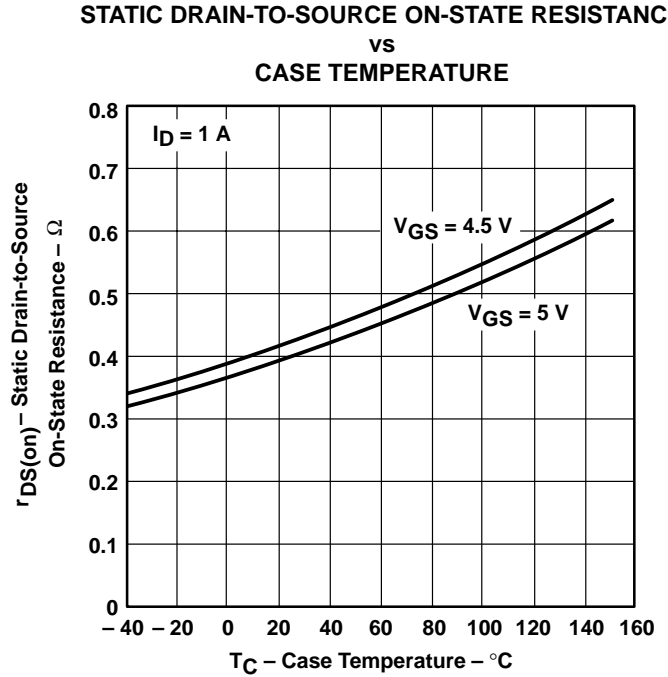


Figure 6

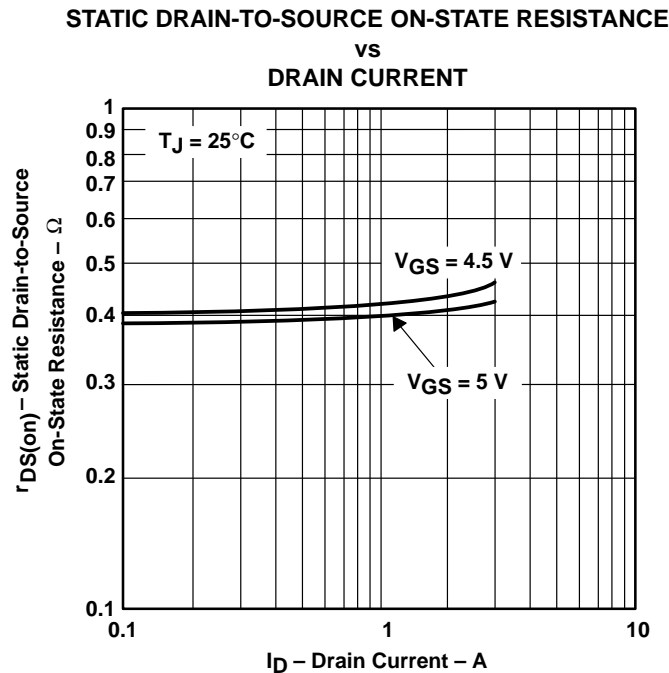


Figure 7

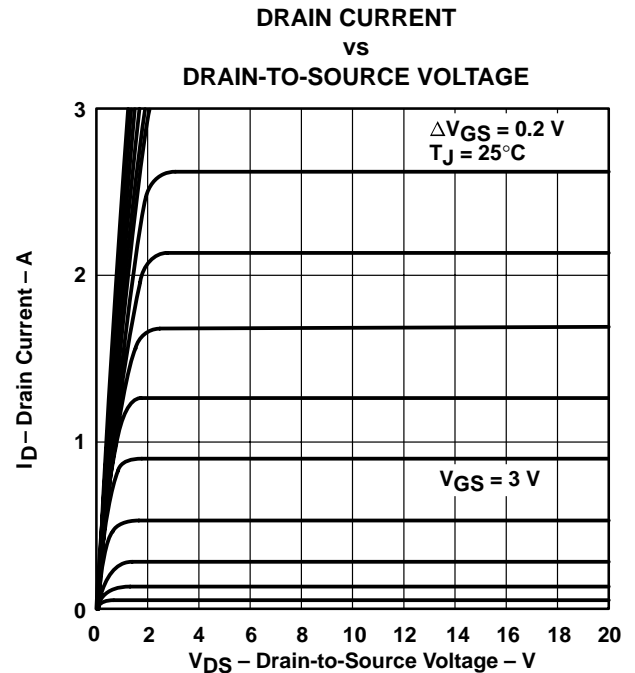


Figure 8

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TYPICAL CHARACTERISTICS

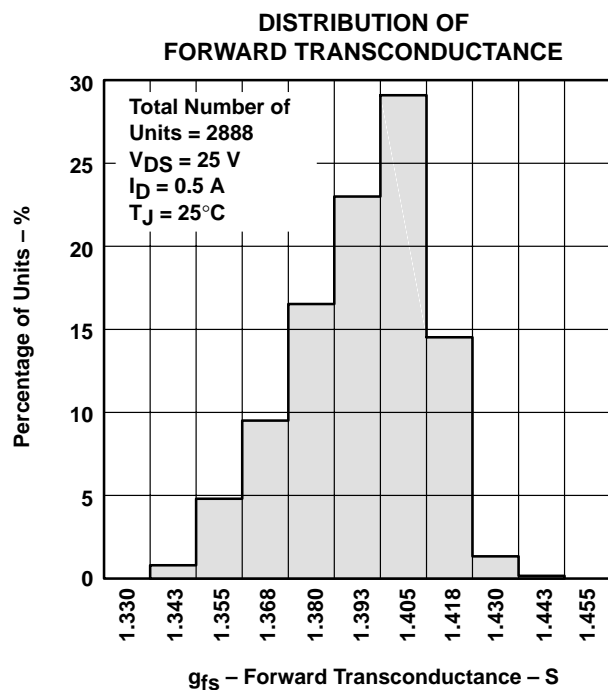


Figure 9

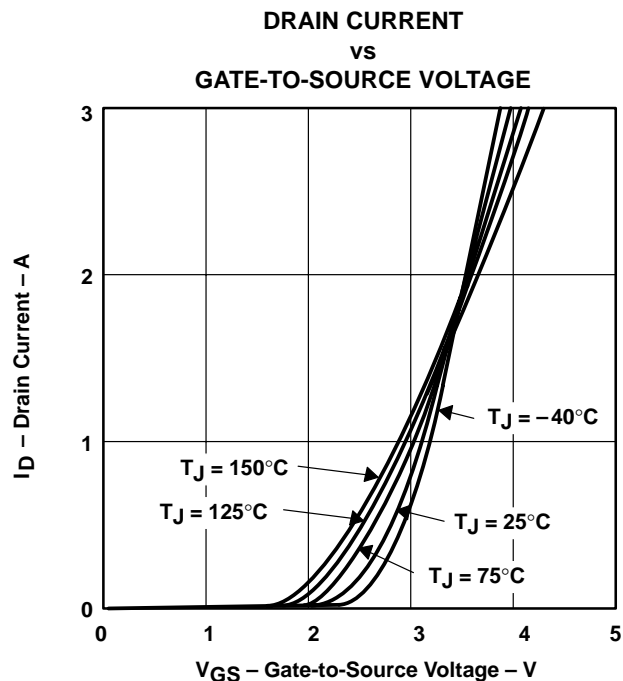


Figure 10

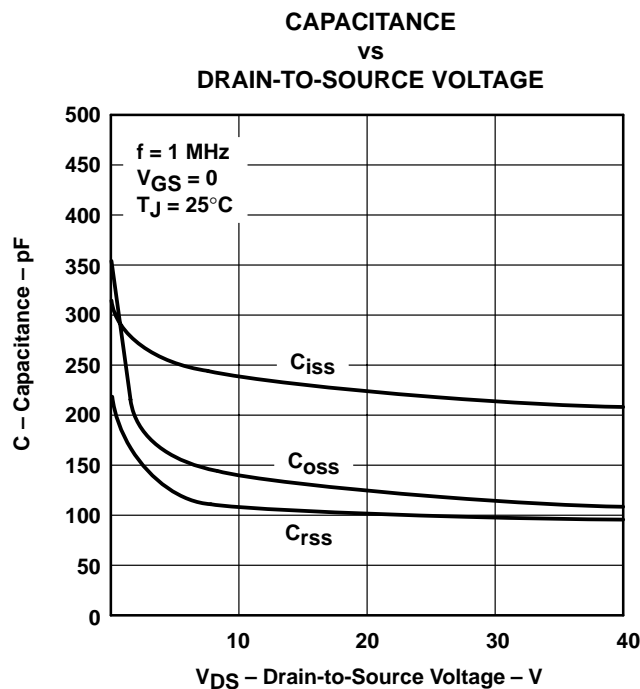


Figure 11

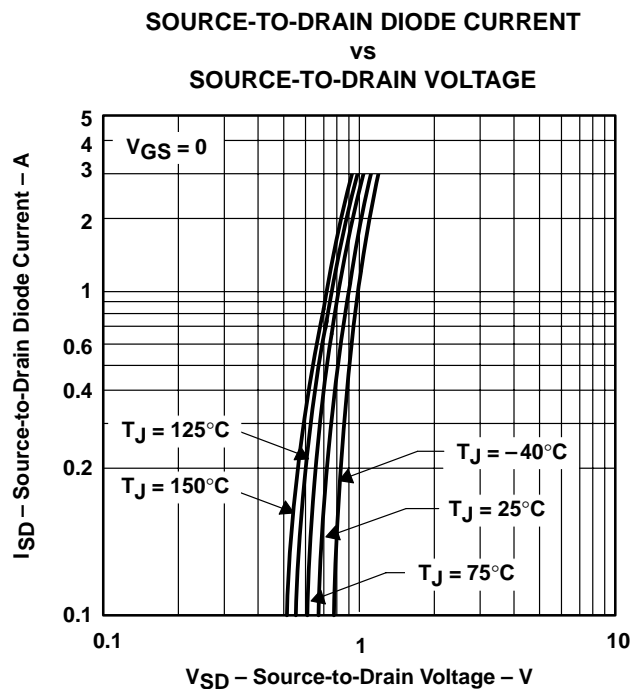


Figure 12

TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE

vs
GATE CHARGE

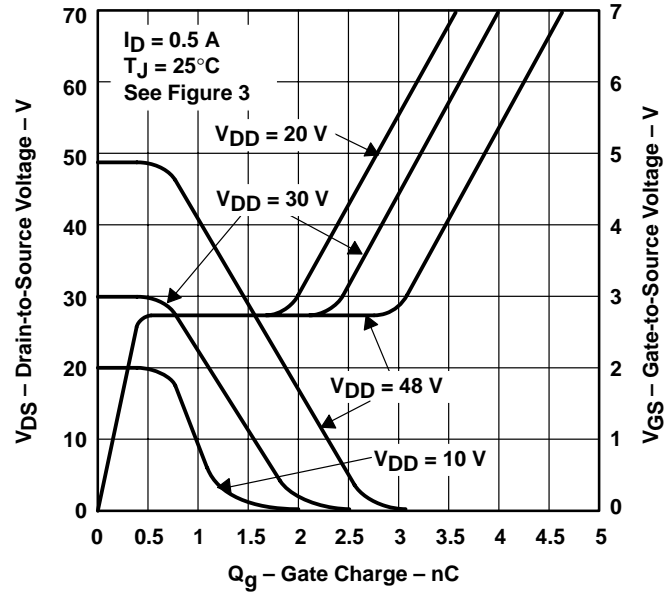


Figure 13

REVERSE-RECOVERY TIME

vs
REVERSE di/dt

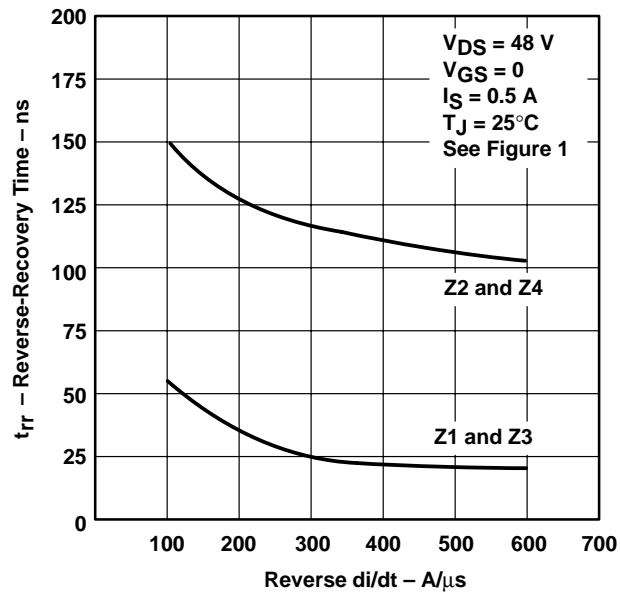


Figure 14

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THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

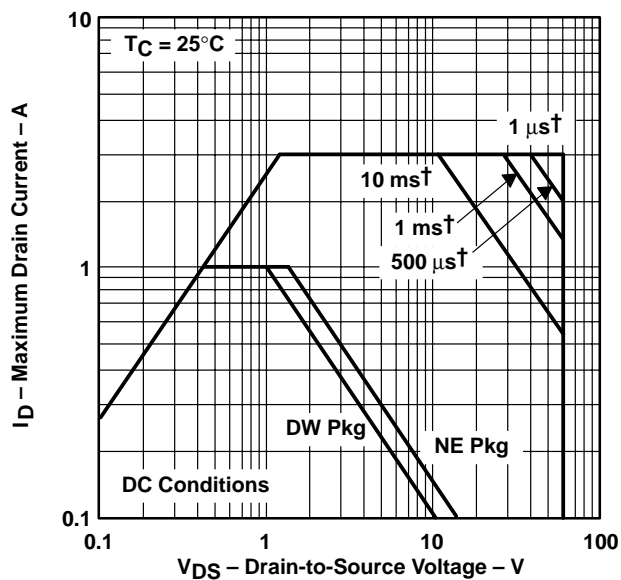


Figure 15

MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

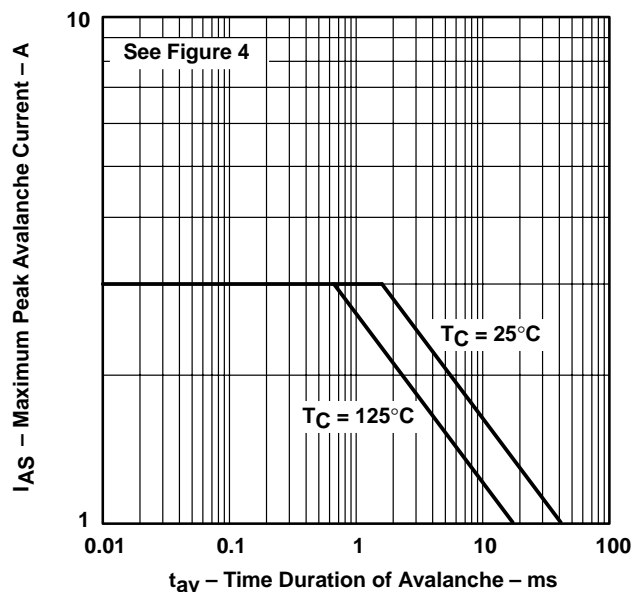
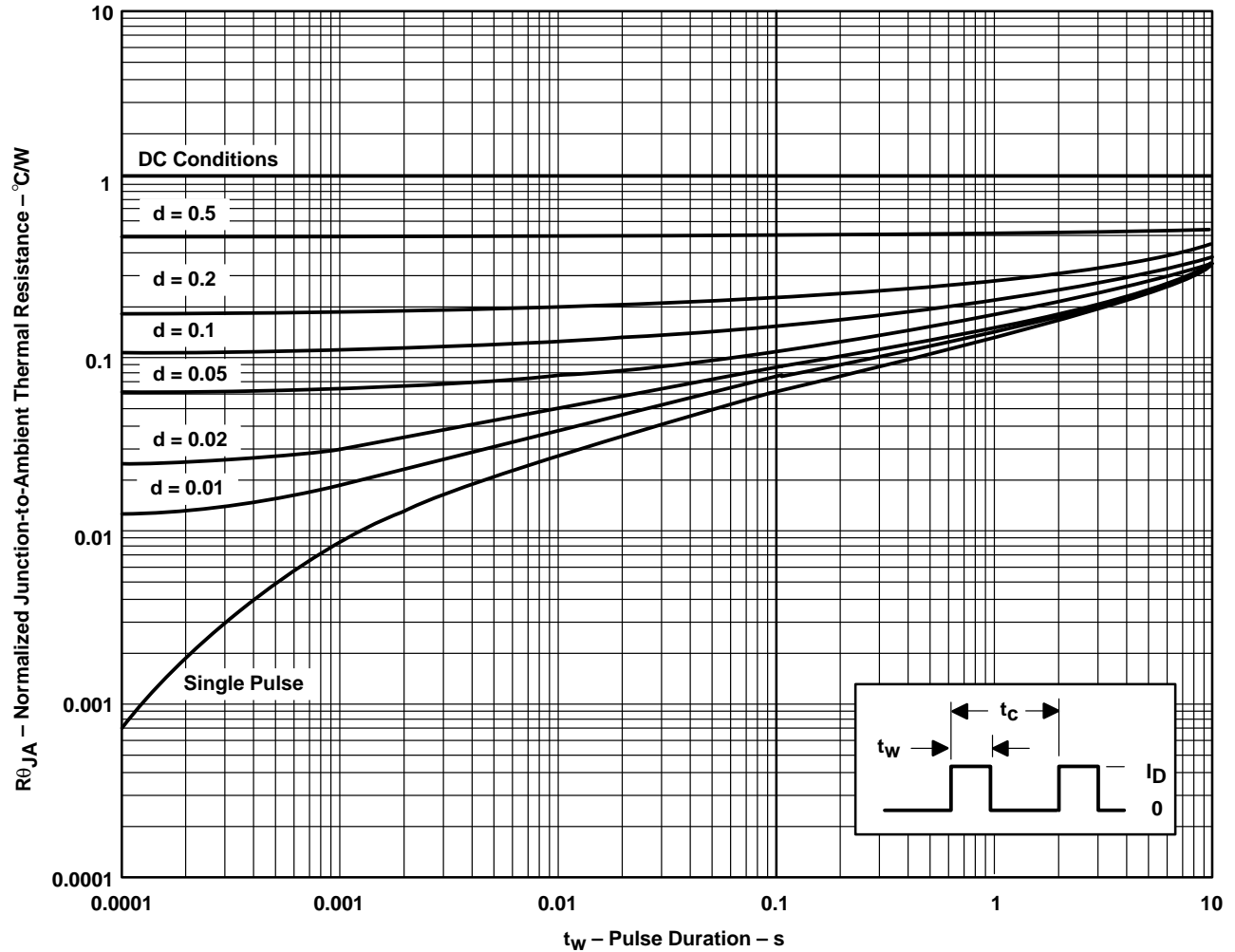


Figure 16

THERMAL INFORMATION

NE PACKAGE† NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE vs PULSE DURATION



† Device mounted on FR4 printed-circuit board with no heatsink.

NOTES A: $Z_{\theta JA}(t) = r(t) R_{\theta JA}$
 t_w = pulse duration
 t_c = cycle time
 d = duty cycle = t_w/t_c

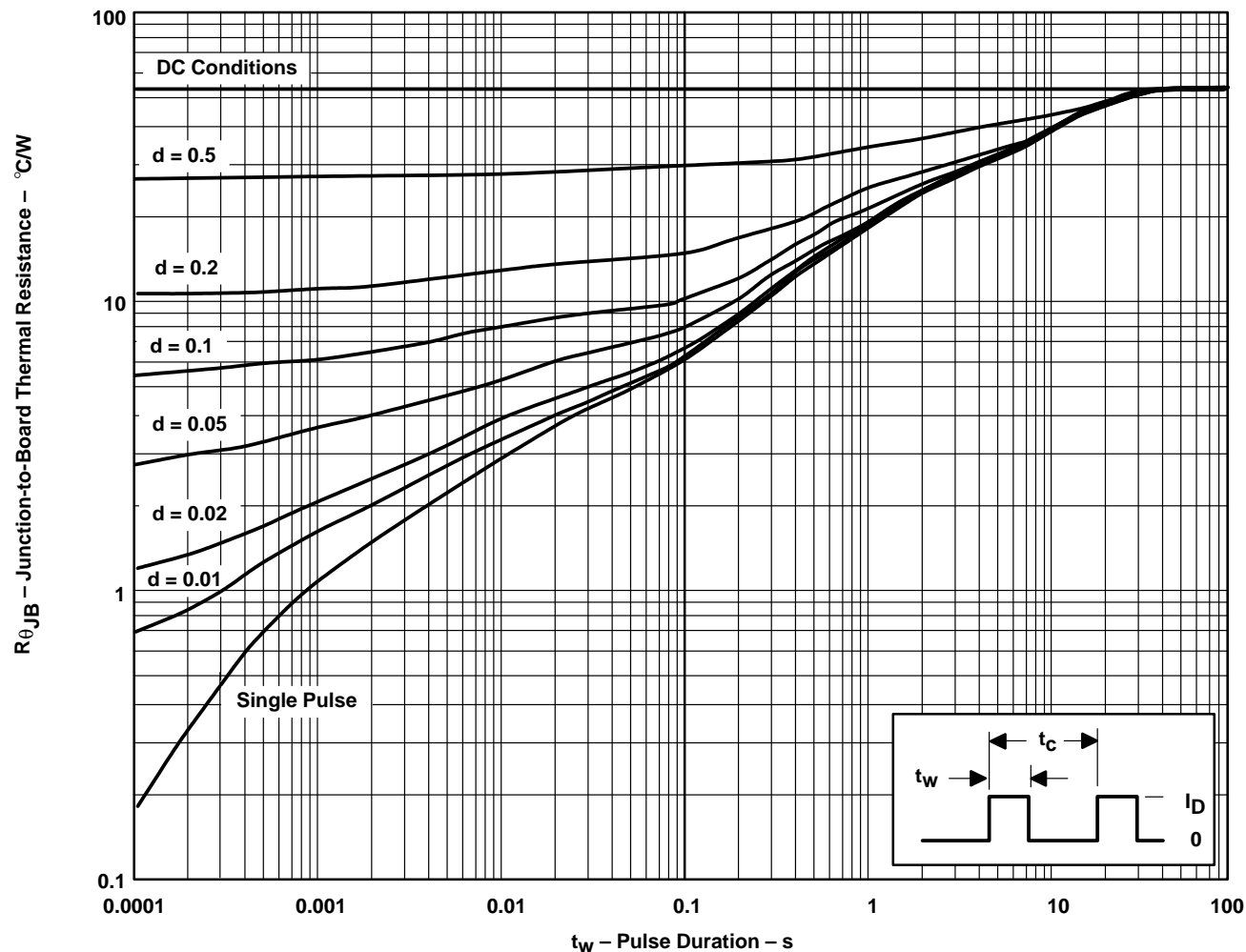
Figure 17

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THERMAL INFORMATION

DW PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
VS
PULSE DURATION



† Device mounted on a 24 in², 4-layer FR4 printed-circuit board with no heatsink.

NOTES A: $Z_{\theta JB}(t) = r(t) R_{\theta JB}$
 t_W = pulse duration
 t_C = cycle time
 d = duty cycle = t_W/t_C

Figure 18

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