

# TPIC5621L SIX-OUTPUT POWER DMOS ARRAY

SLIS033 – JUNE 1994

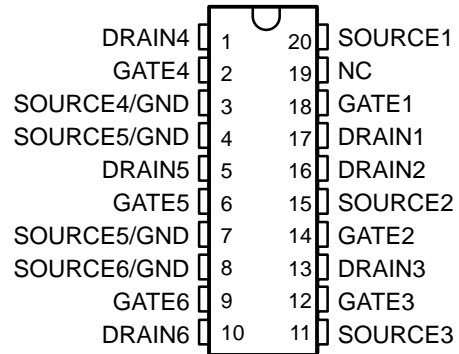
- Low  $r_{DS(on)}$  . . . 0.4  $\Omega$  Typ
- High-Voltage Output . . . 60 V
- Pulsed Current . . . 3 A Per Channel
- Fast Commutation Speed

## description

The TPIC5621L is a monolithic logic-level power DMOS-transistor array that consists of six N-channel enhancement-mode DMOS transistors, three of which are configured with a common source.

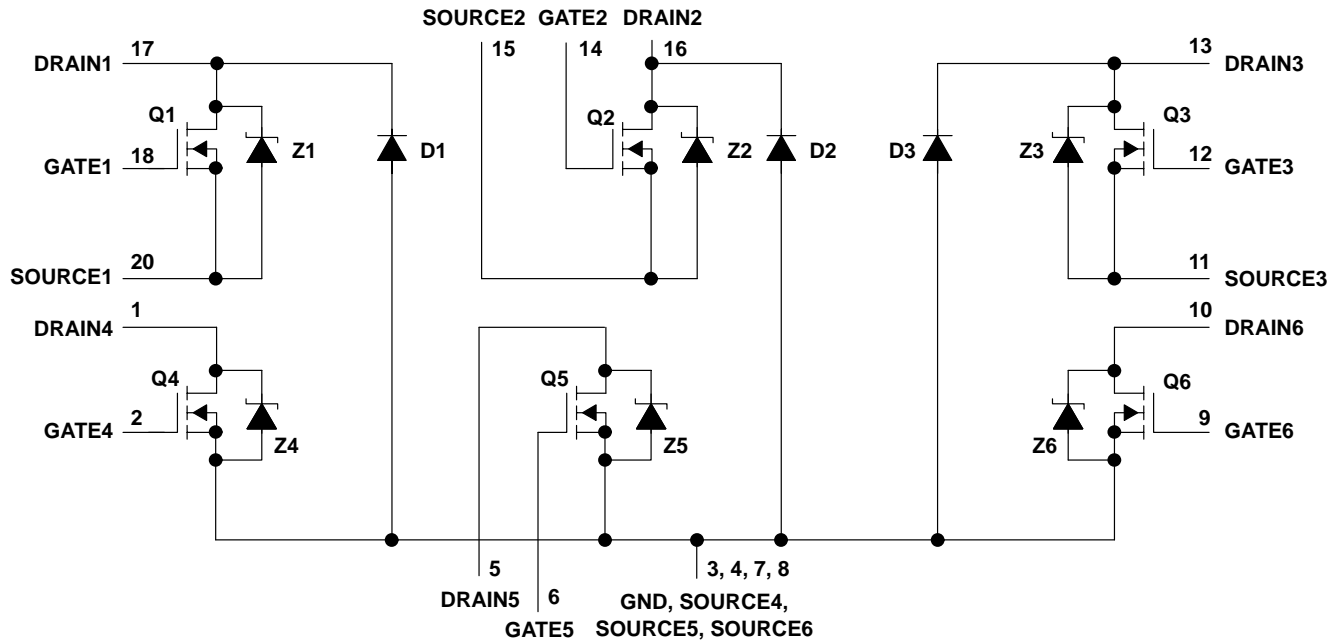
The TPIC5621L is offered in a wide-body surface-mount (DW) package and is characterized for operation over the case temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

DW PACKAGE  
(TOP VIEW)



NC – No internal connection

## schematic



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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# TPIC5621L

## SIX-OUTPUT POWER DMOS ARRAY

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### absolute maximum ratings over operating case temperature range (unless otherwise noted)†

|  |  |
|--|--|
| Drain-to-source voltage, $V_{DS}$ .....  | 60 V                                       |
| Source-to-GND voltage (Q1, Q2, and Q3) .....   | 100 V                                      |
| Drain-to-GND voltage (Q1, Q2, and Q3) .....  | 100 V                                      |
| Drain-to-GND voltage (Q4, Q5, and Q6) .....  | 60 V                                       |
| Gate-to-source voltage range, $V_{GS}$ .....   | $\pm 20$ V                                 |
| Continuous drain current, each output, $T_C = 25^\circ\text{C}$ .....                                    | 1 A  |
| Continuous source-to-drain diode current, $T_C = 25^\circ\text{C}$ .....                                 | 1 A  |
| Pulsed drain current, $I_{max}$ , $T_C = 25^\circ\text{C}$ (each output, see Note 1 and Figure 15) ..... | 3 A  |
| Single-pulse avalanche energy, $E_{AS}$ , $T_C = 25^\circ\text{C}$ (see Figures 4, 15 and 16) .....      | 18 mJ                                      |
| Continuous total dissipation (see Figure 15) .....   | See Dissipation Rating Table               |
| Operating virtual junction temperature range, $T_J$ .....  | $-40^\circ\text{C}$ to $150^\circ\text{C}$ |
| Operating case temperature range, $T_C$ .....  | $-40^\circ\text{C}$ to $125^\circ\text{C}$ |
| Storage temperature range .....  | $-65^\circ\text{C}$ to $150^\circ\text{C}$ |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .....                                       | $260^\circ\text{C}$                        |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%.

DISSIPATION RATING TABLE

| PACKAGE | $T_C \leq 25^\circ\text{C}$<br>POWER RATING | DERATING FACTOR<br>ABOVE $T_C = 25^\circ\text{C}$ | $T_C = 125^\circ\text{C}$<br>POWER RATING |
|---------|---|---|---|
| DW      | 1389 mW                                     | 11.1 mW/ $^\circ\text{C}$                         | 279 mW                                    |

**electrical characteristics,  $T_C = 25^\circ\text{C}$  (unless otherwise noted)**

| PARAMETER     |  | TEST CONDITIONS  |                           | MIN | TYP  | MAX  | UNIT          |
|---------------|--|--|---------------------------|-----|------|------|---------------|
| $V_{(BR)DSX}$ | Drain-to-source breakdown voltage                              | $I_D = 250\ \mu\text{A}$ ,   | $V_{GS} = 0$              | 60  |      |      | V             |
| $V_{GS(th)}$  | Gate-to-source threshold voltage                               | $I_D = 1\ \text{mA}$ ,<br>See Figure 5   | $V_{DS} = V_{GS}$         | 1.5 | 1.85 | 2.2  | V             |
| $V_{(BR)}$    | Reverse drain-to-GND breakdown voltage (across D1, D2, and D3) | Drain-to-GND current = $250\ \mu\text{A}$  |                           | 100 |      |      | V             |
| $V_{DS(on)}$  | Drain-to-source on-state voltage                               | $I_D = 1\ \text{A}$ ,<br>See Notes 2 and 3   | $V_{GS} = 5\ \text{V}$ ,  |     | 0.4  | 0.48 | V             |
| $V_{F(SD)}$   | Forward on-state voltage, source-to-drain                      | $I_S = 1\ \text{A}$ ,<br>$V_{GS} = 0$ (Z1, Z2, Z3, Z4, Z5, Z6),<br>See Notes 2 and 3 and Figure 12 |                           |     | 0.9  | 1.1  | V             |
| $V_F$         | Forward on-state voltage, GND-to-drain                         | $I_D = 1\ \text{A}$ (D1, D2, D3),<br>See Notes 2 and 3   |                           |     | 4.6  |      | V             |
| $I_{DSS}$     | Zero-gate-voltage drain current                                | $V_{DS} = 48\ \text{V}$ ,<br>$V_{GS} = 0$  | $T_C = 25^\circ\text{C}$  |     | 0.05 | 1    | $\mu\text{A}$ |
|               |  |  | $T_C = 125^\circ\text{C}$ |     | 0.5  | 10   |               |
| $I_{GSSF}$    | Forward gate current, drain short circuited to source          | $V_{GS} = 16\ \text{V}$ ,  | $V_{DS} = 0$              |     | 10   | 100  | nA            |
| $I_{GSSR}$    | Reverse gate current, drain short circuited to source          | $V_{SG} = 16\ \text{V}$ ,  | $V_{DS} = 0$              |     | 10   | 100  | nA            |
| $I_{lkg}$     | Leakage current, drain-to-GND                                  | $V_{DGND} = 48\ \text{V}$<br>(D1, D2, D3)  | $T_C = 25^\circ\text{C}$  |     | 0.05 | 1    | $\mu\text{A}$ |
|               |  |  | $T_C = 125^\circ\text{C}$ |     | 0.5  | 10   |               |
| $r_{DS(on)}$  | Static drain-to-source on-state resistance                     | $V_{GS} = 5\ \text{V}$ ,<br>$I_D = 1\ \text{A}$ ,<br>See Notes 2 and 3<br>and Figures 6 and 7      | $T_C = 25^\circ\text{C}$  |     | 0.4  | 0.48 | $\Omega$      |
|               |  |  | $T_C = 125^\circ\text{C}$ |     | 0.65 | 0.68 |               |
| $g_{fs}$      | Forward transconductance                                       | $V_{DS} = 15\ \text{V}$ ,<br>See Notes 2 and 3 and Figure 9  | $I_D = 0.5\ \text{A}$ ,   | 1   | 1.29 | 1.45 | S             |
| $C_{iss}$     | Short-circuit input capacitance, common source                 |  |                           |     | 190  | 240  | pF            |
| $C_{oss}$     | Short-circuit output capacitance, common source                | $V_{DS} = 25\ \text{V}$ ,  | $V_{GS} = 0$ ,            |     | 100  | 125  |               |
| $C_{rss}$     | Short-circuit reverse transfer capacitance, common source      | $f = 1\ \text{MHz}$ ,  | See Figure 11             |     | 40   | 50   |               |

NOTES: 2. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.  
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

**source-to-drain and GND-to-drain diode characteristics,  $T_C = 25^\circ\text{C}$**

| PARAMETER |                       | TEST CONDITIONS   |  | MIN        | TYP  | MAX | UNIT          |
|-----------|-----------------------|---|--|------------|------|-----|---------------|
| $t_{rr}$  | Reverse recovery time | $I_S = 0.5\ \text{A}$ ,<br>$V_{GS} = 0$ ,<br>See Figures 1 and 14 | $V_{DS} = 48\ \text{V}$ ,<br>$di/dt = 100\ \text{A}/\mu\text{s}$ , | Z1, Z2, Z3 | 65   |     | ns            |
|           |                       |   |  | Z4, Z5, Z6 | 150  |     |               |
|           |                       |   |  | D1, D2, D3 | 200  |     |               |
| $Q_{RR}$  | Total diode charge    |   |  | Z1, Z2, Z3 | 0.06 |     | $\mu\text{C}$ |
|           |                       |   |  | Z4, Z5, Z6 | 0.3  |     |               |
|           |                       |   |  | D1, D2, D3 | 0.7  |     |               |

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## resistive-load switching characteristics, $T_C = 25^\circ\text{C}$

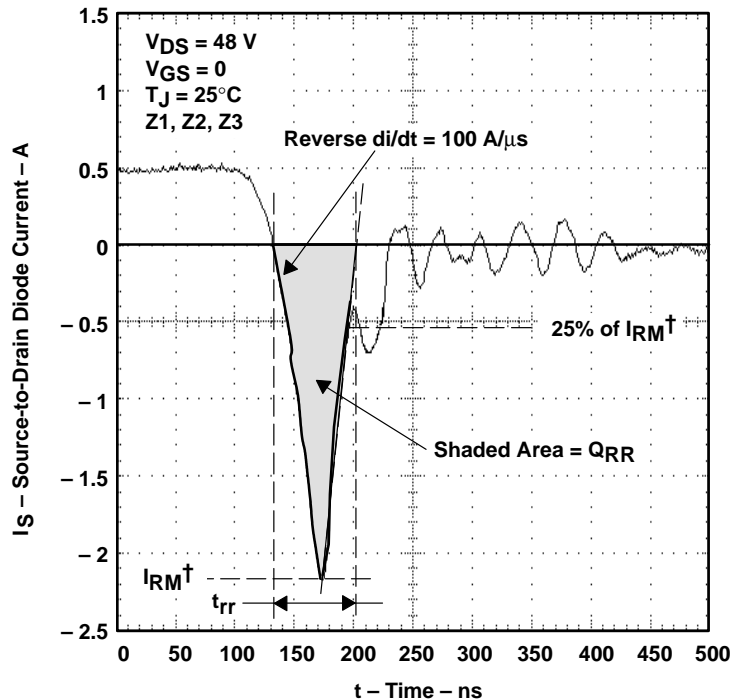
| PARAMETER                                    | TEST CONDITIONS  | MIN | TYP  | MAX | UNIT     |
|--|--|-----|------|-----|----------|
| $t_{d(on)}$ Turn-on delay time               | $V_{DD} = 25\text{ V}$ , $R_L = 50\ \Omega$ , $t_{en} = 10\text{ ns}$ ,<br>$t_{dis} = 10\text{ ns}$ , See Figure 2 |     | 9    | 18  | ns       |
| $t_{d(off)}$ Turn-off delay time             |  |     | 20   | 40  |          |
| $t_r$ Rise time                              |  |     | 21   | 42  |          |
| $t_f$ Fall time                              |  |     | 25   | 50  |          |
| $Q_g$ Total gate charge                      | $V_{DS} = 48\text{ V}$ , $I_D = 0.5\text{ A}$ , $V_{GS} = 5\text{ V}$ ,<br>See Figure 3                            |     | 3.1  | 3.7 | nC       |
| $Q_{gs(th)}$ Threshold gate-to-source charge |  |     | 0.5  | 0.6 |          |
| $Q_{gd}$ Gate-to-drain charge                |  |     | 1.9  | 2.3 |          |
| $L_D$ Internal drain inductance              |  |     | 5    |     | nH       |
| $L_S$ Internal source inductance             |  |     | 5    |     |          |
| $R_g$ Internal gate resistance               |  |     | 0.25 |     | $\Omega$ |

## thermal resistance

| PARAMETER   | TEST CONDITIONS              | MIN | TYP | MAX | UNIT               |
|---|------------------------------|-----|-----|-----|--------------------|
| $R_{\theta JA}$ Junction-to-ambient thermal resistance (see Note 4) | All outputs with equal power |     | 90  |     | $^\circ\text{C/W}$ |
| $R_{\theta JC}$ Junction-to-case thermal resistance                 |                              |     | 27  |     |                    |

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

## PARAMETER MEASUREMENT INFORMATION



$^\dagger I_{RM}$  = maximum recovery current

NOTE A: The above waveform is representative of Z4, Z5, Z6, D1, D2, and D3 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION

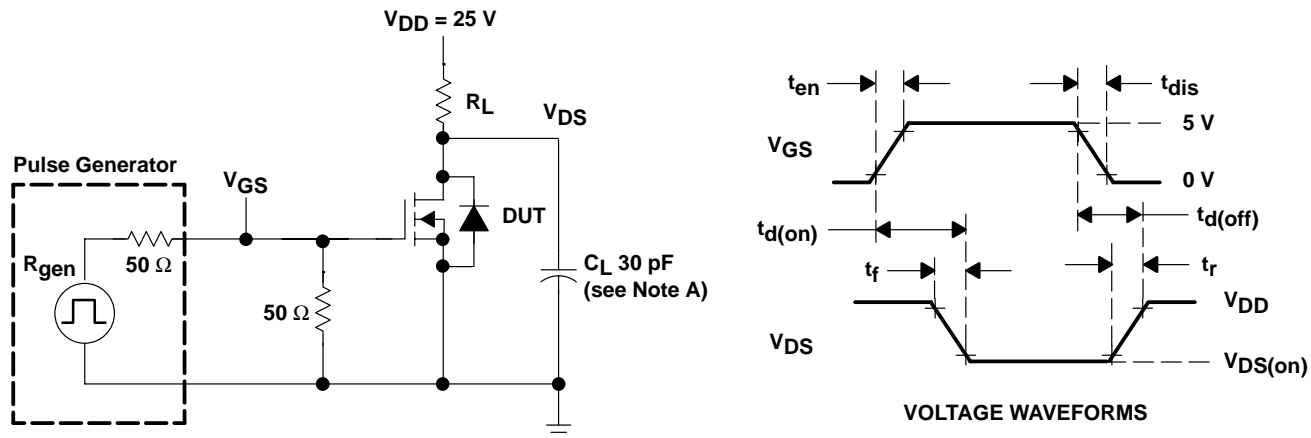


Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

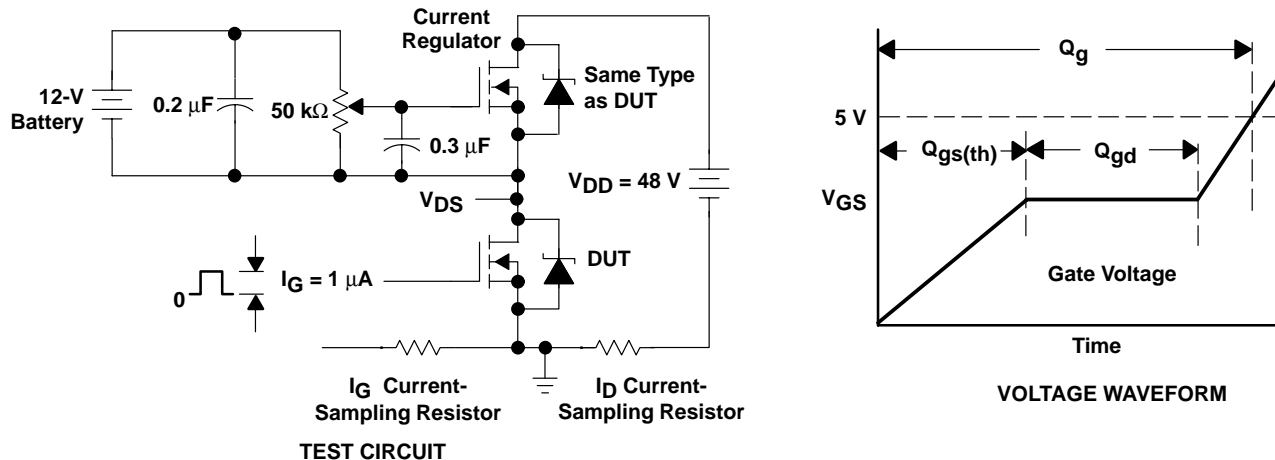
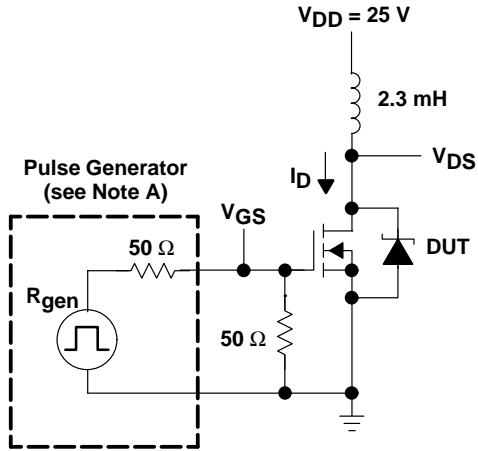


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

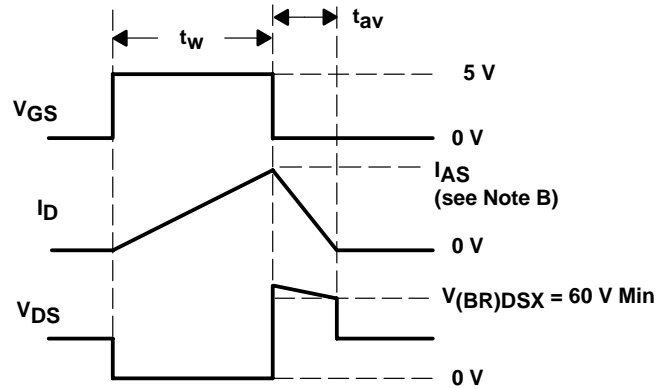
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## PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics:  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_O = 50 \Omega$ .  
B. Input pulse duration ( $t_w$ ) is increased until peak current  $I_{AS} = 3$  A.

$$\text{Energy test level is defined as } E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 18 \text{ mJ.}$$

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

## TYPICAL CHARACTERISTICS

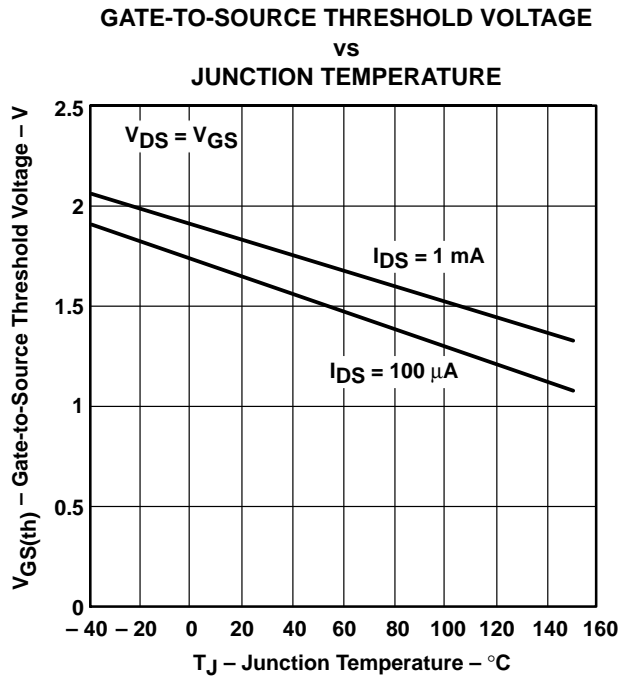


Figure 5

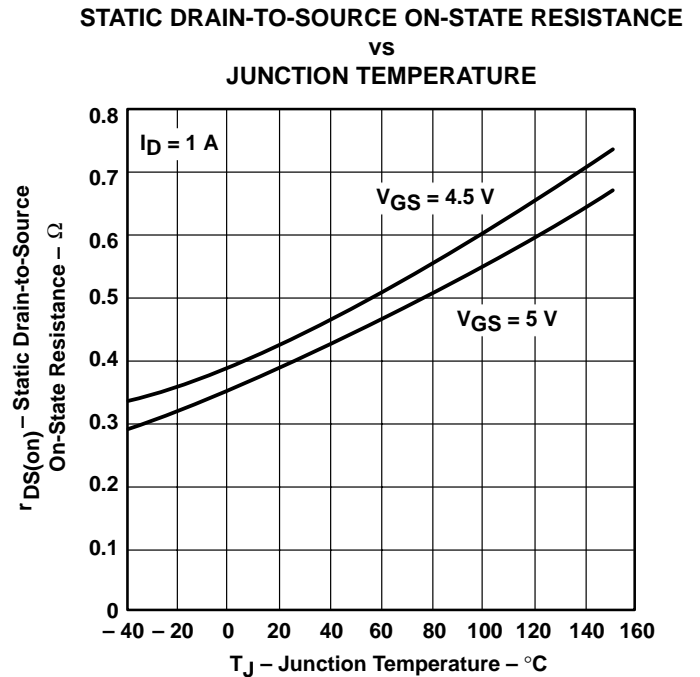


Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE  
vs  
DRAIN CURRENT

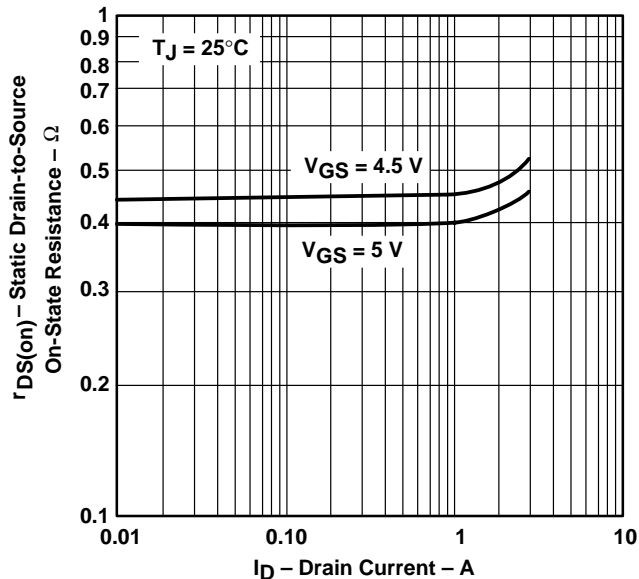


Figure 7

DRAIN-TO-SOURCE CURRENT  
vs  
DRAIN-TO-SOURCE VOLTAGE

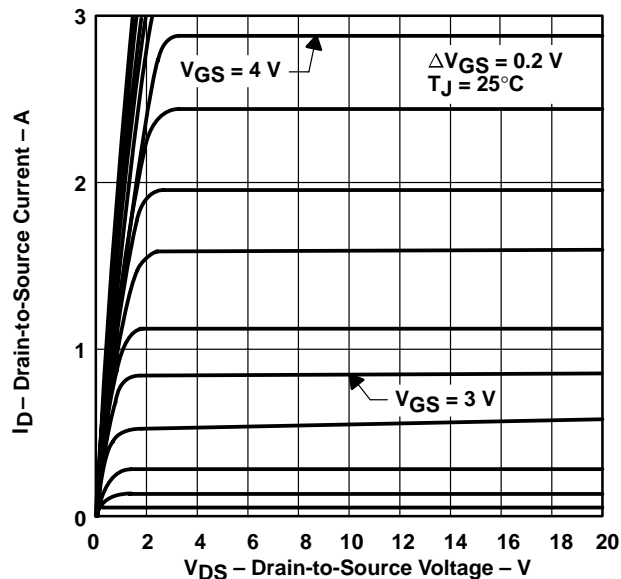


Figure 8

DISTRIBUTION OF  
FORWARD TRANSCONDUCTANCE

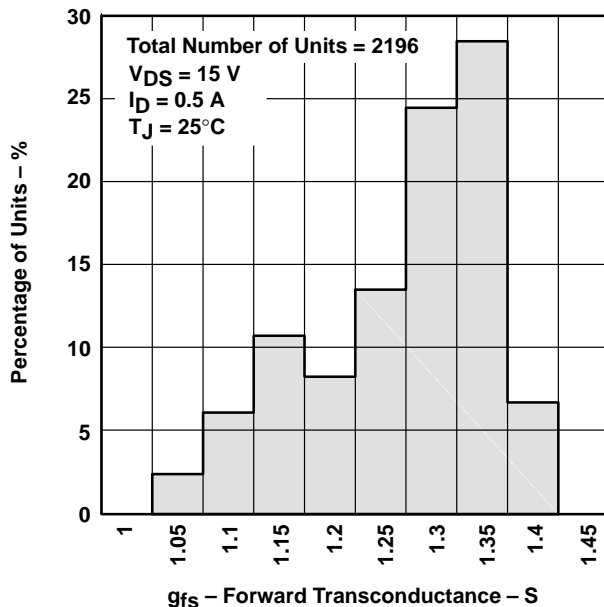


Figure 9

DRAIN-TO-SOURCE CURRENT  
vs  
GATE-TO-SOURCE VOLTAGE

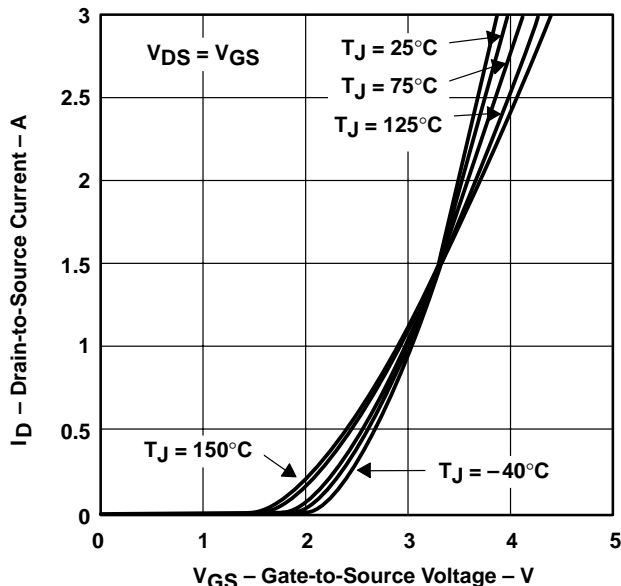


Figure 10

# TPIC5621L SIX-OUTPUT POWER DMOS ARRAY

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## TYPICAL CHARACTERISTICS

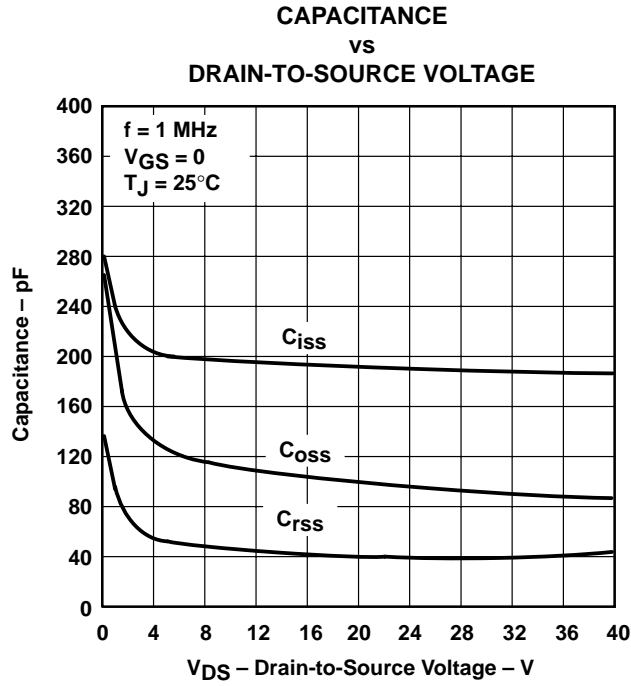


Figure 11

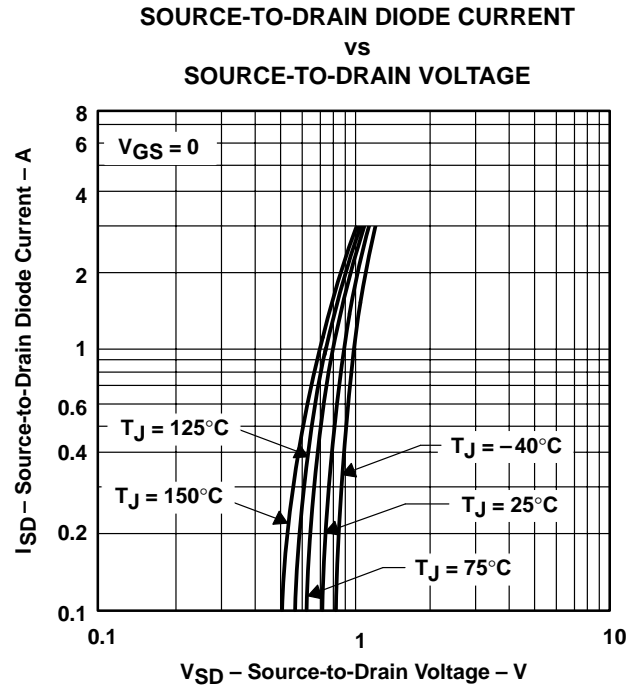


Figure 12

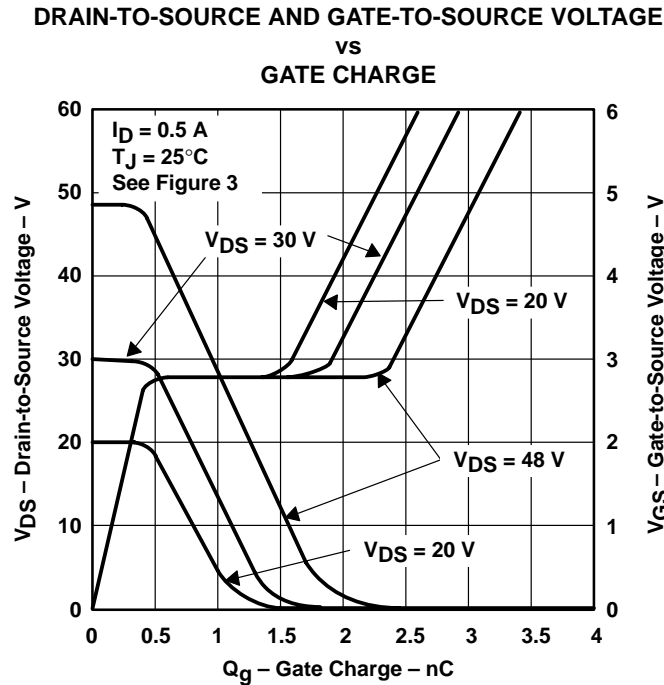


Figure 13

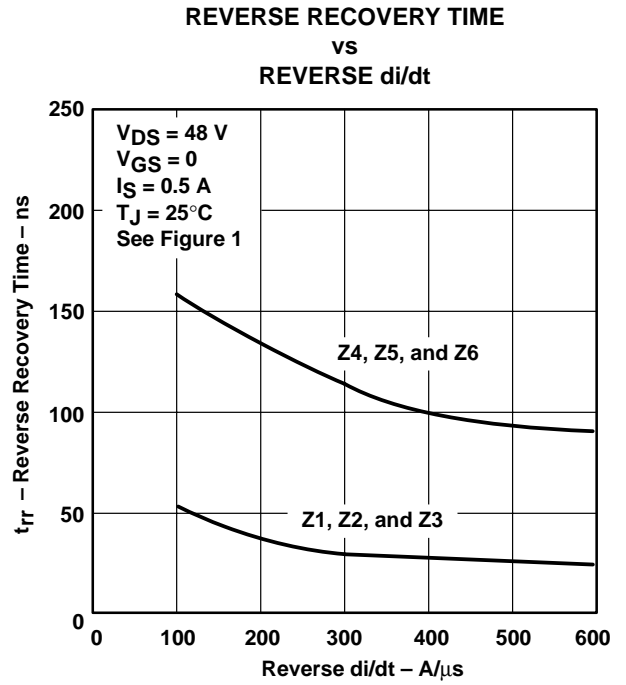
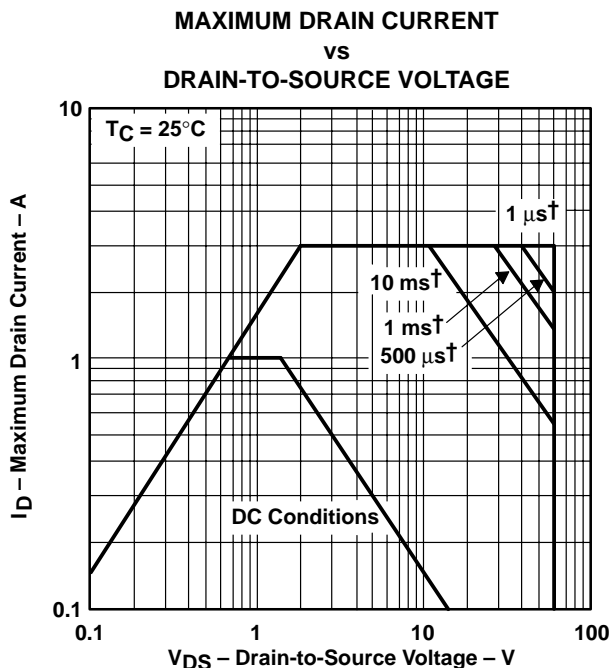


Figure 14



THERMAL INFORMATION



† Less than 2% duty cycle

Figure 15

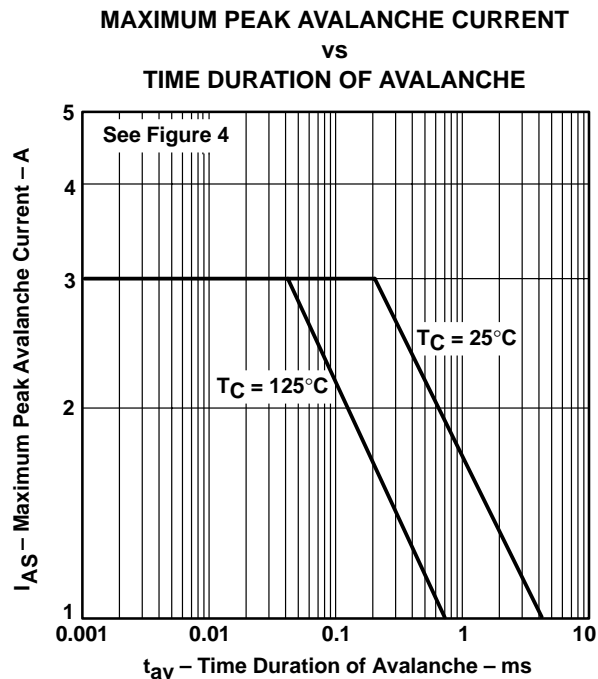
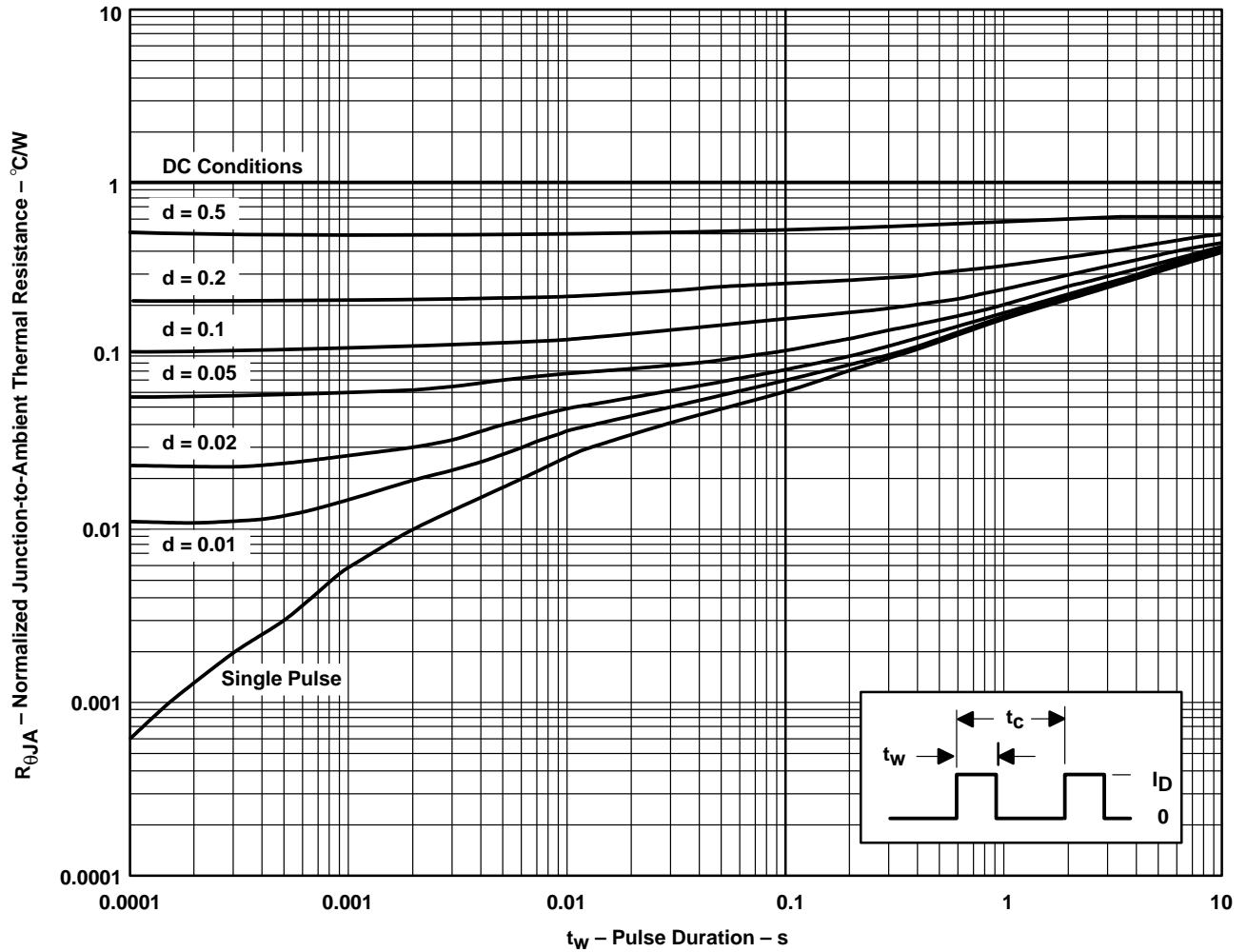


Figure 16

**TPIC5621L**  
**SIX-OUTPUT POWER DMOS ARRAY**

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**THERMAL INFORMATION**  
**NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE†**  
**VS**  
**PULSE DURATION**



† Device mounted on FR4 printed-circuit board with no heat sink

- NOTES:  $Z_{\theta A}(t) = r(t) R_{\theta JA}$   
 $t_w$  = pulse duration  
 $t_c$  = cycle time  
 $d$  = duty cycle =  $t_w/t_c$

**Figure 17**

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