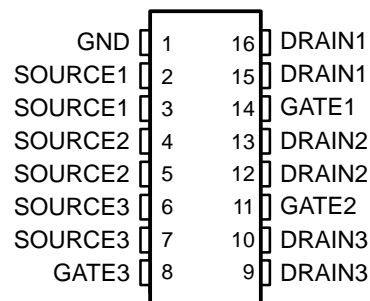


3-CHANNEL INDEPENDENT LOGIC-LEVEL POWER DMOS ARRAY

SLIS034A – JUNE 1994 – REVISED NOVEMBER 1994

- Low $r_{DS(on)}$. . . 0.45 Ω Typ
- High-Voltage Outputs . . . 60 V
- Pulsed Current . . . 3 A Per Channel
- Fast Commutation Speed
- Direct Logic-Level Interface

D PACKAGE
(TOP VIEW)

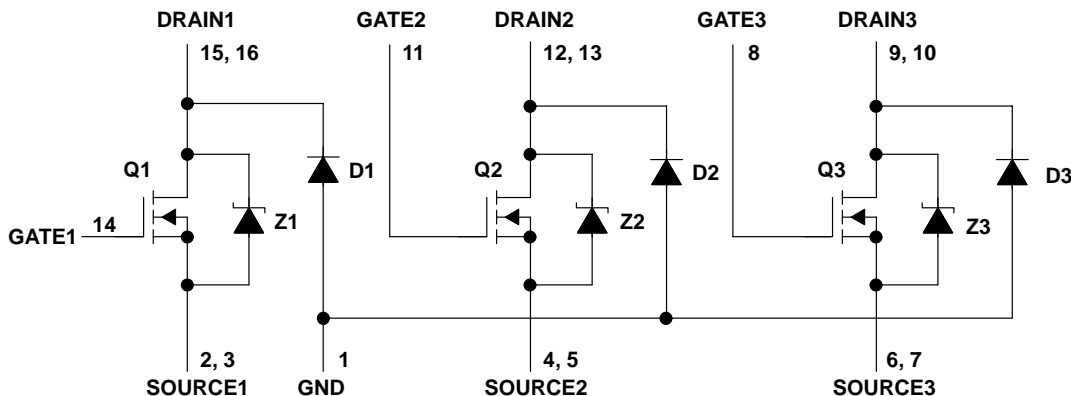


description

The TPIC5322L is a monolithic logic-level power DMOS array that consists of three electrically isolated independent N-channel enhancement-mode DMOS transistors.

The TPIC5322L is offered in a standard 16-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature range of -40°C to 125°C .

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage, V_{GS}	± 20 V
Continuous drain current, each output, all outputs on, $T_C = 25^{\circ}\text{C}$	1 A
Continuous source-to-drain diode current, $T_C = 25^{\circ}\text{C}$	1 A
Pulsed drain current, each output, I_{max} , $T_C = 25^{\circ}\text{C}$ (see Note 1 and Figure 15)	3 A
Single-pulse avalanche energy, E_{AS} , $T_C = 25^{\circ}\text{C}$ (see Figure 4)	40.5 mJ
Continuous total power dissipation at (or below) $T_C = 25^{\circ}\text{C}$	1.09 W
Operating virtual junction temperature range, T_J	-40°C to 150°C
Operating case temperature range, T_C	-40°C to 125°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%.

TPIC5322L

3-CHANNEL INDEPENDENT LOGIC-LEVEL POWER DMOS ARRAY

SLIS034A – JUNE 1994 – REVISED NOVEMBER 1994

electrical characteristics, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	$I_D = 250 \mu\text{A}$,	$V_{GS} = 0$	60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	$I_D = 1 \text{ mA}$, See Figure 5	$V_{DS} = V_{GS}$,	1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2, and D3)	Drain-to-GND current = $250 \mu\text{A}$		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	$I_D = 1 \text{ A}$, See Notes 2 and 3	$V_{GS} = 5 \text{ V}$,		0.45	0.525	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	$I_S = 1 \text{ A}$, See Notes 2 and 3 and Figure 12	$V_{GS} = 0$,		0.85	1	V
V_F	Forward on-state voltage, GND-to-drain	$I_D = 1 \text{ A}$			3.7		V
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = 48 \text{ V}$, $V_{GS} = 0$	$T_C = 25^\circ\text{C}$		0.05	1	μA
			$T_C = 125^\circ\text{C}$			0.5	
I_{GSSF}	Forward gate current, drain short circuited to source	$V_{GS} = 16 \text{ V}$, $V_{DS} = 0$			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	$V_{SG} = 16 \text{ V}$, $V_{DS} = 0$			10	100	nA
I_{lkg}	Leakage current, drain-to-GND	$V_{DGND} = 48 \text{ V}$	$T_C = 25^\circ\text{C}$		0.05	1	μA
			$T_C = 125^\circ\text{C}$			0.5	
$r_{DS(on)}$	Static drain-to-source on-state resistance	$V_{GS} = 5 \text{ V}$, $I_D = 1 \text{ A}$, See Notes 2 and 3 and Figures 6 and 7	$T_C = 25^\circ\text{C}$		0.45	0.525	Ω
			$T_C = 125^\circ\text{C}$			0.7	
g_{fs}	Forward transconductance	$V_{DS} = 10 \text{ V}$, See Notes 2 and 3 and Figure 9	$I_D = 0.5 \text{ A}$,	1	1.24		S
C_{iss}	Short-circuit input capacitance, common source	$V_{DS} = 25 \text{ V}$, $f = 1 \text{ MHz}$, $V_{GS} = 0$, See Figure 11			135	170	pF
C_{oss}	Short-circuit output capacitance, common source				80	100	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				30	40	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	$I_S = 0.5 \text{ A}$, $V_{GS} = 0$, See Figures 1 and 14	$V_{DS} = 48 \text{ V}$, $di/dt = 100 \text{ A}/\mu\text{s}$,	Z1, Z2, Z3		35	ns
				D1, D2, D3		110	
Q_{RR}	Total diode charge			Z1, Z2, Z3		0.035	μC
				D1, D2, D2		0.35	



TPIC5322L

3-CHANNEL INDEPENDENT LOGIC-LEVEL POWER DMOS ARRAY

SLIS034A – JUNE 1994 – REVISED NOVEMBER 1994

resistive-load switching characteristics, $T_C = 25^\circ\text{C}$

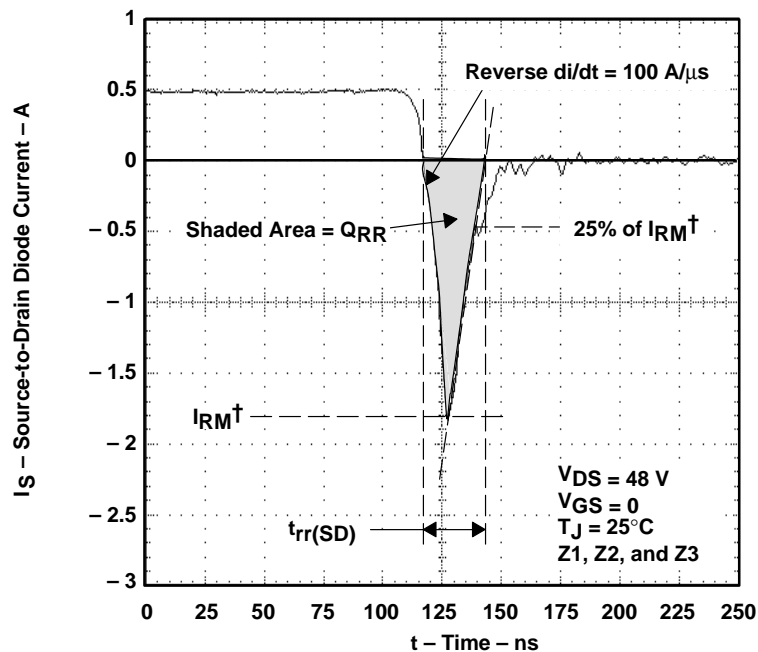
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$ Turn-on delay time	$V_{DD} = 25\text{ V}$, $R_L = 50\ \Omega$, $t_{en} = 10\text{ ns}$, $t_{dis} = 10\text{ ns}$, See Figure 2		21	42	ns
$t_{d(off)}$ Turn-off delay time			20	40	
t_r Rise time			5	10	
t_f Fall time			13	26	
Q_g Total gate charge	$V_{DS} = 48\text{ V}$, $I_D = 0.5\text{ A}$, $V_{GS} = 5\text{ V}$, See Figure 3		3.1	3.8	nC
$Q_{gs(th)}$ Threshold gate-to-source charge			0.4	0.5	
Q_{gd} Gate-to-drain charge			1.3	1.6	
L_D Internal drain inductance			5		nH
L_S Internal source inductance			5		
R_g Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance (see Note 4)	All outputs with equal power		115		$^\circ\text{C/W}$
$R_{\theta JP}$ Junction-to-pin thermal resistance			32		$^\circ\text{C/W}$

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

PARAMETER MEASUREMENT INFORMATION



$\dagger I_{RM}$ = maximum recovery current

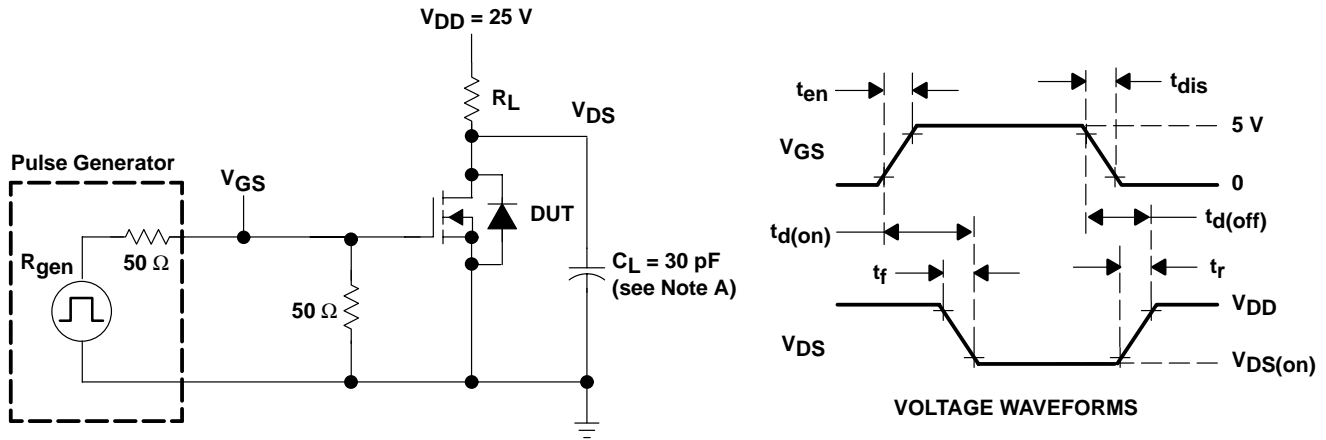
NOTE A: The above waveform is representative of D1, D2, and D3 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

TPIC5322L 3-CHANNEL INDEPENDENT LOGIC-LEVEL POWER DMOS ARRAY

SLIS034A – JUNE 1994 – REVISED NOVEMBER 1994

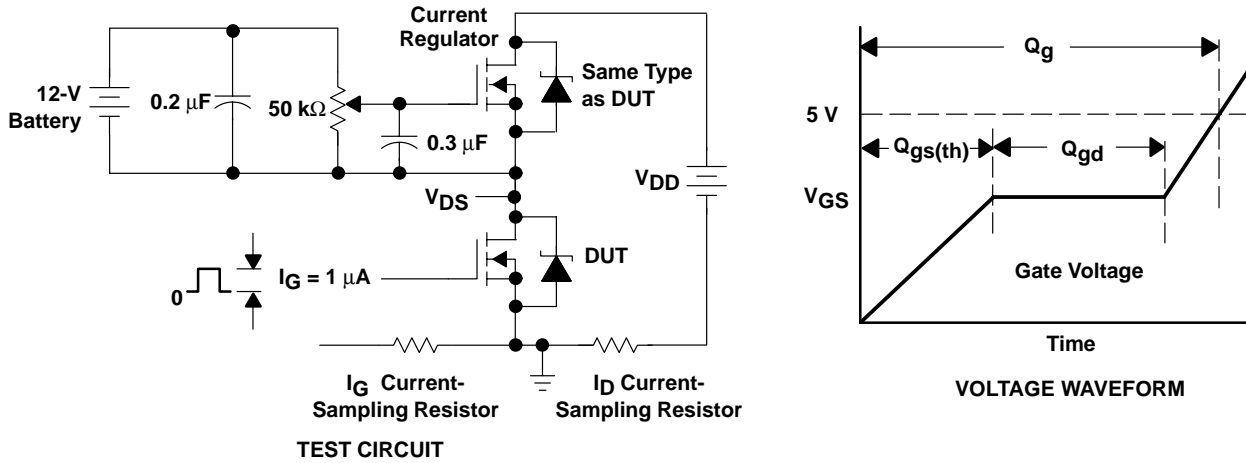
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

NOTE A: C_L includes probe and jig capacitance.

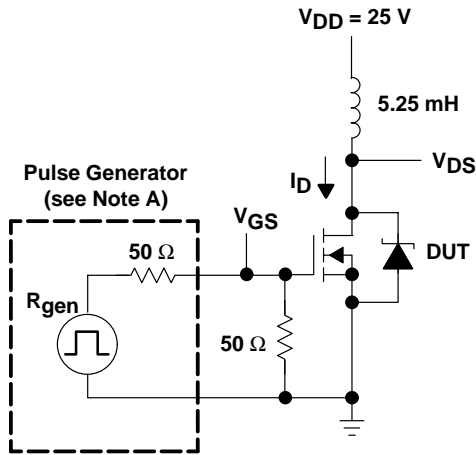
Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms



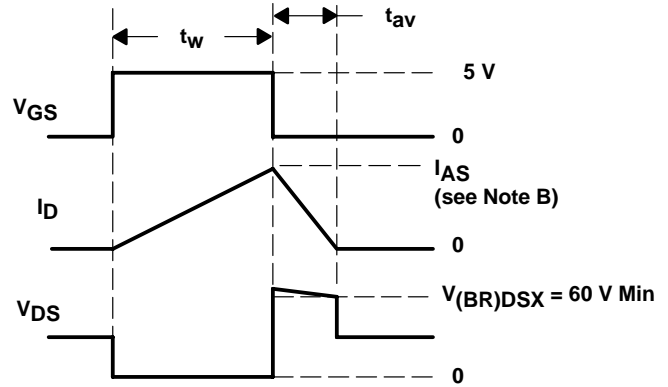
TEST CIRCUIT

Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$, $Z_O = 50 \Omega$.
 B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 3 \text{ A}$.

$$\text{Energy test level is defined as } E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 40.5 \text{ mJ.}$$

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

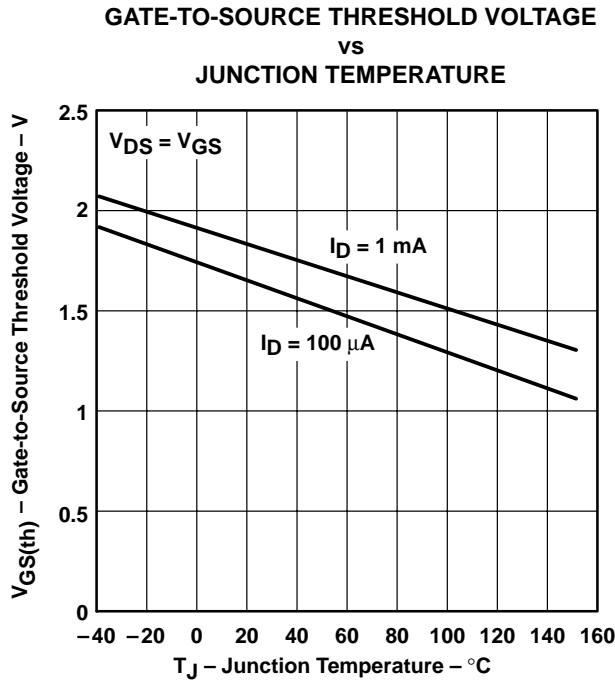


Figure 5

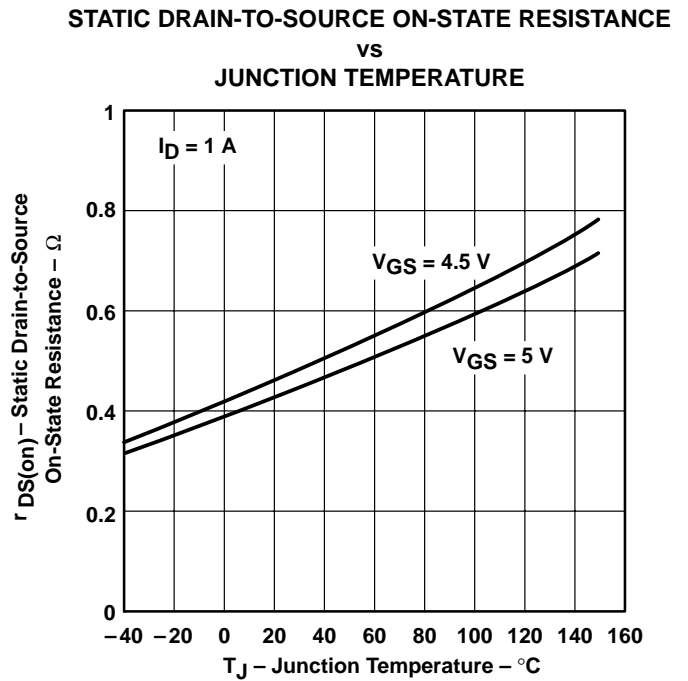


Figure 6

TPIC5322L 3-CHANNEL INDEPENDENT LOGIC-LEVEL POWER DMOS ARRAY

SLIS034A – JUNE 1994 – REVISED NOVEMBER 1994

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
VS
DRAIN CURRENT

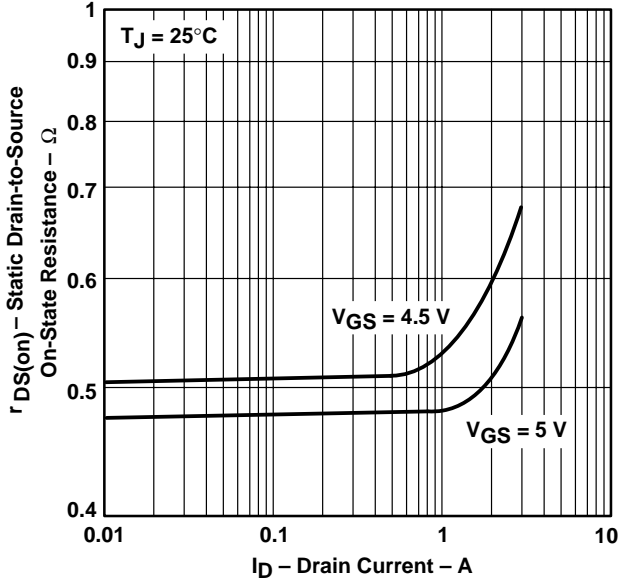


Figure 7

DRAIN CURRENT
VS
DRAIN-TO-SOURCE VOLTAGE

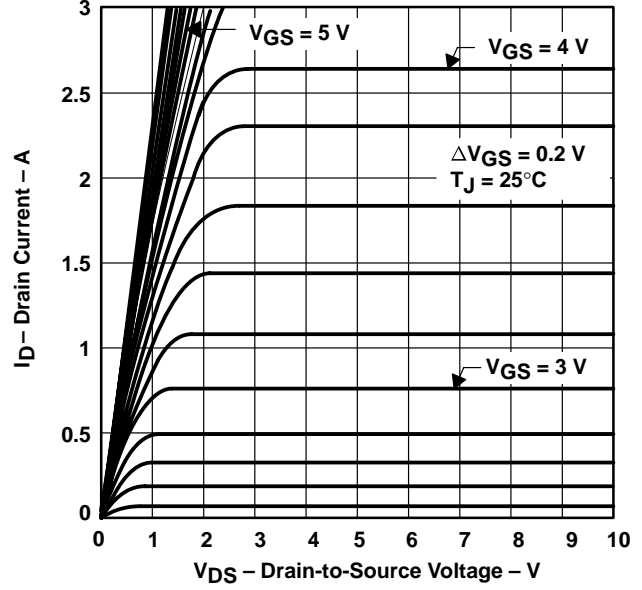


Figure 8

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

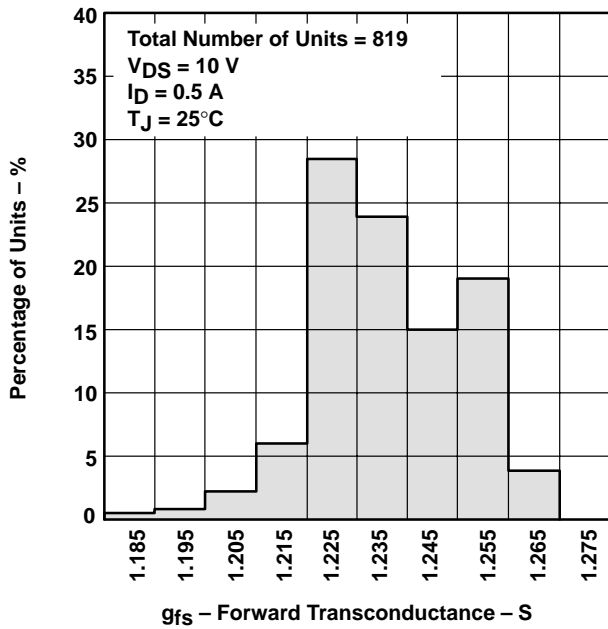


Figure 9

DRAIN CURRENT
VS
GATE-TO-SOURCE VOLTAGE

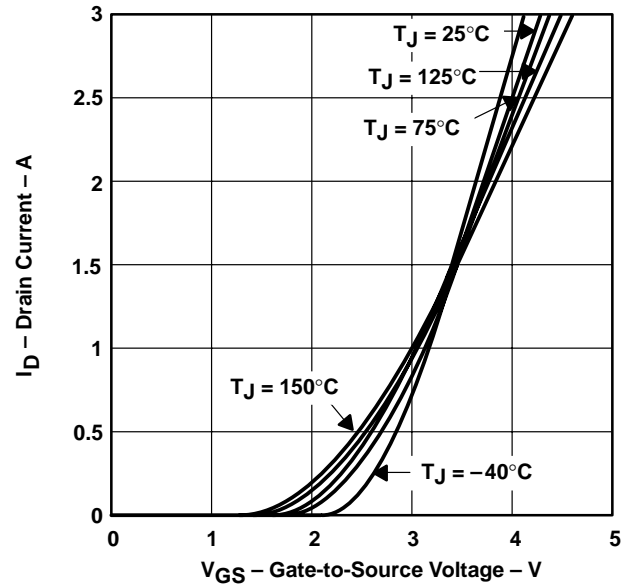


Figure 10



TYPICAL CHARACTERISTICS

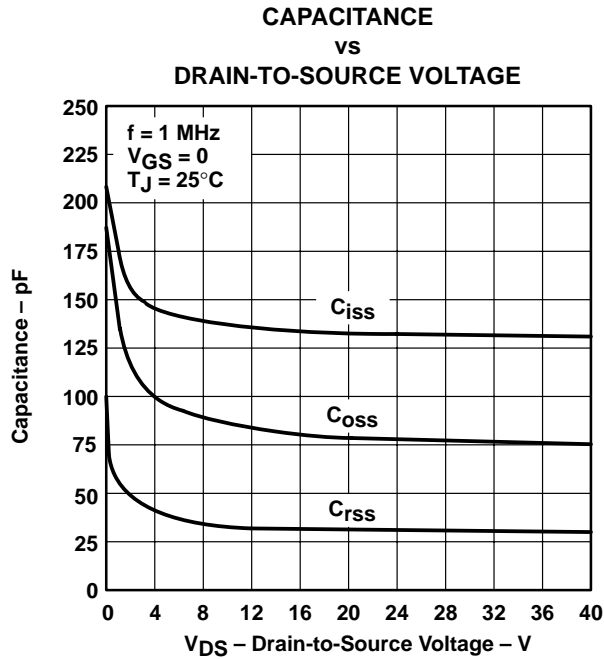


Figure 11

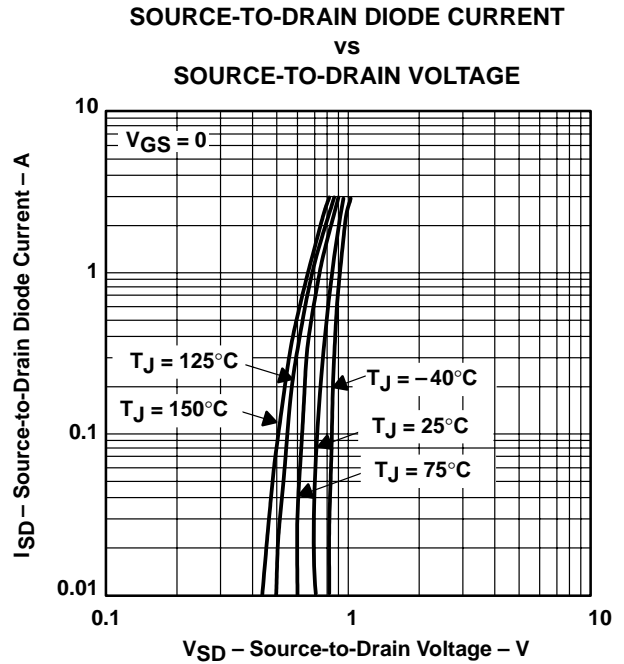


Figure 12

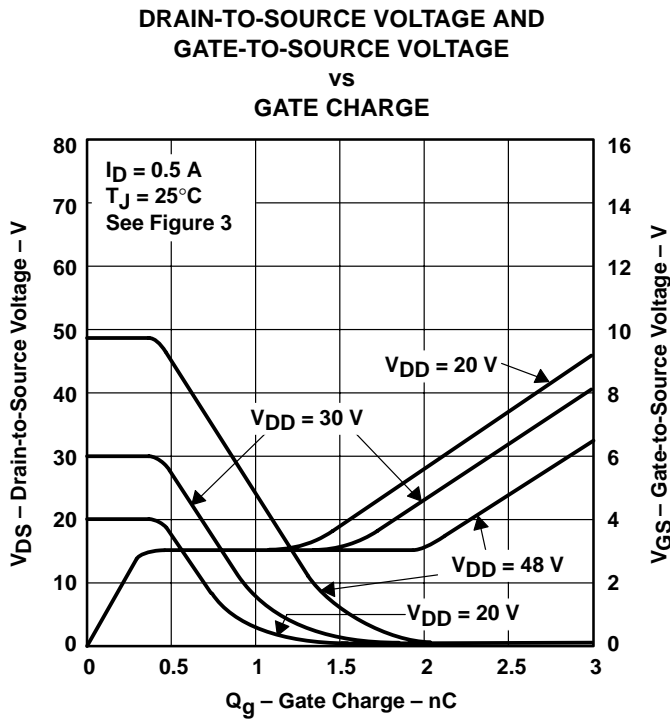


Figure 13

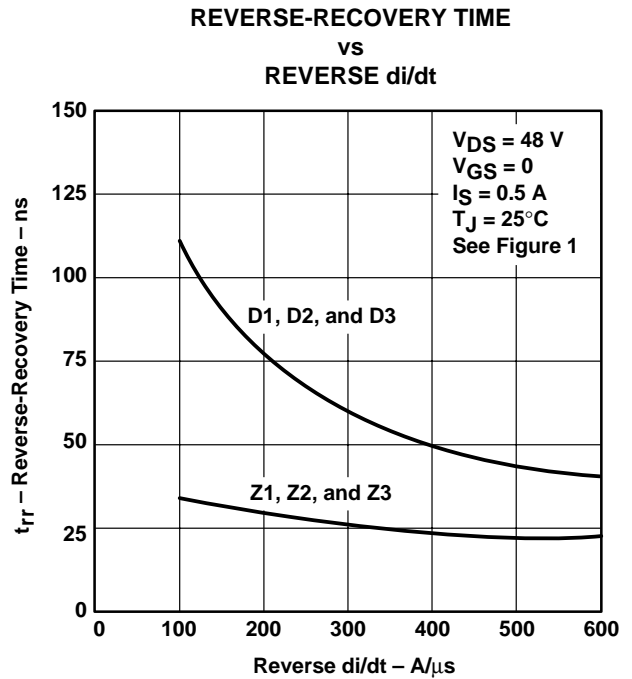


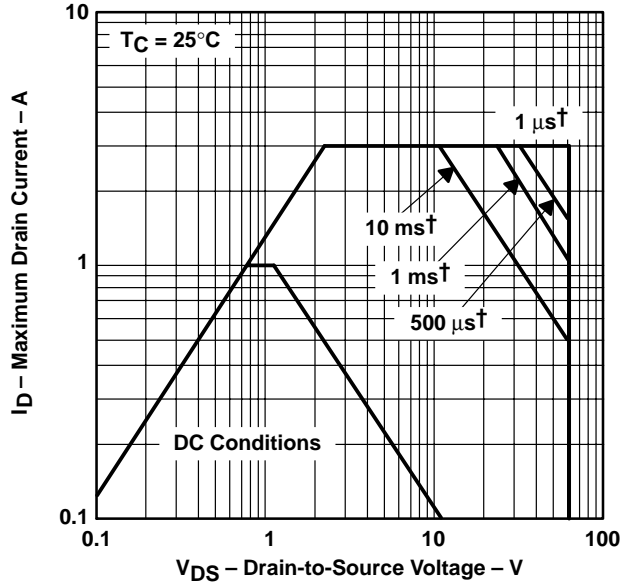
Figure 14

TPIC5322L 3-CHANNEL INDEPENDENT LOGIC-LEVEL POWER DMOS ARRAY

SLIS034A – JUNE 1994 – REVISED NOVEMBER 1994

THERMAL INFORMATION

**MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE**



† Less than 2% duty cycle

Figure 15

**MAXIMUM PEAK-AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE**

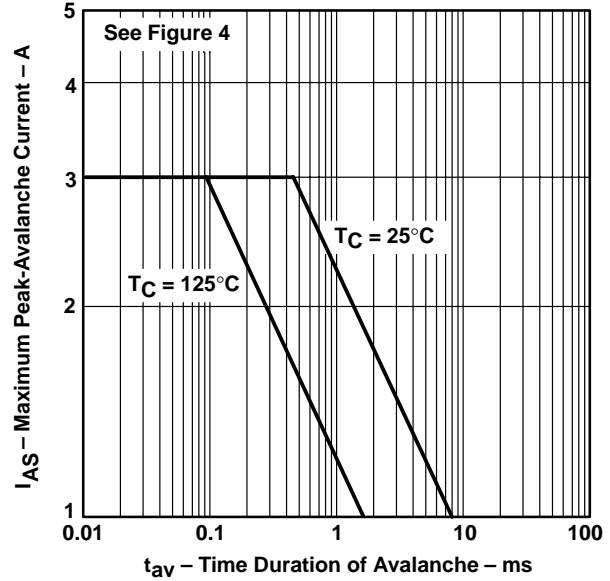
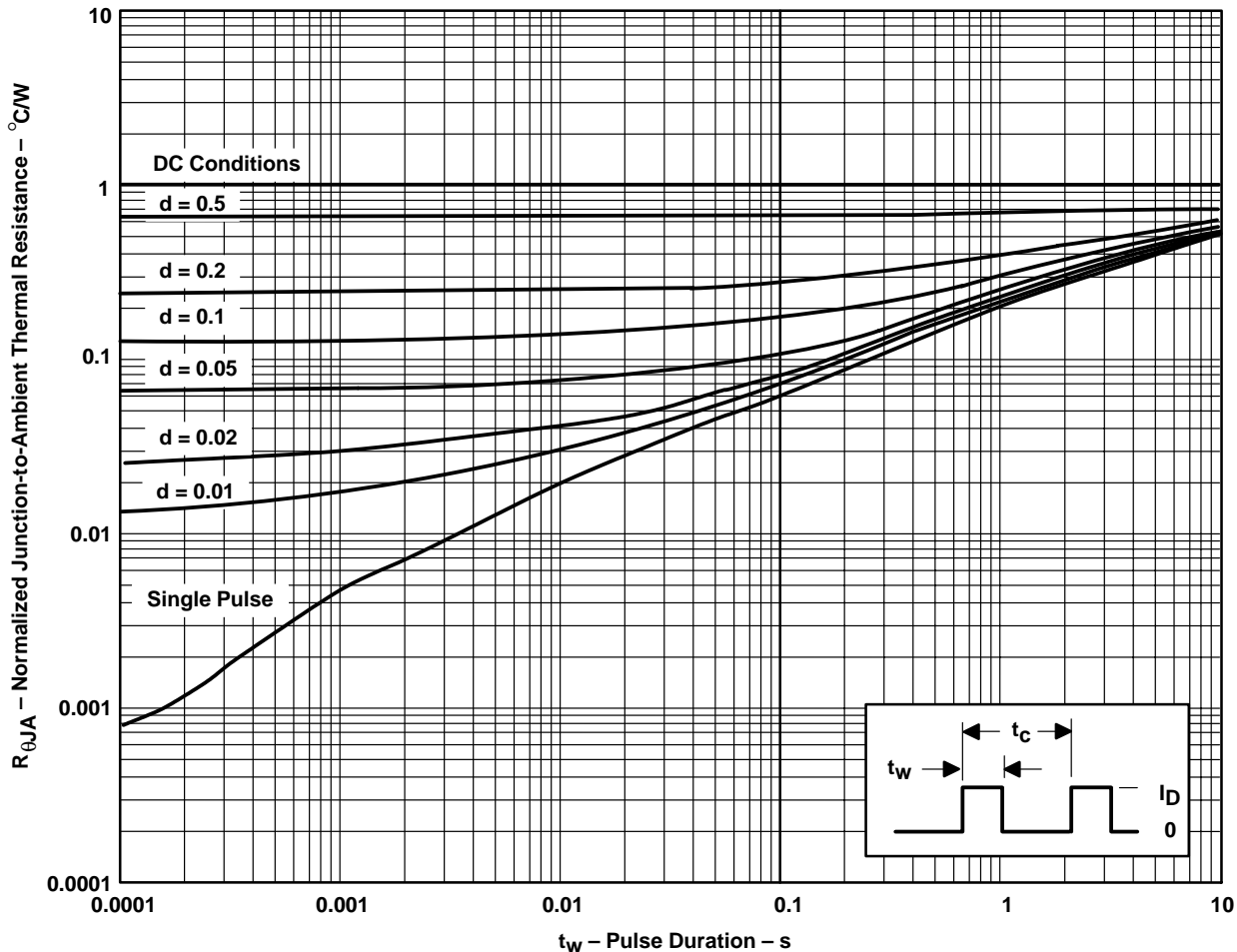


Figure 16

THERMAL INFORMATION

D PACKAGE†
 NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
 VS
 PULSE DURATION



† Device mounted on FR4 printed-circuit board with no heat sink

- NOTES: $Z_{\theta A}(t) = r(t) R_{\theta JA}$
 t_w = pulse duration
 t_c = cycle time
 d = duty cycle = t_w/t_c

Figure 17

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