

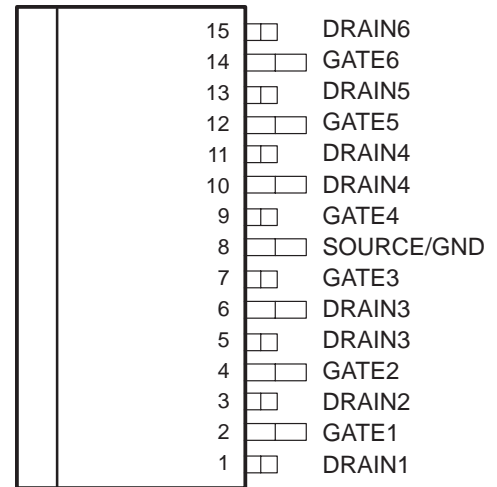
# TPIC2601

## 6-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

SLIS048A – NOVEMBER 1996 – REVISED JANUARY 1998

- Low  $r_{DS(on)}$  . . . 0.25  $\Omega$  Typ
- High Output Voltage . . . 60 V
- Pulsed Current . . . 10 A Per Channel
- Avalanche Energy Capability . . . 105 mJ
- Input Transient Protection . . . 2000 V

KTC or KTD† PACKAGE  
(TOP VIEW)



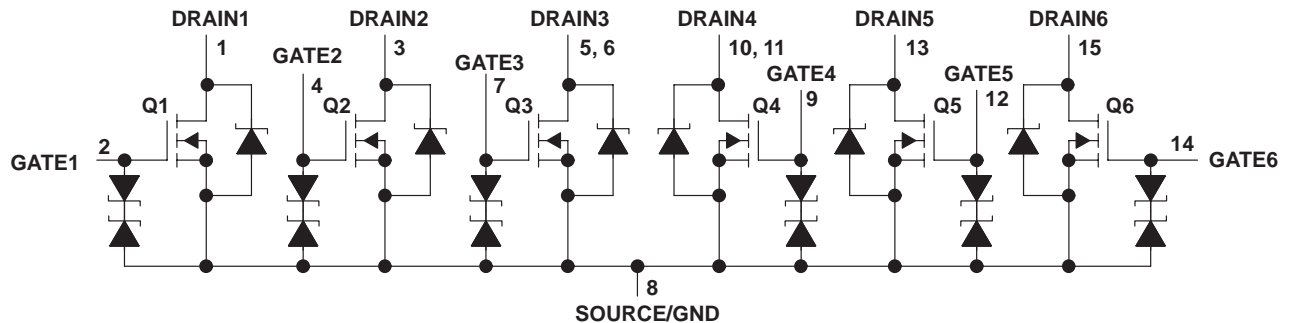
† TI Japan only

### description

The TPIC2601 is a monolithic power DMOS array that consists of six electrically isolated N-channel enhancement-mode DMOS transistors configured with a common source and open drains. Each transistor features integrated high-current zener diodes to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 2000 V of ESD protection when tested using the human-body model.

The TPIC2601 is offered in a 15-pin PowerFLEX™ (KTC) package and is characterized for operation over the case temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . A 15-pin PowerFLEX™ (KTD) package is also available for TI Japan only.

### schematic



NOTE A: For correct operation, no drain terminal may be taken below GND.



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### absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, $V_{DS}$	60 V
Gate-to-source voltage, $V_{GS}$	-9 V to 18 V
Continuous drain current, each output, all outputs on, $T_C = 25^\circ\text{C}$	2 A
Pulsed drain current, each output, $I_{Dmax}$ , $T_C = 25^\circ\text{C}$ (see Note 1 and Figure 7)	10 A
Continuous gate-to-source zener diode current, $T_C = 25^\circ\text{C}$	$\pm 25$ mA
Pulsed gate-to-source zener diode current, $T_C = 25^\circ\text{C}$	$\pm 250$ mA
Single-pulse avalanche energy, $E_{AS}$ , $T_C = 25^\circ\text{C}$ (see Figures 4 and 16)	105 mJ
Continuous total power dissipation at (or below) $T_A = 25^\circ\text{C}$	1.7 W
Power dissipation at (or below) $T_C = 75^\circ\text{C}$ , all outputs on	18.75 W
Operating virtual junction temperature range, $T_J$	-40°C to 150°C
Operating case temperature range, $T_C$	-40°C to 125°C
Storage temperature range, $T_{stg}$	-40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

### electrical characteristics, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	$I_D = 250 \mu\text{A}$ ,	$V_{GS} = 0$	60			V	
$V_{GS(th)}$	Gate-to-source threshold voltage	$I_D = 1 \text{ mA}$ ,	$V_{DS} = V_{GS}$ ,	1.5	2.05	2.2	V	
$V_{GS(th)match}$	Gate-to-source threshold voltage matching	See Figure 5			5	40	mV	
$V_{(BR)GS}$	Gate-to-source breakdown voltage	$I_{GS} = 250 \mu\text{A}$		18			V	
$V_{(BR)SG}$	Source-to-gate breakdown voltage	$I_{SG} = 250 \mu\text{A}$		9			V	
$V_{DS(on)}$	Drain-to-source on-state voltage	$I_D = 2 \text{ A}$ ,	$V_{GS} = 10 \text{ V}$ ,		0.5	0.6	V	
		See Notes 2 and 3						
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	$I_S = 2 \text{ A}$ ,	$V_{GS} = 0$ ,		0.85	1	V	
		See Notes 2 and 3 and Figure 12						
$I_{DSS}$	Zero-gate-voltage drain current	$V_{DS} = 48 \text{ V}$ ,	$V_{GS} = 0$	$T_C = 25^\circ\text{C}$	0.05	1	$\mu\text{A}$	
				$T_C = 125^\circ\text{C}$	0.5	10		
$I_{GSSF}$	Forward gate current, drain short circuited to source	$V_{GS} = 10 \text{ V}$ ,	$V_{DS} = 0$		20	200	nA	
$I_{GSSR}$	Reverse gate current, drain short circuited to source	$V_{SG} = 5 \text{ V}$ ,	$V_{DS} = 0$		10	100	nA	
$r_{DS(on)}$	Static drain-to-source on-state resistance	$V_{GS} = 10 \text{ V}$ ,	$I_D = 2 \text{ A}$ ,	$T_C = 25^\circ\text{C}$	0.25	0.3	$\Omega$	
				$T_C = 125^\circ\text{C}$	0.4	0.5		
		See Notes 2 and 3 and Figures 6 and 7						
$g_{fs}$	Forward transconductance	$V_{DS} = 15 \text{ V}$ ,	$I_D = 1 \text{ A}$	1.3	1.95		S	
		See Notes 2 and 3 and Figure 9						
$C_{iss}$	Short-circuit input capacitance, common source	$V_{DS} = 25 \text{ V}$ ,			180	225	pF	
$C_{oss}$	Short-circuit output capacitance, common source			$f = 1 \text{ MHz}$ ,	$V_{GS} = 0$ ,	110		138
$C_{rss}$	Short-circuit reverse transfer capacitance, common source			See Figure 11		80		100

NOTES: 2. Technique should limit  $T_J - T_C$  to 10°C maximum.

3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.



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### source-to-drain diode characteristics, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{rr}(\text{SD})$	Reverse-recovery time	$I_S = 1\text{ A}$ , $V_{DS} = 48\text{ V}$ , $V_{GS} = 0$ , $di/dt = 100\text{ A}/\mu\text{s}$ , See Figures 1 and 14		72		ns
$Q_{RR}$	Total diode charge			180		nC

### resistive-load switching characteristics, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(\text{on})}$	Delay time, $V_{GS}\uparrow$ to $V_{DS}\downarrow$ turn on	$V_{DD} = 25\text{ V}$ , $R_L = 25\ \Omega$ , $t_{\text{en}} = 10\text{ ns}$ , $t_{\text{dis}} = 10\text{ ns}$ , See Figure 2		194		ns
$t_{d(\text{off})}$	Delay time, $V_{GS}\downarrow$ to $V_{DS}\uparrow$ turn off			430		
$t_r$	Rise time, $V_{DS}$			90		
$t_f$	Fall time, $V_{DS}$			180		
$Q_g$	Total gate charge	$V_{DD} = 48\text{ V}$ , $I_D = 1\text{ A}$ , $V_{GS} = 10\text{ V}$ , See Figure 3		5.1	6.4	nC
$Q_{gs(\text{th})}$	Threshold gate-to-source charge			0.5	0.63	
$Q_{gd}$	Gate-to-drain charge			2.75	3.4	
$L_D$	Internal drain inductance			5		nH
$L_S$	Internal source inductance			5		
$R_g$	Internal gate resistance			500		$\Omega$

### thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power			72	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-case thermal resistance	All outputs with equal power			4	
		One output dissipating power			7	

# TPIC2601 6-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

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## PARAMETER MEASUREMENT INFORMATION

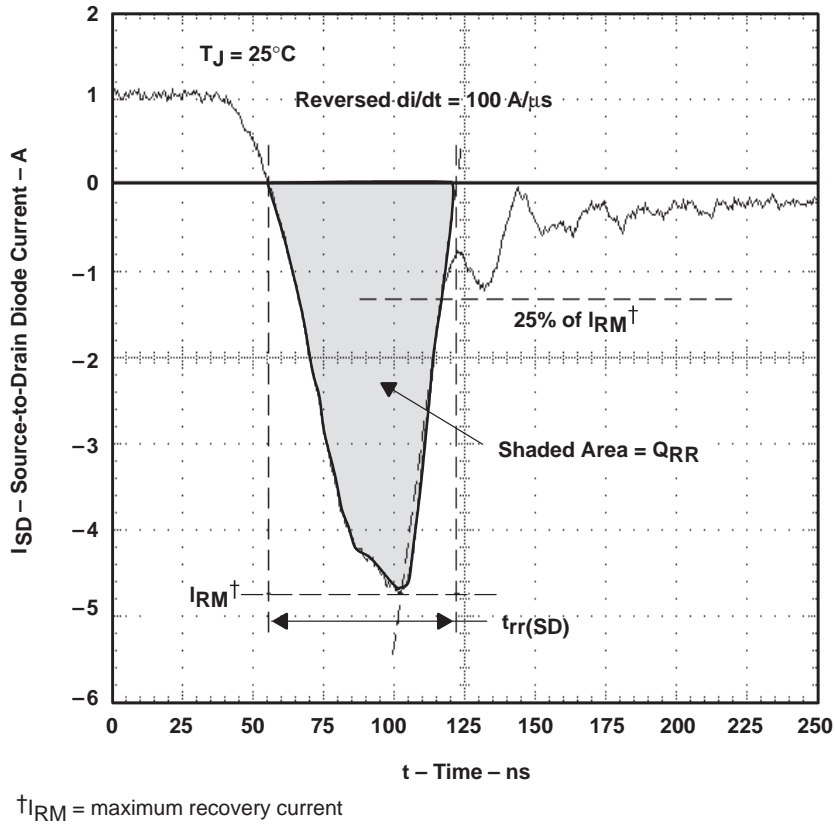
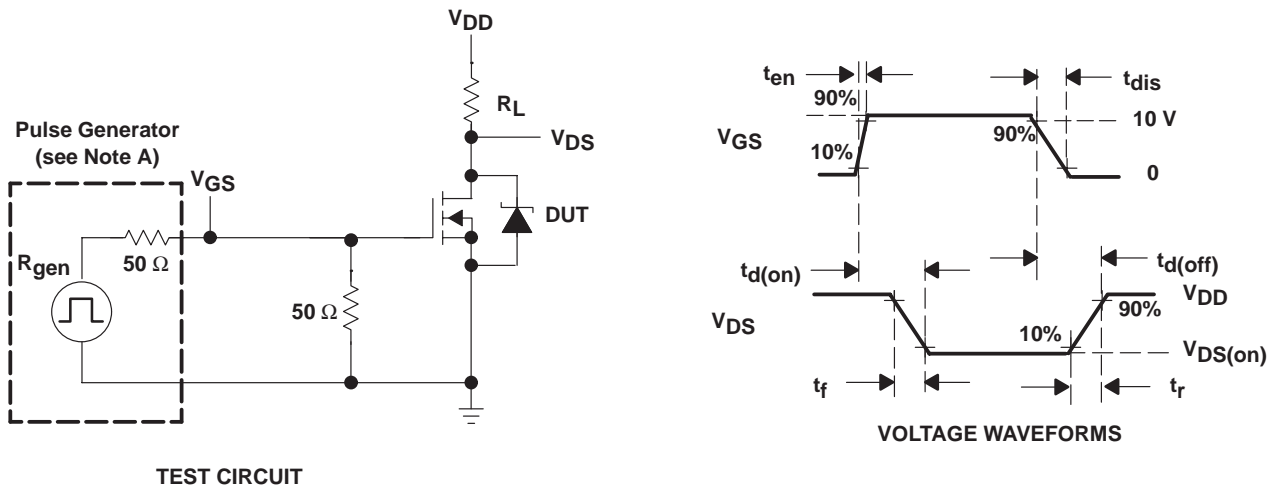


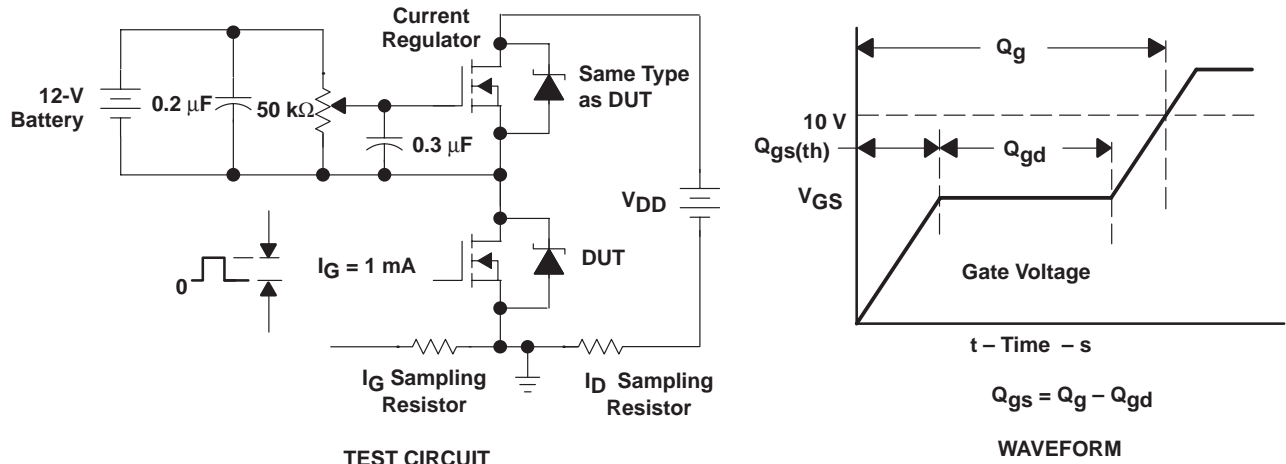
Figure 1. Reverse-Recovery Current Waveform of Source-to-Drain Diode



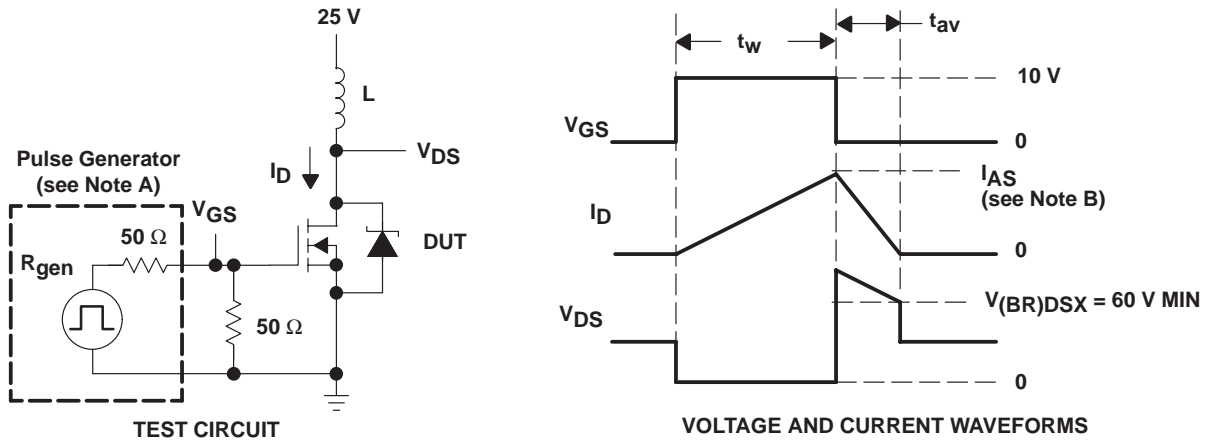
NOTE A: The pulse generator has the following characteristics:  $t_{en} \leq 10 \text{ ns}$ ,  $t_{dis} \leq 10 \text{ ns}$ ,  $Z_O = 50 \Omega$ .

Figure 2. Resistive Switching

**PARAMETER MEASUREMENT INFORMATION**



**Figure 3. Gate Charge Test Circuit and Waveform**



- NOTES: A. The pulse generator has the following characteristics:  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ ,  $Z_O = 50 \Omega$ .  
 B. Input pulse duration ( $t_w$ ) is increased until peak current  $I_{AS} = 2 \text{ A}$ .

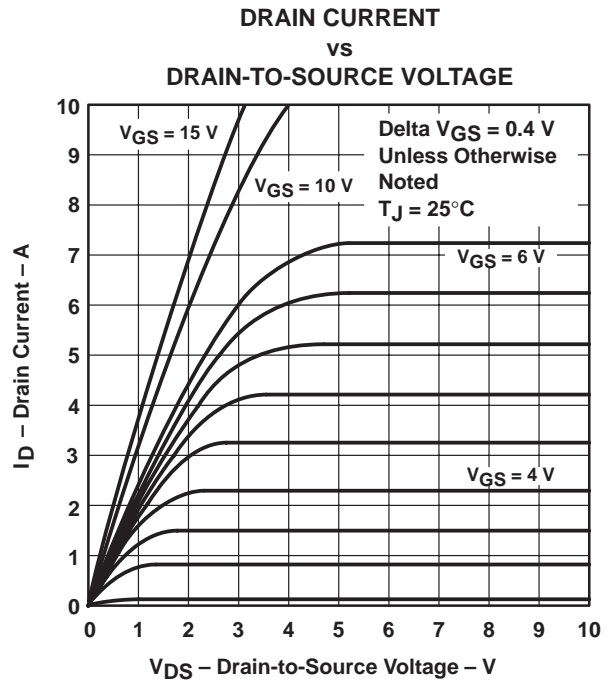
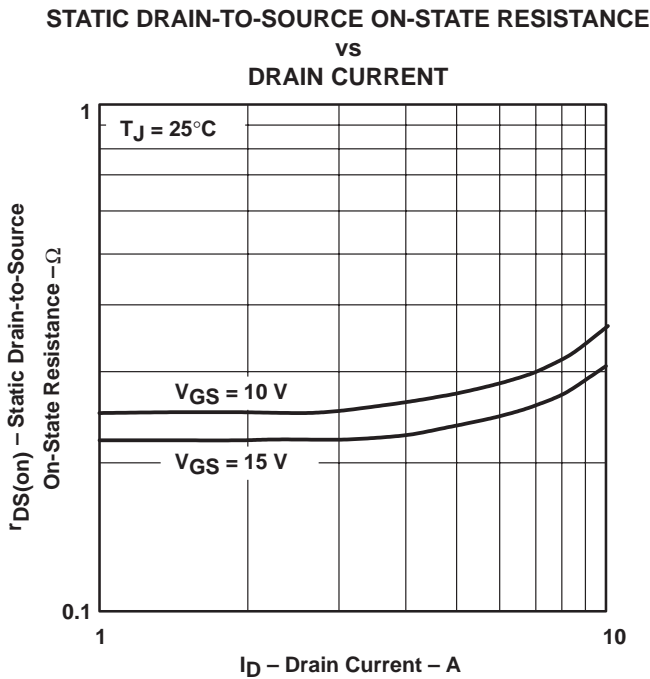
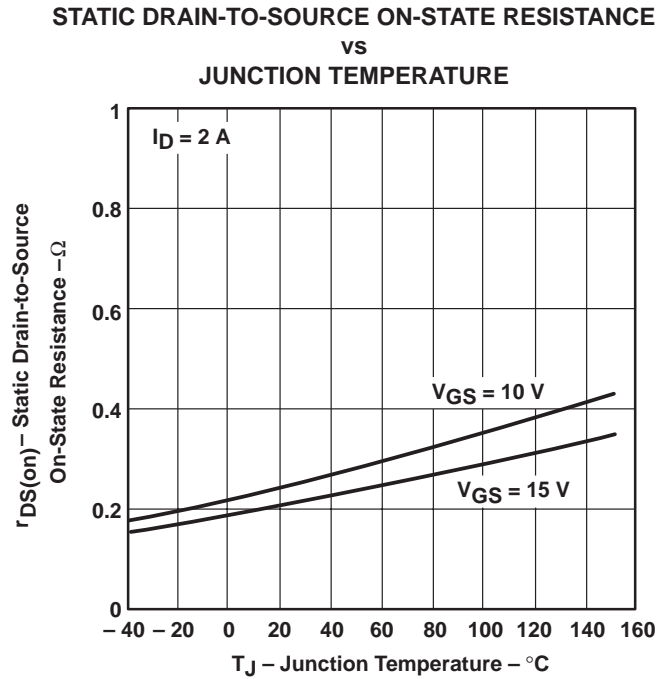
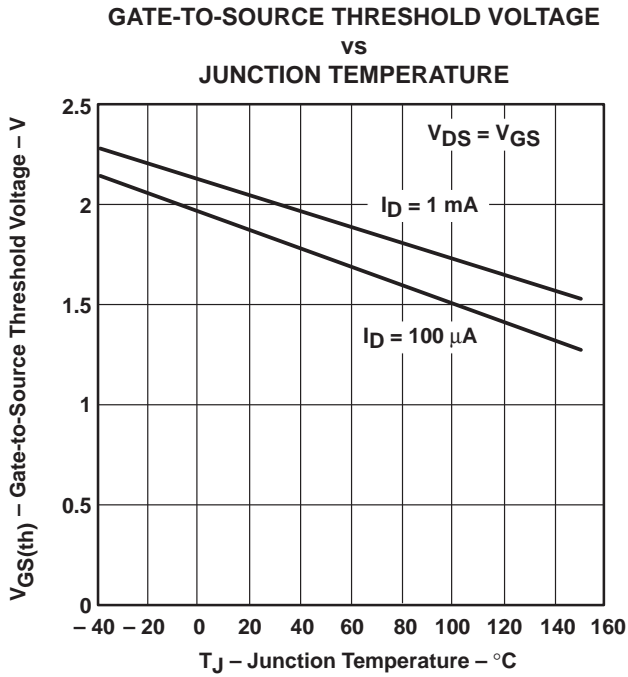
Energy test level is defined as 
$$E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 105 \text{ mJ minimum where } t_{av} = \text{avalanche time.}$$

**Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms**

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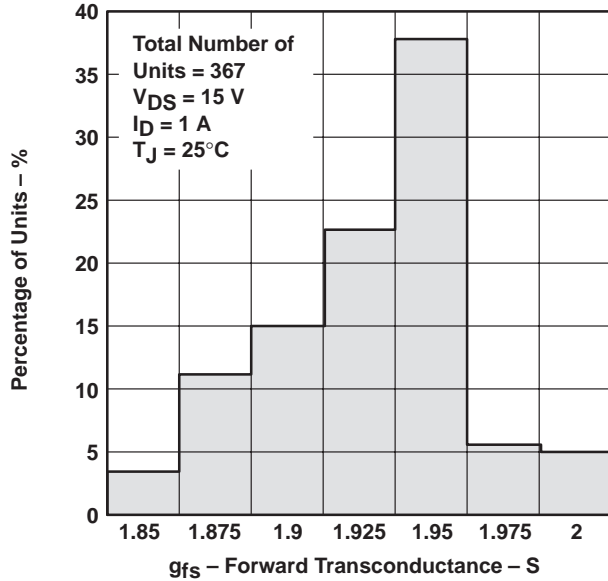
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## TYPICAL CHARACTERISTICS



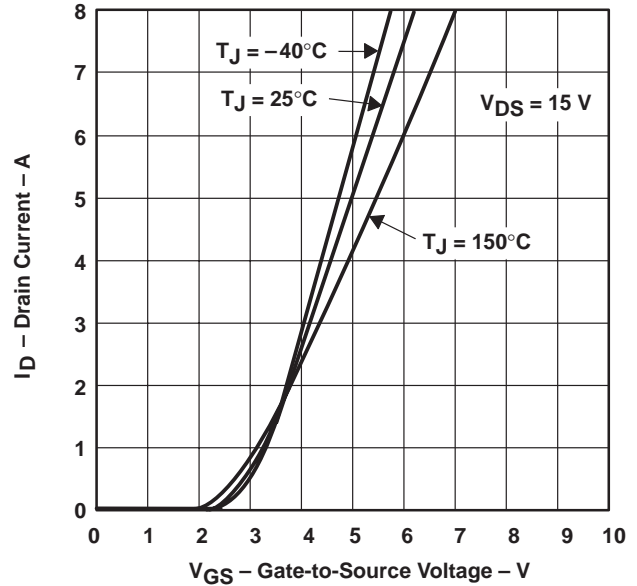
**TYPICAL CHARACTERISTICS**

**DISTRIBUTION OF FORWARD TRANSCONDUCTANCE**



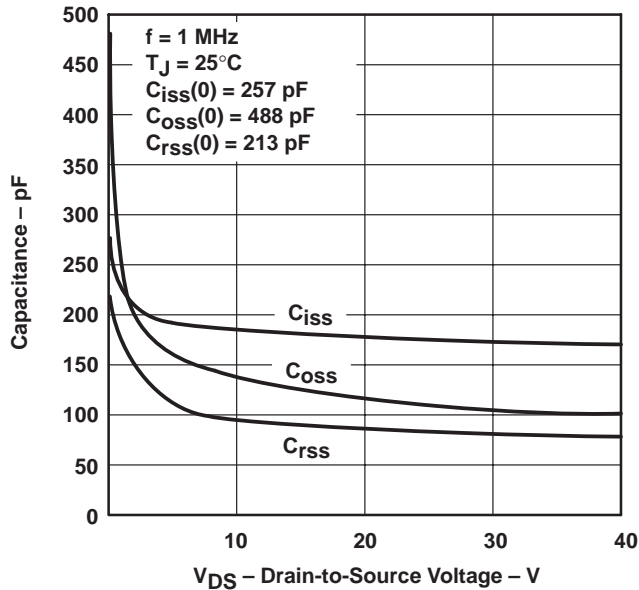
**Figure 9**

**DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE**



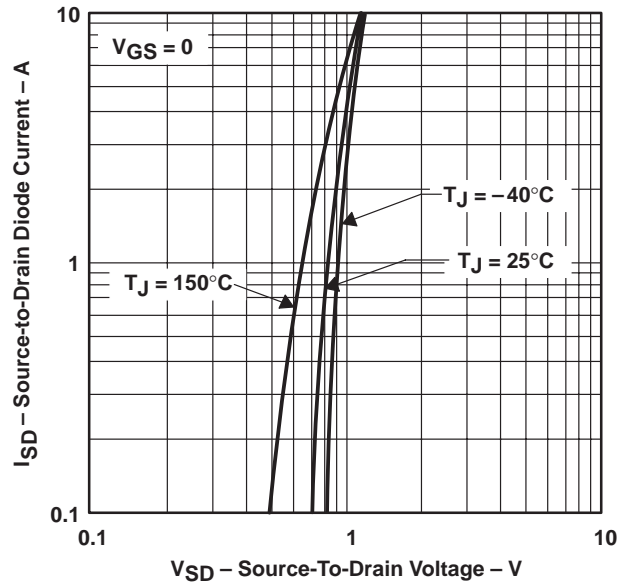
**Figure 10**

**CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE**



**Figure 11**

**SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE**



**Figure 12**

# TPIC2601 6-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

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## TYPICAL CHARACTERISTICS

**DRAIN-TO-SOURCE VOLTAGE AND  
GATE-TO-SOURCE VOLTAGE  
vs  
GATE CHARGE**

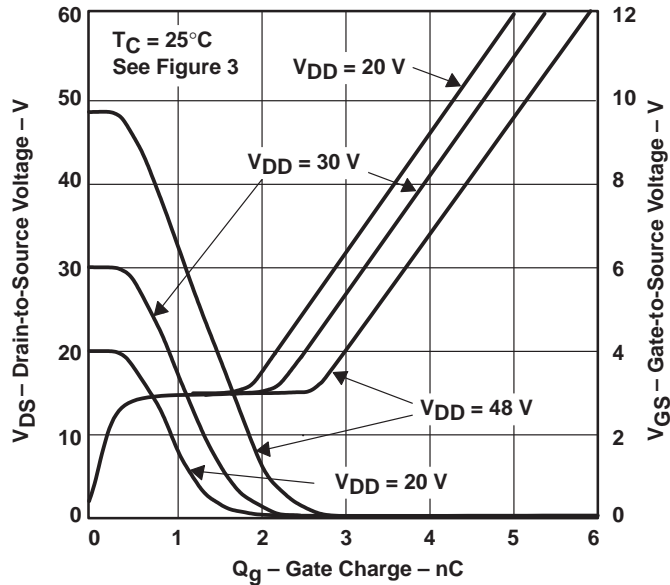


Figure 13

**REVERSE-RECOVERY TIME  
vs  
REVERSE di/dt**

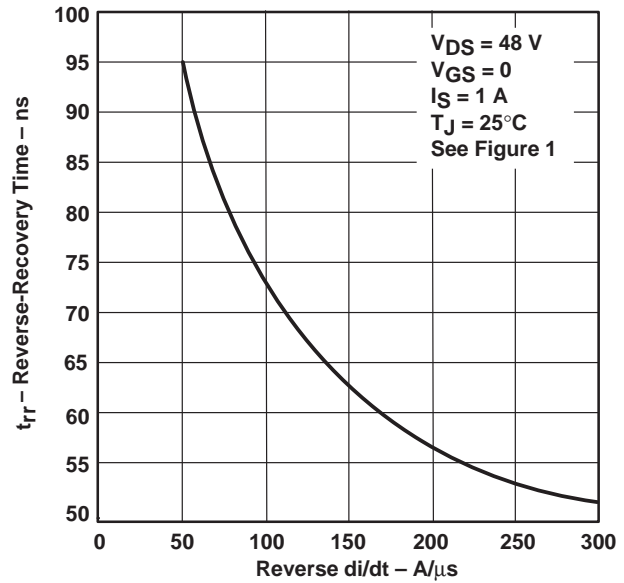


Figure 14

**MAXIMUM DRAIN CURRENT  
vs  
DRAIN-TO-SOURCE VOLTAGE**

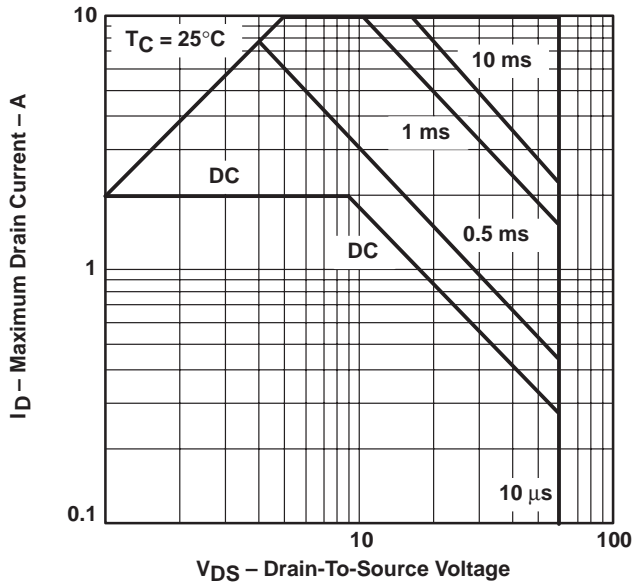


Figure 15

**MAXIMUM PEAK AVALANCHE CURRENT  
vs  
TIME DURATION OF AVALANCHE**

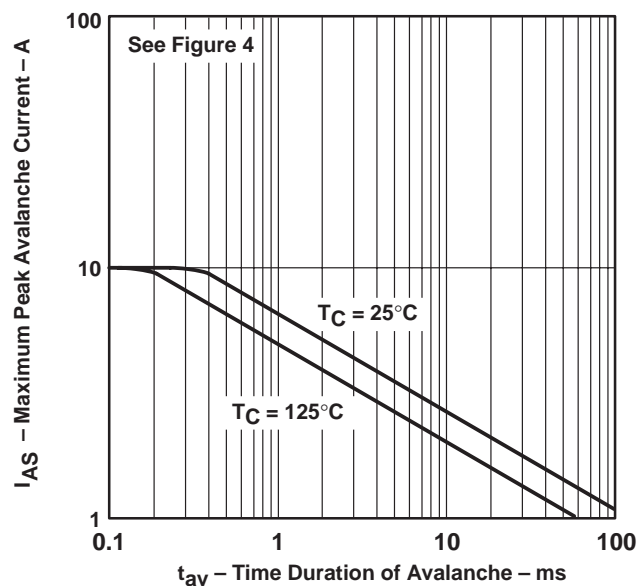


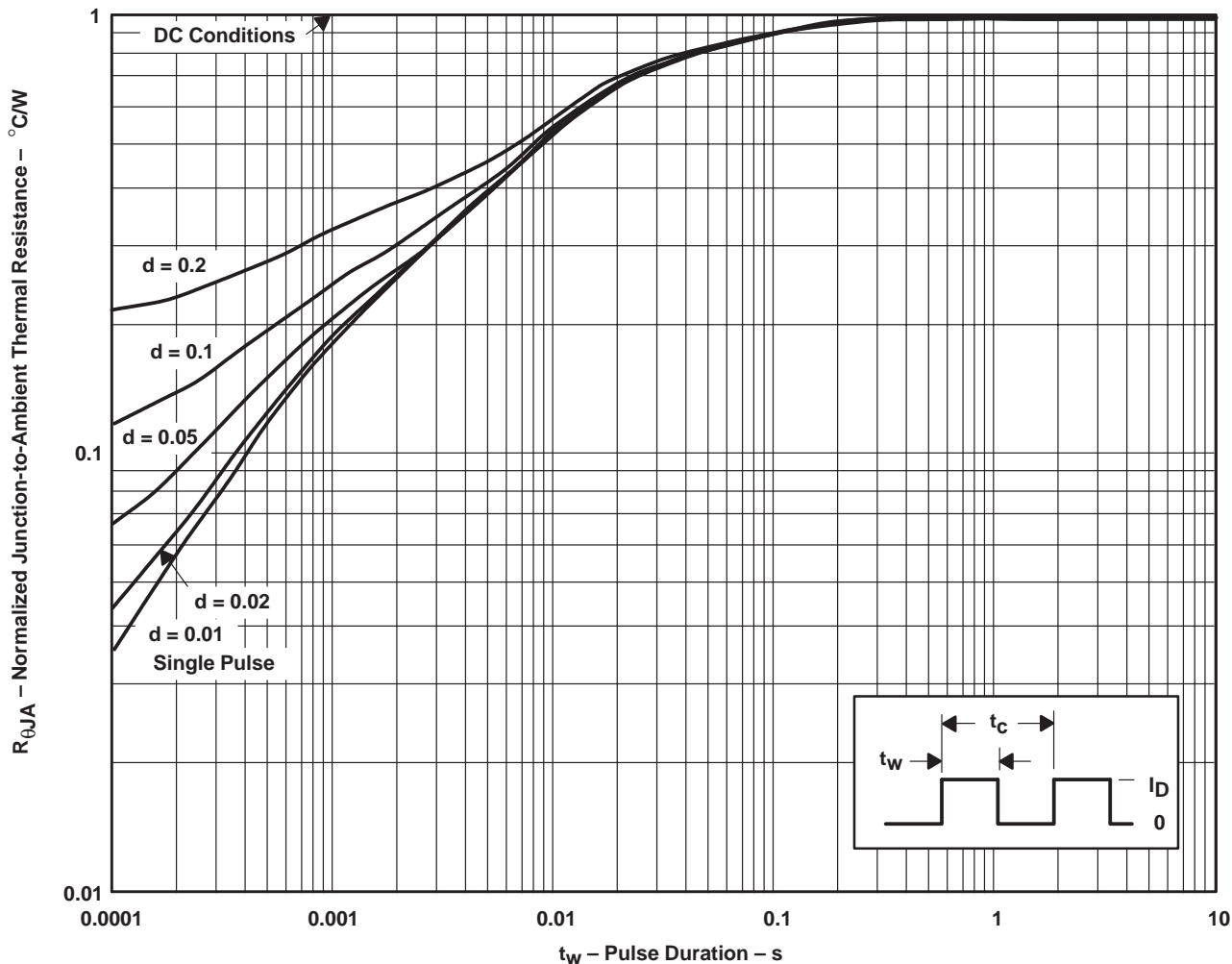
Figure 16





THERMAL INFORMATION

KTC PACKAGE†  
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE  
VS  
PULSE DURATION



† Device mounted on 24 in<sup>2</sup>, 4-layer FR4 printed-circuit board with no heatsink.

NOTE A:  $Z_{\theta A}(t) = r(t) R_{\theta JA}$   
 $t_w$  = pulse duration  
 $t_c$  = cycle time  
 $d$  = duty cycle =  $t_w/t_c$

Figure 17

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