

Linear Products

DC Brush Motor Control Using the TPIC2101

In many applications, a key design goal is to minimize variations in power delivered to a load as the supply voltage varies. This application brief describes a simple DC brush motor control circuit using the Texas Instruments TPIC2101 to maintain a constant effective voltage across the motor.

The TPIC2101 is a pulse-width modulated (PWM) power FET predriver used for speed control of DC brush motors. It can also be used for other applications requiring PWM. The device has three states: sleep state, run state, and fault state.

The sleep state is the power conserving state. The run state is the normal operating state of the device. Fault state is entered when the device detects an over voltage or over current condition. The device features two input modes (Manual and Auto), soft start, over/under voltage protection, and the ability to limit the power dissipation of an externally driven device.

Theory of Operation

Figure 1 illustrates a fan motor circuit used in an automobile application. The TPIC2101

SYSTEM BENEFITS

- ▼ Constant Load Voltage
- ▼ Over Voltage/Current Protection
- ▼ Low Power Consumption During Sleep State
- ▼ Built-In Soft Start

generates a pulse width drive to an external power NMOS transistor which is proportional to the input signal while also compensating for

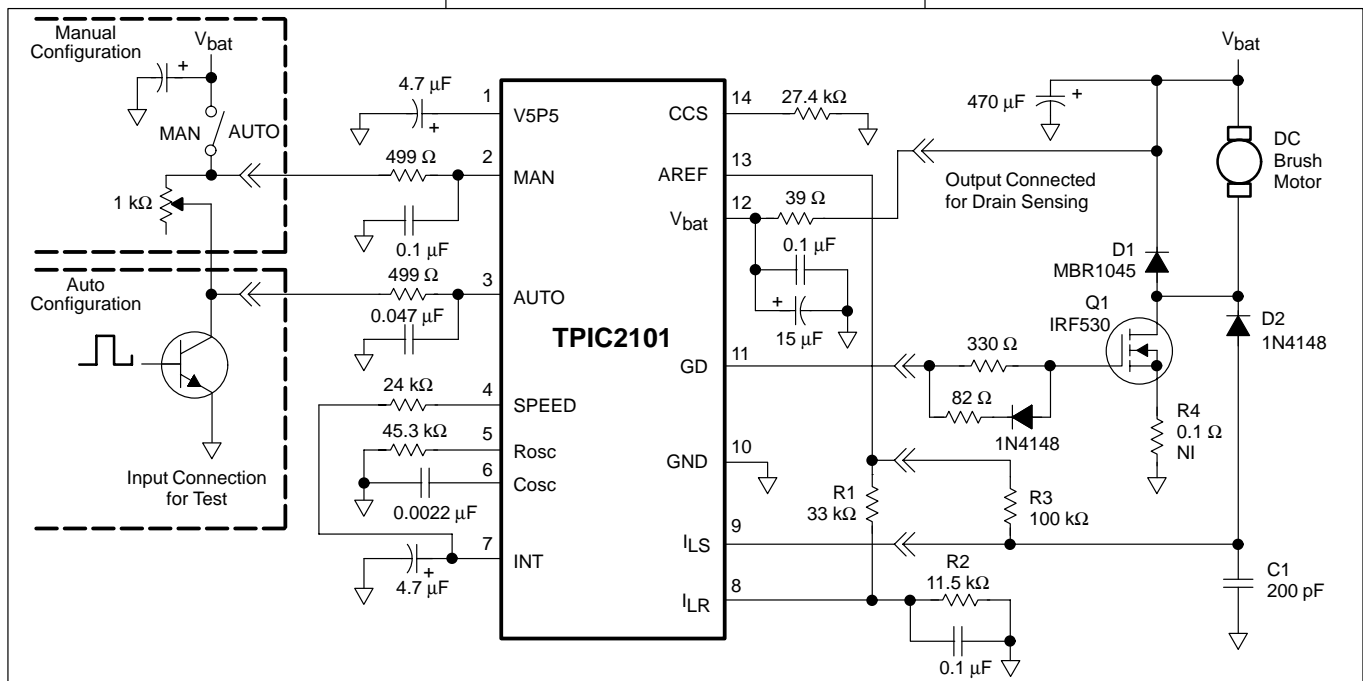


Figure 1. Fan Motor Schematic with PWM Speed Control

supply voltage changes. For a detailed description of each pin, refer to the TPIC2101 data sheet.

Operation Modes

Auto Mode

To assert the Auto mode, an open collector PWM signal is used to pull the AUTO pin low while the MAN (manual) pin is open. The input PWM frequency required is approximately 100 Hz. This signal is conditioned by the internal circuitry and becomes an output at the SPEED pin. An external RC integrates this signal, which then becomes the input for the INT (integrator) pin. At the INT pin a DC voltage of 0.72 V to 4 V corresponds to an input pulse width from 100% to 0% as seen at pin 3, and will generate an output PWM drive signal at the GD (gate drive) pin varying from 18% to 100% depending on the supply voltage, (Vbat). The output gate drive frequency is approximately

20 kHz. The output pulse width in Auto mode is determined by the formula, $PWM_{out} = ((2.88 + 13.12(1 - \text{input duty cycle})) / V_{bat}) * 100\%$. Figures 2 and 2A demonstrate the Auto mode operation.

Figure 2 shows the input configuration for Auto mode. Figure 2A shows the relationship between PWM in (input PWM at the base of the NPN transistor) and Veff (effective motor voltage).

Manual Mode

To assert Manual mode, the MAN pin is pulled high, and the voltage difference between the MAN and AUTO pins, 0 V to 2.2 V, determines the IC's output PWM drive signal of approximately 18% to 100% depending on Vbat. Just as in Auto mode, the input signal is conditioned by the internal circuitry, output at the SPEED pin, and via an external RC becomes an input of 0.72 V to 4 V DC at the

INT pin. Both the MAN and AUTO pins sink 2 mA in the Manual mode. Therefore, simply placing a resistor between the two pins will generate the required input signal. For example, a 1 kΩ potentiometer can be used to generate the 0 V to 2.2 V required for a full range output. The output pulse width in Manual mode is determined by the formula, $PWM_{out} = ((2.88 + 6.56(V_{man} - V_{auto})) / V_{bat}) * 100\%$. Figure 3 shows the input configuration for the Manual mode of operation. Figure 3A illustrates the relationship between the differential voltage (Vman - Vauto) and the effective motor voltage.

Note: In both Auto and Manual modes, the INT pin actually controls the output pulse width by comparing V_{COSC} and V_{INT}. When V_{COSC} is greater than V_{INT} the GD output is turned off. These waveforms are illustrated in Figure 5. The INT pin could be used as an input for some special applications not requiring the input signal conditioning

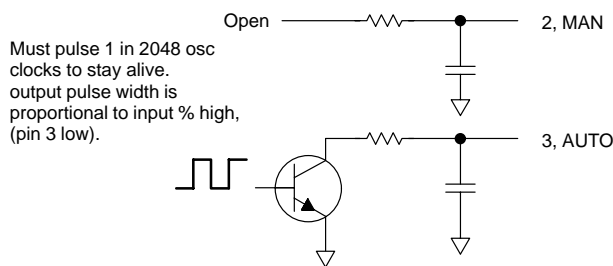


Figure 2. Auto Mode Input

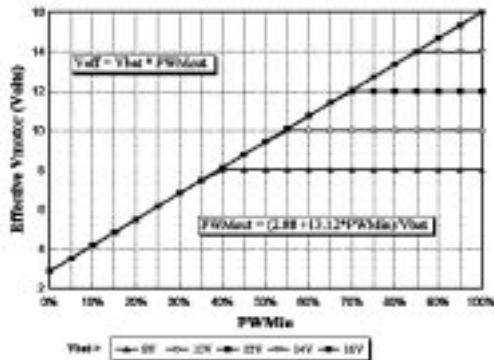


Figure 2A. Auto Mode Effective Voltage

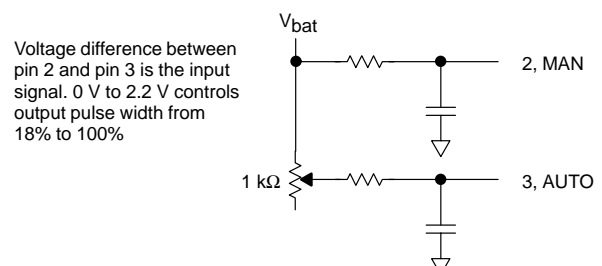


Figure 3. Manual Mode Input

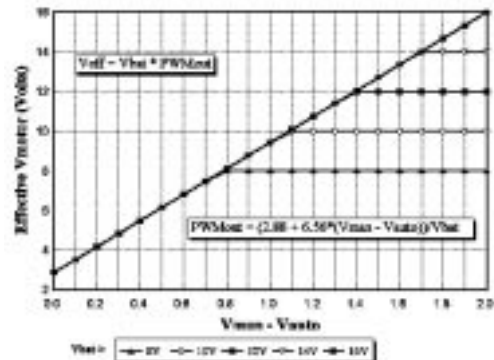


Figure 3A. Manual Mode Effective Voltage

by floating the SPEED pin and applying the input signal directly to the INT pin as shown in Figure 4.

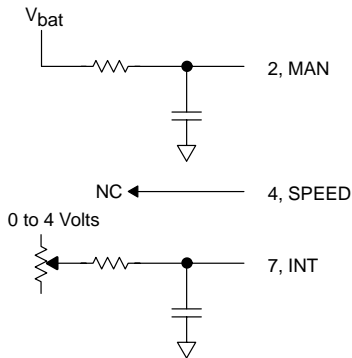


Figure 4. Aux Mode Method

Sleep State

When the integrated circuit is not in Run state it is in Sleep state. In this condition the supply current for the IC is reduced from a maximum of 10 mA to less than 200 μ A. The purpose of Sleep state is to preserve battery life when applicable.

Soft Start

In order to prevent abrupt application of power to the motor, the TPIC2101 includes a soft start feature that gradually ramps the output signal. When Run state is asserted, the output GD is increased in width from 0 to the commanded percent width over approximately 1 second. As previously discussed, the SPEED pin outputs the conditioned input signal, and the INT pin controls the IC's output pulse width. The resistor between the SPEED and INT pins has a minimum value of 20 k Ω , and the capacitor is selected for the start up time desired, usually 4.7 μ F for approximately 1 second to full on.

Figure 5 demonstrates the soft start feature for Manual mode. For this illustration a 1 k Ω resistor was

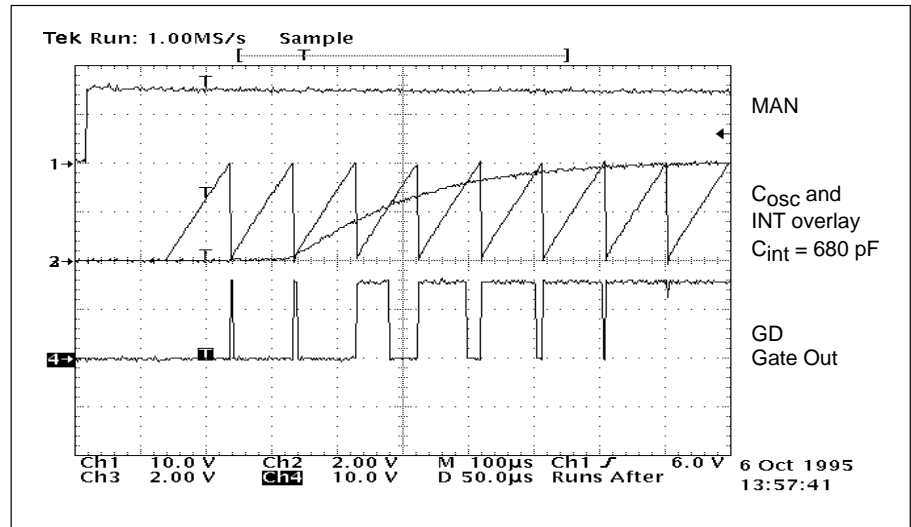


Figure 5. Soft Start

placed between the MAN pin and the AUTO pin to command a 100% output pulse width. The INT capacitor was reduced to 680 pF for a start up time of approximately 350 μ s (this short time is used to make the waveform more visible). On the top trace, the rising edge shows when Manual mode is asserted.

The second trace shows the oscillator which generates the output PWM frequency. The third trace is an overlay of trace two, and illustrates the rise time of the INT pin. The bottom trace shows the GD pulse width increasing from 0% to 100% as the INT pin voltage rises.

Under Voltage

Under voltage occurs when Vbat falls below 8 V. Under voltage conditions will cause the device to enter Sleep state with the gate drive held low. Recovery is automatic when Vbat increases approximately 1 V above the under voltage threshold. Hysteresis prevents the device from toggling in and out of Sleep state.

Fault States

Over Voltage

Over voltage is sensed by the Vbat pin internally and is not user adjustable. Over voltage occurs when Vbat rises between 17 V and 20 V. During over voltage condition, GD will be turned off and the device will enter Fault state. Recovery is automatic when Vbat decreases 0.5 V to 1 V below the over voltage threshold. Hysteresis will ensure that the condition does not toggle off and on near the threshold.

Over Current (limit)

If while the GD pin is high, I_{LS} (current limit sense) pin is higher than I_{LR} (current limit reference) pin, the internal circuitry will pull the INT pin low, thereby reducing the commanded output GD pulse width. This is on a pulse by pulse basis. This limits the power dissipation of the output device in the short term.

Over Current (fault)

If the above condition persists during the next 64,000 pulses, the

IC will enter Fault state with the GD held low for 64,000 pulses. At that time, one automatic restart will be attempted. If the Over Current condition occurs a second consecutive time, the IC will remain in Fault state until the device is cycled through a Sleep state to a Run state. This is accomplished when the input command is removed and reestablished. Note that 64,000 pulses at 20 kHz is approximately three seconds. The actual time will be proportional to the PWM frequency in use. For a more detailed description of the internal circuit refer to the TPIC2101 data sheet.

Figures 6–8 illustrate the device’s response to overload conditions using a drain sense configuration. Refer to Figure 1 for the detailed schematic. Figure 6 demonstrates normal operation without overload. The top trace shows the current in the lead to the INT capacitor. The second trace shows the voltage at the I_{LS} pin. The voltage at the I_{LS} pin rises from zero at the beginning of each pulse at a rate determined by R3 and C1 until it reaches one diode drop above the drain voltage of the external transistor. This is compared by the internal circuitry to the voltage set at the I_{LR} pin. This reference voltage is set by the voltage divider R1/R2 from V_{AREF} . The third trace shows the drain current of the external transistor well under the threshold setting determined by the reference voltage. The bottom trace shows the GD voltage.

In Figure 7, the load has been increased to the threshold setting. The top trace shows that the internal circuit is pulling current out of the INT capacitor which lowers the demand voltage at the INT pin.

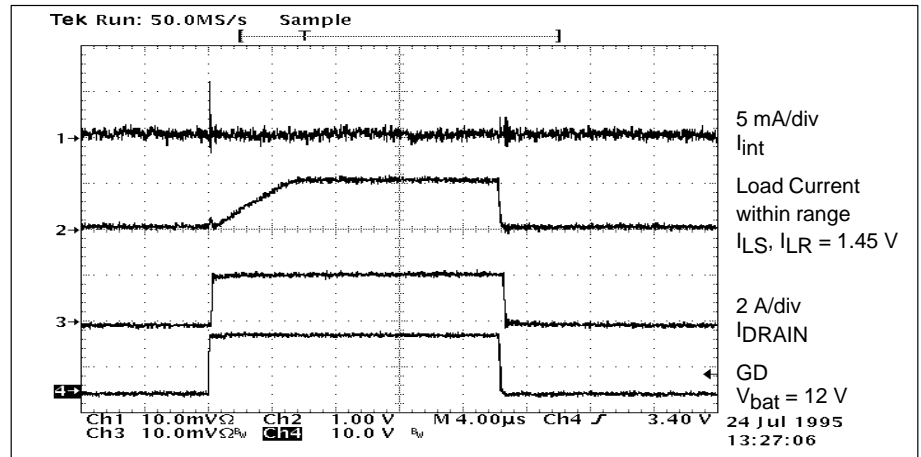


Figure 6. Normal Run State

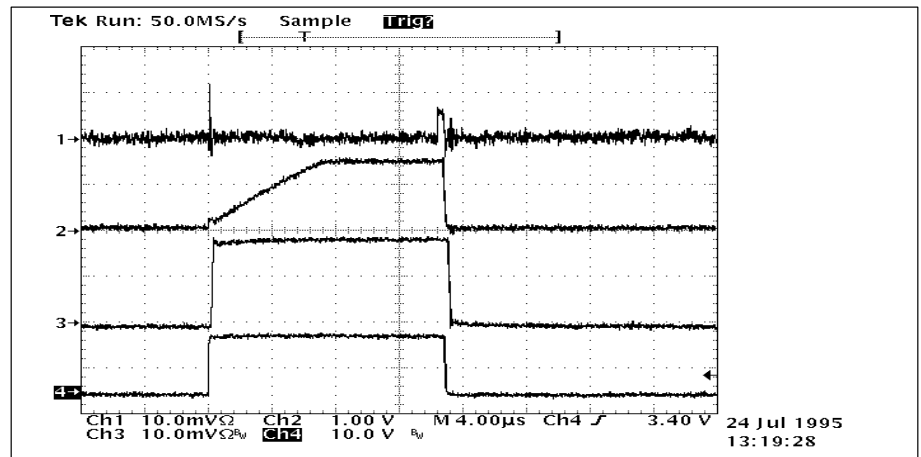


Figure 7. Run State at Threshold

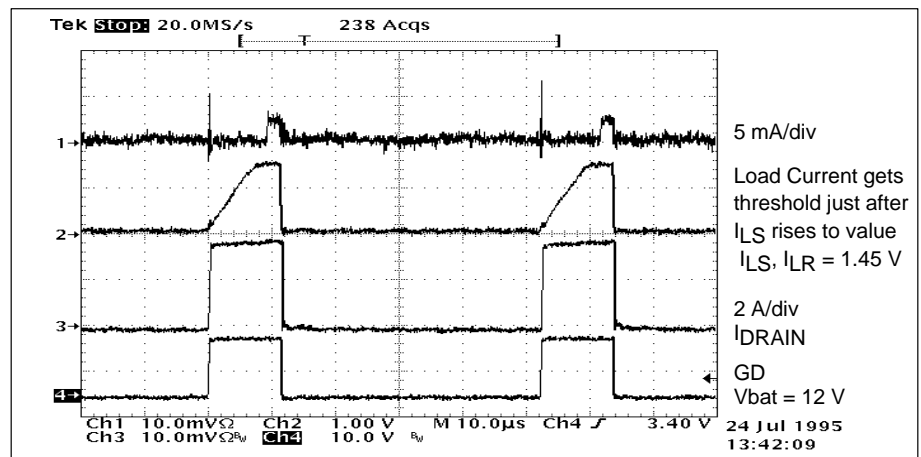


Figure 8. Run State Over Threshold

The second trace is reaching the threshold set by the I_{LR} pin. The third trace shows the drain current at the higher level, and the bottom trace reflects the narrower drive signal, as compared to Figure 6.

Figure 8 illustrates the effect of an additional load increase. As the load continues to increase, the pulse width is substantially reduced. If the load continues to increase until the pulse width is less than the rise time of the sensing voltage at the I_{LS} pin (determined by R3 and C1), overload detect is no longer functioning, and a minimum pulse width has been reached. Therefore, the components should be selected to obtain the minimum width required for starting the motor, within the 64,000 pulses (approximately 3 seconds), or a fault will be sensed. On the other hand, the pulse cannot be so wide that it allows the external transistor to exceed its power rating.

Run State

Although other output methods can be used, this brief summarizes Run state using the drain voltage sensing method. Referring to the

overall schematic Figure 1, the GD pin goes high turning the external transistor full on for a time equal to the commanded pulse width. During that time current flows through the motor and transistor. When GD goes low, the transistor turns off, but the current in the motor continues to flow by way of the recirculation diode, D1, using the energy stored in the motor inductance.

When GD is low, the I_{LS} pin is held low internally. When GD goes high, capacitor C1 starts charging through R3 from AREF, and the voltage at I_{LS} rises until it is clamped by forward biasing diode D2 to the drain of the external transistor Q1. Therefore, during the on time, the voltage at the I_{LS} pin becomes, $V_{ILS} = I_D * (R5 + R_{DS(on)}) + V_{FD1}$,
 $I_D =$ drain current = 3.6 A (at desired trip point)
 $R4 = 0.1 \Omega$ (This non-inductive resistor is used for monitoring the current. It is not required for this connection, but must be considered if there)
 $R_{DS(on)} = 0.1 \Omega$ (On resistance at 3.6 A from IRF530 data sheet)

$V_{FD1} = 0.7$ V (Diode forward voltage) Using these component values, $V_{ILS} = 1.42$ V. Also, if the bias at the I_{LR} pin is set by divider R1, R2 from AREF to a value of 1.45 V, overload will trip at 1.45 V ± 10 mV.

The advantage of drain sensing is that the output device is power dissipation limited. As power dissipation increases, the temperature of the external FET also increases. This rise in temperature results in a higher $R_{DS(on)}$. Therefore, since $V_{DRAIN} = I_{DRAIN} * R_{DS(on)}$, V_{DRAIN} , which is being sensed, responds to that increase. The disadvantage of this method is that the characteristics of the external transistor, such as V_{SAT} drain-to-source, must be considered when selecting the FET.

Conclusions

The TPIC2101 provides a cost effective means of maintaining a constant effective voltage in DC motor applications.



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