TEXAS INSTRUMENTS

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Automotive Fuel Injector Control Using Power+™ Control with Power+ Arrays™ Devices

The automotive industry is faced with increasingly strict environmental regulations which require that automotive module designs include real-time monitoring and off-line fault isolation. These requirements demand that protection and fault diagnostics be present in the module to help monitor emission levels and maintain system reliability. One area that is very sensitive to these requirements is the automotive powertrain. With today's highly specialized fuel systems, fuel injector drive is of key interest.

Texas Instruments has introduced four new devices, the TPIC46L01/02 and TPIC44L01/02, that are well-suited for fuel injector control applications. The 6-channel TPIC46L01/02 and the 4-channel TPIC44L01/02 are low-side pre-FET drivers capable of serial or parallel interface. These predrivers, which can control either TI's Power+ Arrays™ or discrete power FET's, allow the system designer the flexibility to select the power stage that best fits the particular system load requirements.

A typical engine control unit (ECU) is shown in Figure 1. The ECU receives sensor and control inputs from the engine and drives medium-current loads that require protection and fault diagnostics. In a typical engine control module, loads such as relays, lamps, and solenoid-controlled valves may be driven by TI's TPIC2603, 6-channel low-side power driver. The TPIC0107 or TPIC0108, H-bridge driver can control the throttle and idle speed. The fuel injector drive is accomplished by the TPIC46L01 or TPIC46L02, 6-channel pre-FET driver, in conjunction with the TPIC2601, 6-channel Power+ Array. This application is discussed in greater detail below. The configuration of the TPIC44L01 or TPIC44L02, 4-channel pre-FET drivers, in conjunction with the TPIC2401, 4-channel Power+ Array will be discussed at the end of this application brief.

SYSTEM BENEFITS

- Design flexibility to select power output stage that matches system load requirements
- Parallel input interface to provide real-time control of outputs
- Fault diagnostics to increase fault isolation capability

Application Overview

The TPIC46L01/02 offers serial interface to the microcontroller to transfer control data to the driver and output fault data back to the controller. The pre-FET driver

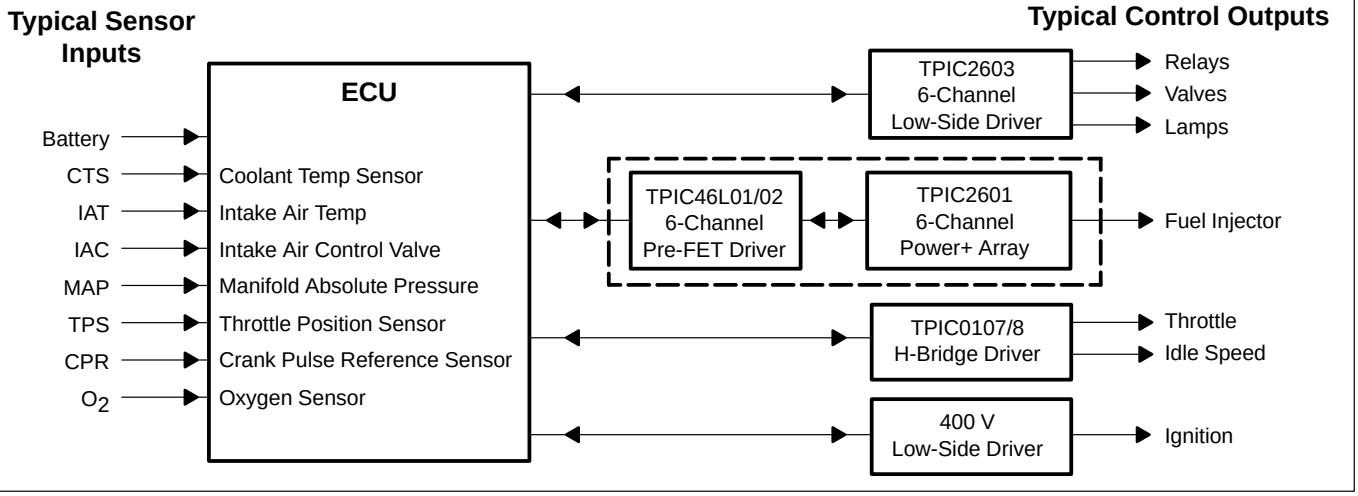


Figure 1. ECU Block Diagram

may be cascaded to minimize interconnects to the microcontroller, hence reducing costs. When using this configuration, serial data is input to the device and is transferred out the serial data output (SDO) terminal following the fault data.

For the power drive, TI offers the TPIC2601, a 6-channel common-source power DMOS array with gate protection. Coupled with the TPIC46L01/02, it provides power and protection capabilities for switching medium-current loads. The TPIC46L01/02 and TPIC2601 combination provides effective switching of the fuel injectors by means of a parallel load interface, fault detection and protection, and an efficient power output stage. Fault isolation features included in the TPIC46L01/02 are shorted and open-load detection, and over and under-battery voltage shutdown; all are real-time fault indicators via a fault interrupt to the microcontroller. Load fault protection is provided by disabling the gate output for the TPIC46L01 or transitioning to a low duty cycle pulse-width-modulated (PWM) state for the TPIC46L02.

To enable parallel data transfer, data is transferred directly from the parallel interface inputs (IN0–IN5) to each respective gate output asynchronously. The channel is turned ON with a logic high and OFF with a logic low. The parallel input port and serial control data are OR'ed in the output control register to allow either interface to control the gate outputs. While the serial interface is not required for parallel control, it is still available to transfer fault data back to the microcontroller.

Normal Operation of a Fuel Injector

Microcontroller inputs are provided to the predriver via the parallel input terminals as shown in Figure 2. To turn an output on, the appropriate parallel input is transitioned from low to high. Trace 1 of Figure 3 shows an example waveform for the IN0 input. Trace 2 shows the corresponding gate drive output GATE0. The waveform in trace 3 illustrates that the power transistor drain current (DRAIN0), i.e. injector current, rises at a rate determined by the injector inductance and the battery voltage. It continues to rise until the maximum value is reached, a result of the injector resistance. Once the injector is turned off, the magnetic field collapses inducing a voltage at DRAIN0 node of the power transistor. This voltage (trace 4) then rises until it is clamped at approximately 55 V.

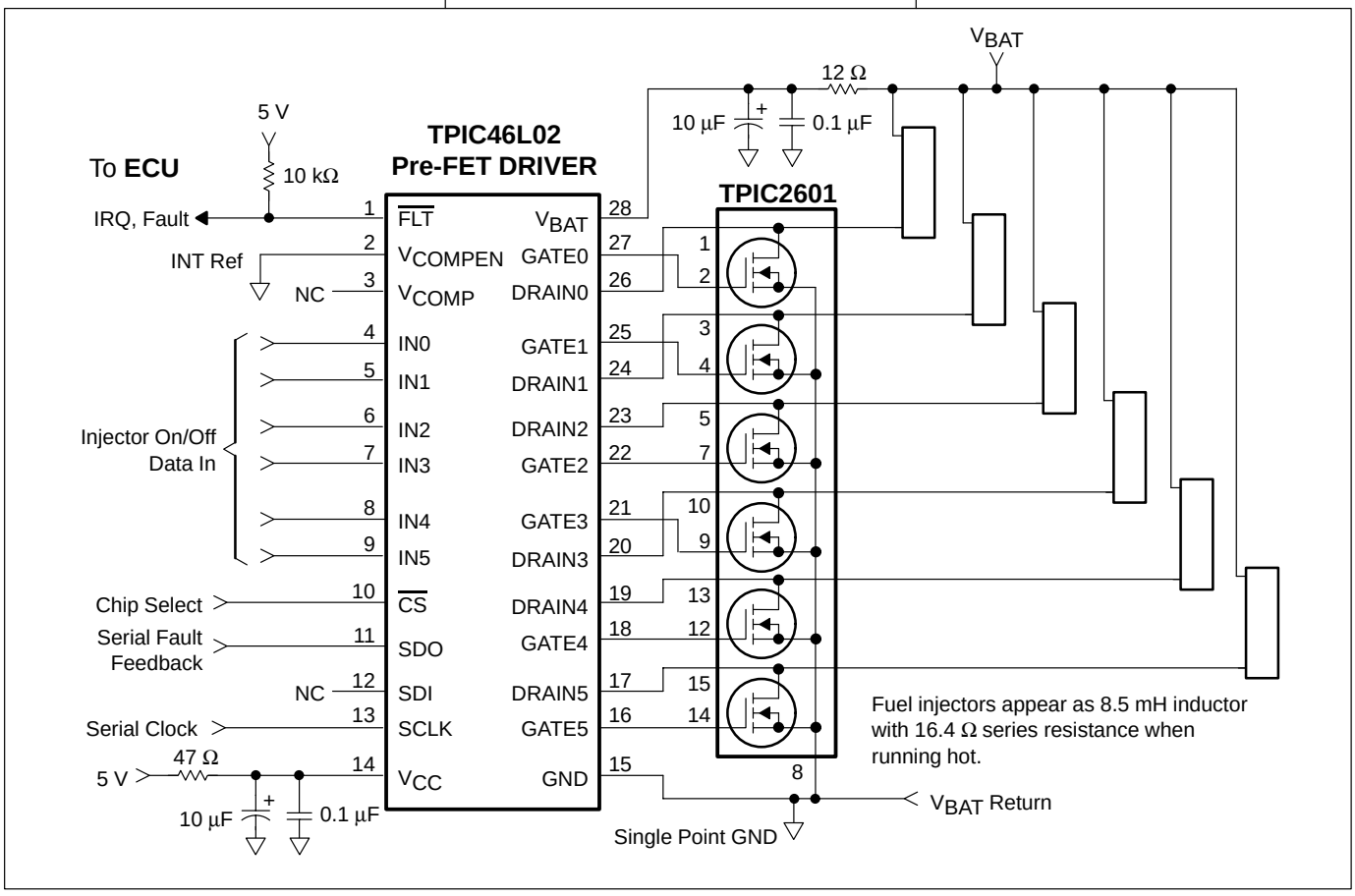


Figure 2. Circuit Schematic of the TPIC46L02 Pre-FET Driver and the TPIC2601 Power+ Array

The predriver monitors the drain voltage of the FET to detect fault conditions and the inductive transient. The drain inputs are used in an internal clamp, or "snub", circuit to pull up the gate. This snub circuit turns the output on to dissipate the energy stored in the injector and prevent the drain voltage from exceeding the maximum V_{DS} of the power transistor. Once the gate voltage has fallen, a delay of approximately 125 µs is observed before the gate turns off completely. Trace 2 of Figure 3 shows the gate pull-up due to the inductive transient.

Fault Isolation

The TPIC46L01/02 offers fault isolation to meet emission control requirements placed on today's engine control systems. The real-time monitoring comes in the form of a fault interrupt line ($\overline{FLT}$). After the $\overline{FLT}$ goes low, the microcontroller can check the serial diagnostic data to isolate the channel at fault. As can be seen in Figure 4, the output controlled by IN4 (trace 4) is shorted and the output controlled by IN0 is open. During normal operation, $\overline{CS}$ is held high to disable the serial interface and to allow the device to monitor the fault status of the load. The fault register status is locked on the falling edge of $\overline{CS}$ and diagnostic data is transferred out of SDO on the falling edges of SCLK.

For the TPIC46L01, a fault is captured when it occurs and is available on the SDO port whenever $\overline{CS}$ transitions low to enable the serial interface. As can be seen in Figure 5, the $\overline{FLT}$ goes low when the fault occurs and then remains low. When the fault occurs, the gate output turns off after 60 µs and remains off until the input is turned off and back on.

For the TPIC46L02 to capture a fault condition and have the fault data available at the SDO port, the $\overline{CS}$ must go low while the fault exists. The fault interrupt ($\overline{FLT}$) will remain active (see Figure 6) until cleared by $\overline{CS}$. When a shorted-load fault occurs, the gate drive output goes into a low duty cycle PWM mode and will remain there as long as the output is enabled and the fault condition is present. The $\overline{FLT}$ is refreshed when $\overline{CS}$ transitions low after the fault has been cleared.

A total of eight bits of fault status data are provided including bits for over-battery-voltage, under-battery-voltage, and shorted-load or open-load faults. As $\overline{CS}$ goes low, the first bit of fault status data (over-battery) is immediately available. The second bit of fault status data is transferred on the first high-to-low transition of SCLK with the remaining data transferred on the falling edges of the following six clocks. The $\overline{CS}$ input must be transitioned high after the eighth clock to load control data into the output buffer and re-enable fault reporting.

When using either the serial or parallel port for control, care must be taken to ensure that eight bits of data are clocked into the SDI port if $\overline{CS}$ transitions low. Less than eight bits of data may result in unknown data being transferred into the output control register as $\overline{CS}$ transitions high. To illustrate the fault status in trace 4 of Figure 4, there are two bytes of fault data shown, one indicating a short present at DRAIN4 and the other indicating an open at DRAIN0. As $\overline{CS}$ goes low, the bit representations are: left to right starting with the most significant bit to the least significant bit, over-battery (MSB), under-battery, and FLT5 to FLT0 (LSB).

Operation of a Shorted Injector

Among the faults monitored is that of a shorted injector. This fault is isolated only when the output transistor is on. Trace 4 of Figure 7 illustrates the drain of the output transistor controlled by IN0 shorted to V_{BAT}. IN0 (trace 1) transitions high as the output is commanded to turn

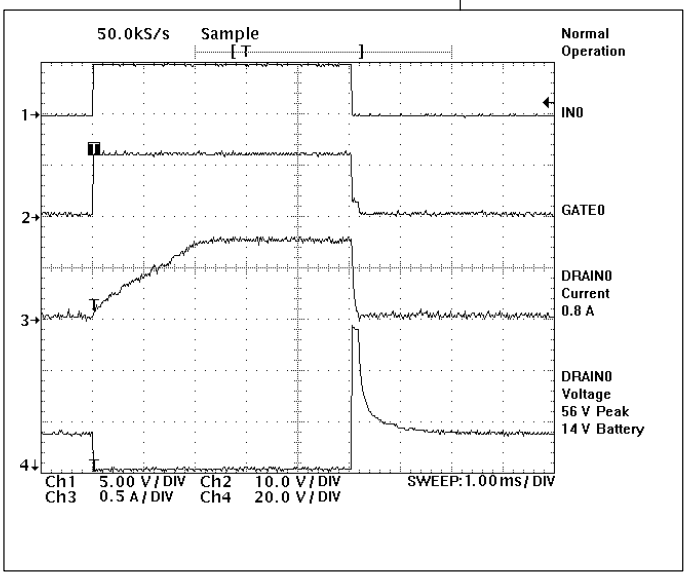
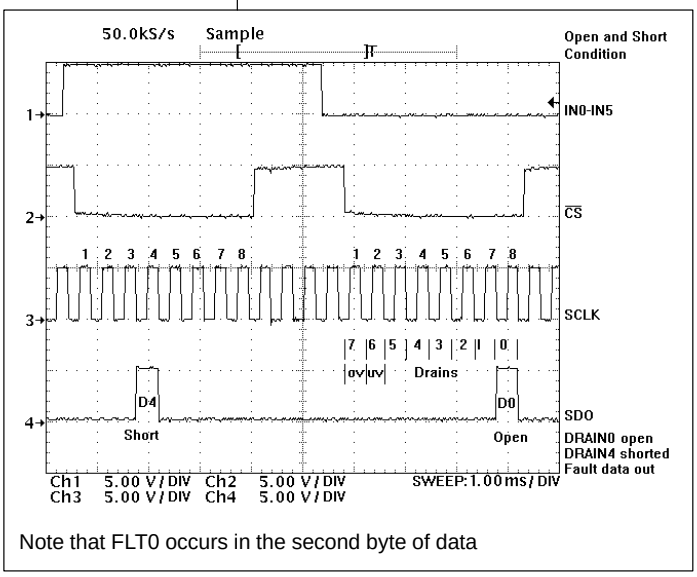


Figure 3. Drain Voltage and Current



Note that FLT0 occurs in the second byte of data

Figure 4. Open/Short-Fault Conditions

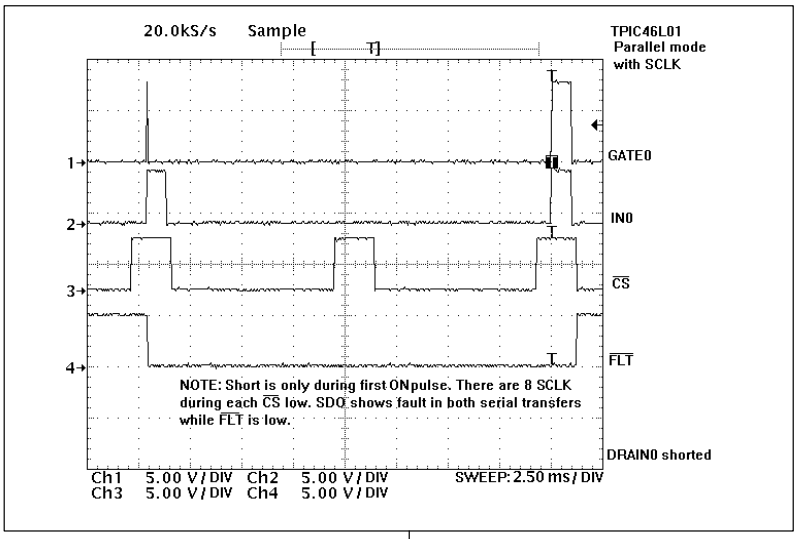


Figure 5. Fault is Captured

on. After the output is turned on, a delay of 60 µs is allowed for the output to stabilize. At this time, the drain voltage is compared to the fault reference threshold. If the drain voltage is greater than the reference of 1.25 V, then an over-current or shorted-load condition exists. The $\overline{FLT}$ (trace 3) is transitioned low to notify the microcontroller of the error.

The TPIC46L01 and TPIC46L02 handle shorted-load fault conditions differently. The TPIC46L01 flags the microcontroller that a fault condition exists and the gate output is automatically shut off until the microcontroller turns it back on. This reduces the on-time to approximately 60 µs, keeping the power dissipation within limits and preserving the output transistor. When the TPIC46L02 experiences a shorted-load condition, it transitions to a low duty cycle PWM state to automatically re-check the fault condition and protect the FET from over-heating. An example is shown in trace 4 of Figure 7. This mode continues until the error has been corrected or until the microcontroller turns the output off.

Operation of an Open Injector

The test for an open load is performed only when the output transistor is off. Under normal condition, the drain is pulled high by the load (see Figure 2). The drain inputs for unused channels must be pulled high to prevent false reporting of open load condition. An open load is checked by placing a 60 µA current source on the drains of each of the FET's. If the load impedance is high, the current source will be sufficient to pull the drain of the transistor below the 1.25 V reference threshold of the detection circuit. A deglitch time of 60 µs is provided to allow the drain to stabilize before the test is enabled. If an open-load fault is present, then a fault flag is issued to the microcontroller until the fault has been corrected.

Over/Under-Battery Voltage Detection and Shutdown

The predriver monitors the battery voltage to protect the load and power transistor from over-battery conditions. The over-battery voltage detection threshold is set at 34 V. The under-battery voltage threshold is set at 4.8 V to protect the output transistor and load from thermal stress. In both cases, the device disables all gate outputs as long as the battery fault condition is present. Shorted and open-load fault reporting is disabled until the battery voltage error has been corrected to ensure erroneous faults are not reported (see trace 4, Figure 8).

Fault Detection Threshold Reference

As mentioned previously, approximately 60 µs after a gate transition (i.e. the stabilization time), the drain voltage is compared to an internal reference of 1.25 V during the on/off time to check for a shorted/open output. In Figure 2, pin 2 of the TPIC46L01/02 is the voltage compare enable (V_{COMPEN}). This pin is grounded to select the internal 1.25 V reference. The pin is pulled high to select the external reference voltage compare (V_{COMP}) at pin 3. An external voltage can be used at this pin to set the fault threshold reference to a different value.

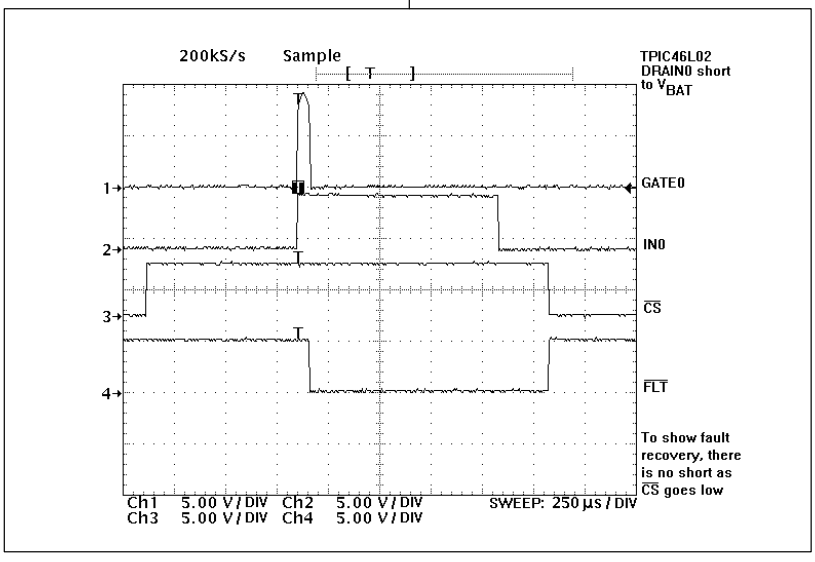


Figure 6. Fault Clears

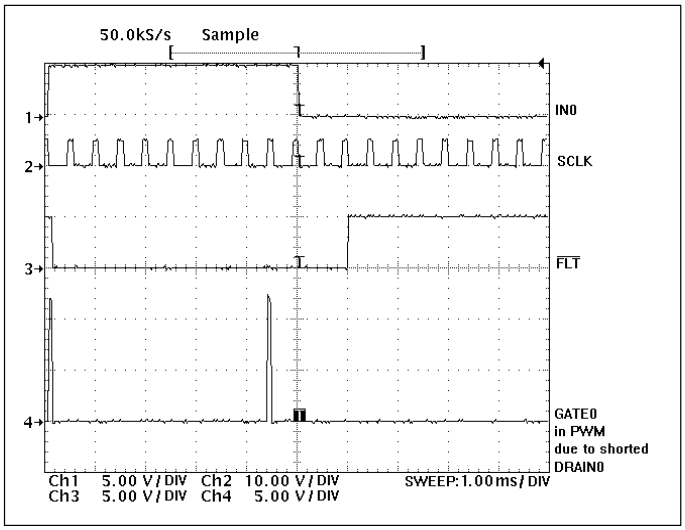


Figure 7. Shorted Drain

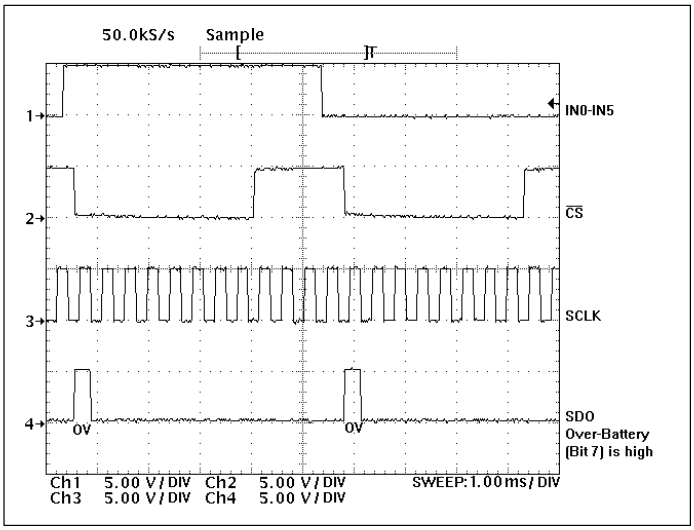


Figure 8. Over/Under-Battery Fault Conditions

Some designs may require a different current detection level to better match a particular power transistor's on-resistance or meet other system requirements.

System Power Dissipation

A key design consideration when selecting the power output stage for this particular application is power dissipation. The total power dissipation of the transistor array is the sum of the power in the on-state, plus the power resulting from the transient as the inductor is turned off, multiplied by the number of transistors in the array. To illustrate, values from Figure 3 waveforms and the TPIC2601 datasheet will be used. For simplicity, three worst case assumptions will be made. The first is that the drain current decays linearly when it is turned off. The second is that the maximum operating ambient temperature is 125°C. The third and final assumption is that a heat sink will provide a system thermal resistance, case to ambient, less than or equal to 5°C/W. The power dissipation parameters are given as follows:

f = frequency = 100 Hz
T_{on} = on-time = 50% or 5 ms
T_d = decay time = 125 µs
I_D = drain current = 0.8 A, same as peak injector current, I_P
V_{CL} = clamp voltage = 60 V
$R_{\theta JC}$ = thermal resistance junction to case = 4°C/W
$R_{\theta CS}$ = thermal resistance case to heat sink = 0.5°C/W
$R_{\theta SA}$ = thermal resistance heatsink to ambient = 4.5°C/W
V_{BAT} = battery voltage = 14 V
L_{IJ} = injector inductance = 8.5 mH
R_{IJ} = injector resistance = 16.4 Ω, hot
T_{Jmax} = maximum junction temperature allowed = 150°C
T_A = maximum ambient operating temperature = 125°C, assumed
T_C = case temperature
T_S = heat sink/temperature
P_{on} = power during on-time
P_d = power during current decay or switch off-time
$P_T = P_{on} + P_d$ = total power

Thermal Considerations for the Output FET Array

After defining the power parameters, the maximum allowed power that can be dissipated by the power array depends on (1) the ambient temperature at which it operates and (2) the thermal resistance from the FET junctions to that ambient. The result is as follows:

Equation 1: $(T_{Jmax} - T_A) / (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) = W$

Solution 1: (150°C – 125°C)/ (4°C/W + 0.5°C/W + 4.5°C/W) = 2.78 W*

*Total power for the package

Power Dissipation for a Single Transistor

The on and off-time power that is dissipated in the transistor is a function of the drain current I_D (trace 3) in Figure 3, $r_{DS(on)}$, and the snub voltage. The on-time power is the sum of the power during the ramp up (0 – 2 ms) = 2 ms and the power at the maximum value (2 ms – 5 ms) = 3 ms.

Equation 2: $P_{onramp} = 1/3\ I_D^2 * r_{DS(on)} * T_{onramp} * f$ (during ramp up time period)

Solution 2: $P_{onramp} = 1/3\ (0.8)^2 * 0.4 * 0.002 * 100 = 0.017$ W

Equation 3: $P_{onmax} = I_D^2 * r_{DS(on)} * T_{onmax} * f$ (during maximum value time)

Solution 3: $P_{onmax} = (0.8)^2 * 0.4 * 0.003 * 100 = 0.077$ W

Equation 4: $P_{on} = P_{onramp} + P_{onmax}$

Solution 4: P_{on} = 0.017 W + 0.077 W = 0.094 W

The off-time power is the power during current decay which can be seen in Figure 3 when observing the IN0 (trace1), the DRAIN0 current

I_D (trace 3), and the DRAIN0 voltage (trace 4) waveforms. The gate is held on for approximately 125 µs which clamps the drain voltage at 60 V while the current decays to zero. As stated previously, assuming linear decay as the worst case scenario, the power can be calculated if the information obtained from the drain current and voltage waveforms of Figure 3 is known. By integrating current over time and multiplying by the voltage, this will give the equivalent:

Equation 5: $P_d = V_{CL} * I_D / 2 * T_d * f$

Solution 5: $P_d = 60 * (0.8 / 2) * 0.000125 * 100 = 0.3$ W

If the information in Figure 3 were not yet available, i.e. the TPIC46L01/02 and TPIC2601 had not already been incorporated into the system, the calculation could be made from the data in the above table.

Equation 6: $P_d = f * (3 * L_{IJ} * I_D^2 * V_{CL}) / (6 * (V_{CL} – V_{BAT}) + 4 * R_{IJ} * I_D)$

Solution 6: $P_d = 100 * (3 * 0.0085 * 0.8^2 * 60) / (6 * (60 – 14) + 4 * 16.4 * 0.8) = 0.298$ W

From solutions 4 and 5 above, the total power for each transistor is:

Equation 7: $P_T = P_{on} + P_d$

Solution 7: $P_T = 0.094 + 0.3 = 0.394$ W

The power dissipated with all six FETs conducting is 6 * 0.394 W = 2.364 W. From Solution 1, it was determined that the total power capacity for the package is 2.78 W; therefore, all six power transistors can turn on simultaneously and operate below the maximum allowable junction temperature of 150°C.

TPIC44L01/02 and TPIC2401

Effective fuel injector drive can also be accomplished with the TPIC44L01/02 and TPIC2401. As mentioned earlier, the TPIC44L01/02 are 4-channel low-side pre-FET drivers capable of serial or parallel interface and the TPIC2401 is a 4-channel common-source power DMOS array with gate protection. There are slight differences between the 4-and 6-channel chipsets.

Cascading the TPIC44L01/02

The TPIC44L01/02 uses a 4-bit data word for serial transfers which allows the user to cascade two pre-drivers to communicate with 8-bit words. Cascading of the serial ports requires a minimum of 4 bits for the control information with serial word operation valid for any multiple of 4 bits. This could potentially double the serial throughput while sending and receiving data with the microcontroller. The first stage transfers its fault data through the second stage followed by control data. As with the 6-channel devices, the fault data is available immediately when $\overline{CS}$ transitions low to monitor the status of the SDO port. An example of 8-bit serial word operation can be seen in Figure 9 when observing the timing diagrams.

The use of a 4-bit serial word increases data throughput compared to 8-bit words. Due to the absence of the over/under-battery voltage bit reporting, serial data transfer of both fault data and control data information is more efficient and advantageous for 4-channel switching requirements.

The MSB of fault data is available first with the following bit representations from left to right, FLT7 to FLT0 (LSB). The 4-channel device offers real-time fault reporting by means of the $\overline{FLT}$ interrupt line. The over/under-battery voltage condition results in all outputs being turned off and the disabling of fault reporting for shorted and open-load conditions. With the 4-channel device, fault isolation is identical to that of the 6-channel device with the exception of over- and under-battery voltage fault bits being removed from the serial fault data. An additional feature on the 4-channel devices is an active low reset line ($\overline{RESET}$). The $\overline{RESET}$ line clears the fault register, the control register, and the

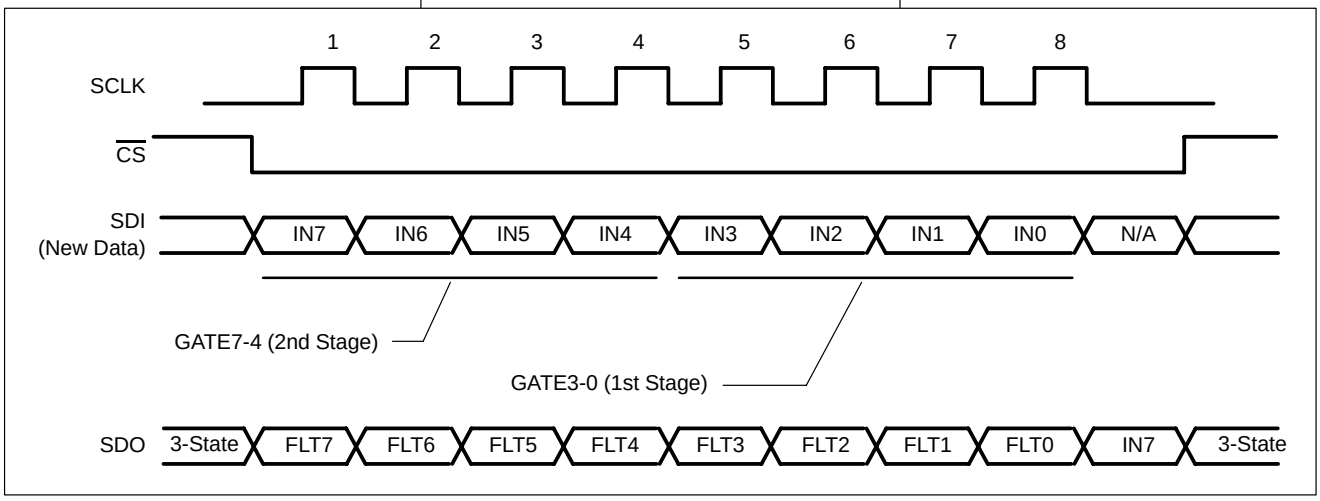


Figure 9. 8-Bit Serial Word Operation

fault interrupt line when transitioned low. This provides the means to disable the outputs and clear the device by toggling a single input.

Conclusions

The 6-channel (TPIC46L01/02 and TPIC2601) or 4-channel (TPIC44L01/02 and TPIC2401) chipset offer an enhanced approach to switching medium-load current applications. This dual-chip solution provides greater flexibility for the designer to select a power stage that better matches load requirements than may be available when using an integrated device. The TPIC46L01/02 or TPIC44L01/02 offers a parallel input interface to perform real-time control of the external power output stage in addition to providing fault detection and protection to prolong transistor life and increase system reliability.

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