TEXAS INSTRUMENTS

# *FlatLink*™ *Data Transmission System*

## *Design Overview*

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# *FlatLink™ Data Transmission System Design Overview*

***Kevin Gingerich, Technical Staff, Texas Instruments Inc.***

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## INTRODUCTION

FlatLink™ is a data transmission system that can provide better than a 2:1 reduction in the number of signal lines used for synchronous parallel data bus structures with no loss in data throughput. To do this, FlatLink takes single-ended data at clock rates of up to 68 MHz and increases the data signaling rate seven times up to 476 Mbps. The following report provides some design guidelines for successful implementation of a basic FlatLink system with no justification provided. For a more in-depth discussion, see the FlatLink Designer's Guide.

## SYSTEM DEFINITION

### General Description

This example of the FlatLink data transmission system is a single SN75LVDS81 transmitter and SN75LVDS82 receiver over 0.2 m of cable between the video display processor (VDP) and flat panel display (FPD) controller. The display offers a 1024 × 768 pixel resolution and 256 colors (8 bit/pixel). The graphical system clock is a nominal 65 MHz. The cable consists of five twisted-pair signal cables, a power wire, and a ground wire. There are board-mounted connectors on the VDP and FPD printed circuit boards (PCBs).

**NOTE:**

For more detailed information about the SN75LVDS81 FlatLink transmitter and the SN75LVDS82 FlatLink Receiver, see their respective data sheets (literature numbers SLLS258 and SLLS259).

### System Diagram

Figure 1 shows a basic FlatLink system with one transmitter connected to one receiver.

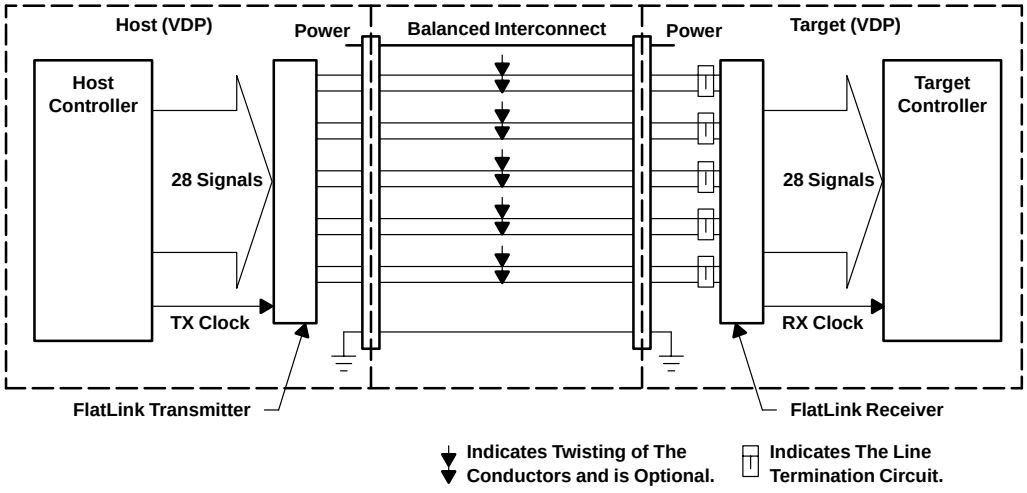


**Figure 1. Typical Connection of One FlatLink Transmitter and One Receiver.**

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### Interface Definition

The data inputs to the transmitter are from the VDP and consist of up to 24 bits of video information, a horizontal synchronization bit, a vertical synchronization bit, an enable bit, and a spare bit for a total of 28 data signals. All data is to be valid upon the falling edge of the clock signal to the SN75LVDS81. The bit mapping is listed in Table 1.

**Table 1. Bit Mapping and Terminal Assignments for 24-Bit Color Display**

| SIGNAL | | SN75LVDS81/82 INPUT/OUTPUT SIGNAL | SN75LVDS81 TERMINAL NUMBER | SN75LVDS82 TERMINAL NUMBER |
|---|---|---|---|---|
| Red0 | MSB | D0 | 51 | 27 |
| Red1 | | D1 | 52 | 29 |
| Red2 | | D2 | 54 | 30 |
| Red3 | | D3 | 55 | 32 |
| Red4 | | D4 | 56 | 33 |
| Red5 | | D6 | 3 | 35 |
| Red6 | | D27 | 50 | 7 |
| Red7 | LSB | D5 | 2 | 34 |
| Green0 | MSB | D7 | 4 | 37 |
| Green1 | | D8 | 6 | 38 |
| Green2 | | D9 | 7 | 39 |
| Green3 | | D12 | 11 | 43 |
| Green4 | | D13 | 12 | 45 |
| Green5 | | D14 | 14 | 46 |
| Green6 | | D10 | 8 | 41 |
| Green7 | LSB | D11 | 10 | 42 |
| Blue0 | MSB | D15 | 15 | 47 |
| Blue1 | | D18 | 19 | 51 |
| Blue2 | | D19 | 20 | 53 |
| Blue3 | | D20 | 22 | 54 |
| Blue4 | | D21 | 23 | 55 |
| Blue5 | | D22 | 24 | 1 |
| Blue6 | | D16 | 16 | 49 |
| Blue7 | LSB | D17 | 18 | 50 |
| H_SYNC | | D24 | 27 | 3 |
| V_SYNC | | D25 | 28 | 5 |
| ENABLE | | D26 | 30 | 6 |
| Reserved | | D23 | 25 | 2 |
| CLOCK | | CLKIN/CLKOUT | 31 | 26 |

The output of the receiver goes to the controller in the FPD with the same bit mapping as input to the transmitter. The receiver presents valid data on the falling edge of the output clock.

Both the transmitter and receiver must be supplied with a reasonably clean 3.3-V (nominal) supply voltage and a connection to a ground plane.

## ELECTRICAL CHARACTERISTICS

### Transmitter

#### *Inputs*

- Unused inputs to the transmitter should be left open circuited. All inputs are internally pulled down to ground with approximately a 300-kΩ resistance.
- If not actively driven, the $\overline{\text{SHTDN}}$ terminal should be pulled up to $V_{CC}$ by no more than a 10-kΩ resistor.
- The board trace between the VDP and the transmitter should be less than 9 cm in length and all lengths matched to within 1 cm of each other.
- The output buffer of the VDP should be rated at an output current of 4 mA minimum.

#### *Supply Voltage*

- Place a 0.01 µF Z5U ceramic, mica, or polystyrene dielectric 0805-size chip capacitor between each of the $V_{CC}$, $PLLV_{CC}$, and $LVDSV_{CC}$ terminals of the transmitter and the ground plane. The capacitors should be located as close as possible to the device terminals.
- A ground plane is highly recommended, if not mandatory. A power plane is recommended, but if not used, sharing of supply traces with other components should be held to a minimum.

#### *Outputs*

- If the PCB trace is more than 2 cm in length between the transmitter output terminals and the connector, the PCB must be constructed to maintain a controlled differential impedance near 100 Ω (see Figure 2).
- The physical length of each trace between the transmitter outputs and the connector should be matched to within 5 mm of each other. This usually requires mitering of the traces as shown in Figure 3.

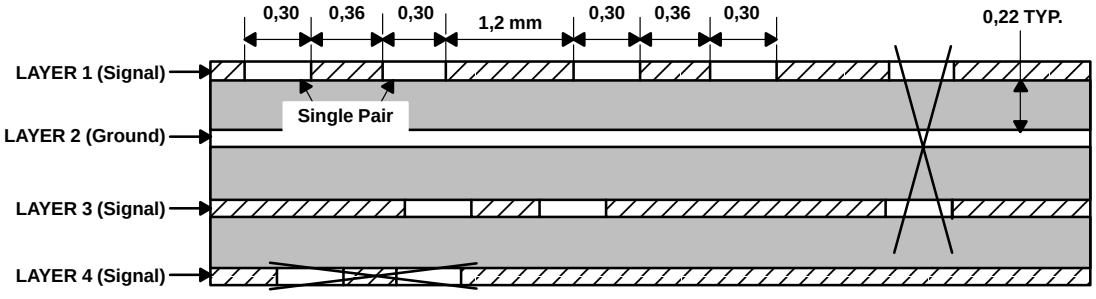


**Figure 2. Typical PCB Construction**

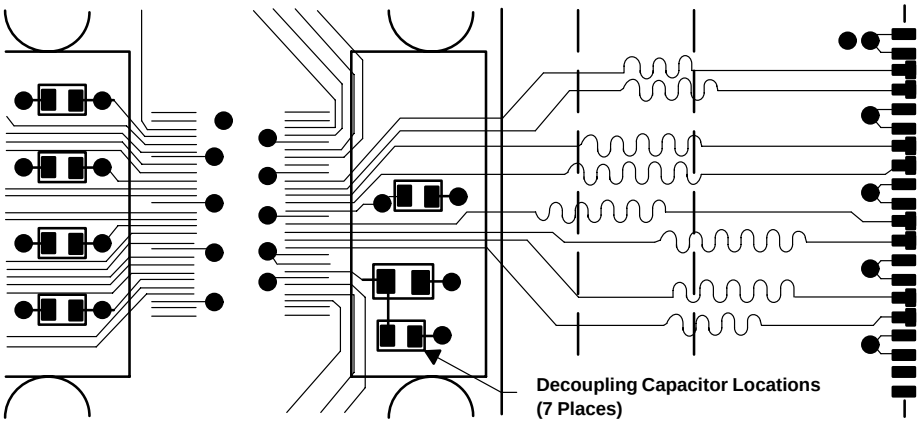


**Figure 3. Transmitter Layout Example**

## Receiver

### *Inputs*

- If there is more than 2 cm distance between the connector and the receiver input pins, the PCB must be constructed to maintain a controlled differential impedance near 100 Ω.
- The physical length of each trace between the connector and the receiver inputs should be matched to within 5 mm of each other. This may require mitering of the traces.
- A common misconception is that the receiver requires a termination resistor. This is not true. Termination is part of the interconnection and may or may not be located at the inputs to the receiver. See the Termination section of this document for more details.
- The $\overline{\text{SHTDN}}$ terminal is internally pulled down to ground such that the device is disabled if this pin is left open circuited.
- If not actively driven, the $\overline{\text{SHTDN}}$ terminal should be pulled up to $V_{CC}$ by no more than a 10-kΩ resistor.

### *Supply Voltage*

- Place a 0.01 μF Z5U ceramic, mica, or polystyrene dielectric 0805- or 0603-size chip capacitor between each of the $V_{CC}$, $PLLV_{CC}$, and $LVDSV_{CC}$ terminals of the receiver and the ground plane. The capacitors should be located as close as possible to the device terminals.
- A ground plane is highly recommended, if not mandatory. A power plane is recommended, but if not used, sharing of supply traces with other components should be held to a minimum.
- It is recommended that the supply voltage (particularly the $PLLV_{CC}$) be filtered through a surface mount (0805) ferrite followed by a 0.01 μF capacitance to ground between the ferrite and the receiver.

### *Outputs*

- The total length of board traces between the receiver outputs and the receiving controller should be less than 9 cm.
- The input capacitance to the controller should be less than 5 pF.

## Interconnection

### *Characteristic Impedance*

- At any cut point in the interconnect, the differential characteristic impedance should be 90 Ω to 130 Ω.
- Use polyethylene, polypropylene, or Teflon™ insulation in either round or flat cables and uniform distance between the conductors in a signal pair.
- Twisting of the signal pairs is recommended but not mandatory.
- Beldon #9807 is an example round cable.
- Beldon #9V28010 is an example flat cable.

### *Termination*

- Termination at the far end of the interconnect from the transmitter is mandatory.
- The system diagram in Figure 1 shows locations of the terminations.
- The termination schematic diagram is shown in Figure 4.

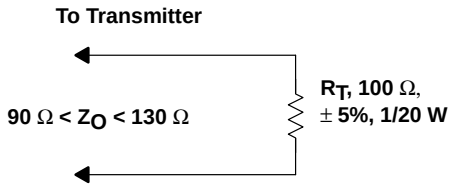


**Figure 4. Differential Termination**

- Use thick film leadless (0603 or 0805) chip resistors.

### *Balance*

- The distance and insulation between the signal and return conductors in a pair should be uniform.
- Any parasitic loading (capacitance) must be applied in equal amounts to each line.

### *Stubs*

- A stub is any conductive path(s) connected to the cable conductors or PCB traces between the transmitter and receiver.
- A stub should be as short as possible but no longer than 2 cm to 3 cm.
- The interconnect ends at the termination. If the receiver cannot be located within 2 cm of the termination, use the fly-by termination shown in Figure 5.

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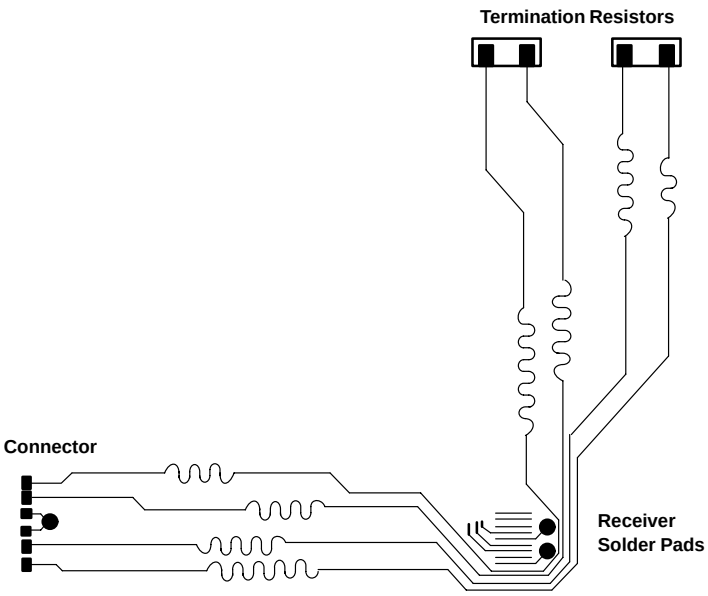


**Figure 5. Fly-By Termination at the Receiver**

***Skew and ISI***

- Keep the overall length of the interconnect between the transmitter and receiver less than 0.5 m.
- Keep the physical length of the signal pairs in the cable and PCB traces as close to the same as possible.
- The skew between signal pairs in good quality manufactured cables can range from 40 ps/m to 120 ps/m and should be specified by the vendor. A lower number is better.

## TIMING REQUIREMENTS

Assuming the prior guidelines have been followed:

- The VDP should provide a minimum set up time of 4 ns and a minimum hold time of 2.5 ns relative to the falling edge of the clock.
- The nominal period (between falling edges) of the clock signal should be greater than 14.5 ns.
- In general, the period of the input clock signal should not change by more than 2 ns from nominal. (See the FlatLink Designer's Guide on how to measure this and jitter in general.)
- The FPD controller should require no more than 4 ns of set up time and 4 ns of hold time relative to the falling edge of the clock.

## ELECTROMAGNETIC COMPATIBILITY

**Electrostatic Discharge**

- It is advisable that exposed connectors have pins recessed from the shell to prevent casual contact and discharges.

- It is also a good idea to have the ground pins longer than the signal pins in order to make the ground connection first and equalize the ground potentials before signal connections.

**Radiated Emissions and Susceptibility**

- There should be only one path for return current between the VDP and the FPD PCBs.
- Unused pins in connectors as well as unused wires in cables should be single-point grounded at the connector. Unused wires should be grounded at alternate ends.
- If an overall shield used, use a short pig-tail crimped to the shield end at each connector and then brought through a separate connector pin to a ground located as close to the connector as possible.
- If individual shielding of the signal pairs is used, use the same terminating technique as for the overall shield.

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