Configuring the TI 400 Mbit PHY as a 1394 Repeater Node

APPLICATION BRIEF: SLLA016A

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Abstract

This document specifies how the TSB41LV03 can be electronically configured to function as an IEEE 1394 bus repeater with minimal external circuitry. As a repeater it can be used to extend an IEEE 1394 network by being an active repeater connected by cable connections to other nodes in the network. It can also be used to multiply the number of ports available in a single module such as a device bay machine. The TSB41LV03 as a repeater maintains an IEEE1394 bus even after its IEEE 1394 link layer has been powered down. This document assumes that the reader is familiar with the hardware and nomenclature of IEEE 1394 and has access to the TSB41LV03 data sheet, which can be obtained through the Internet at http://www.ti.com/sc/1394.

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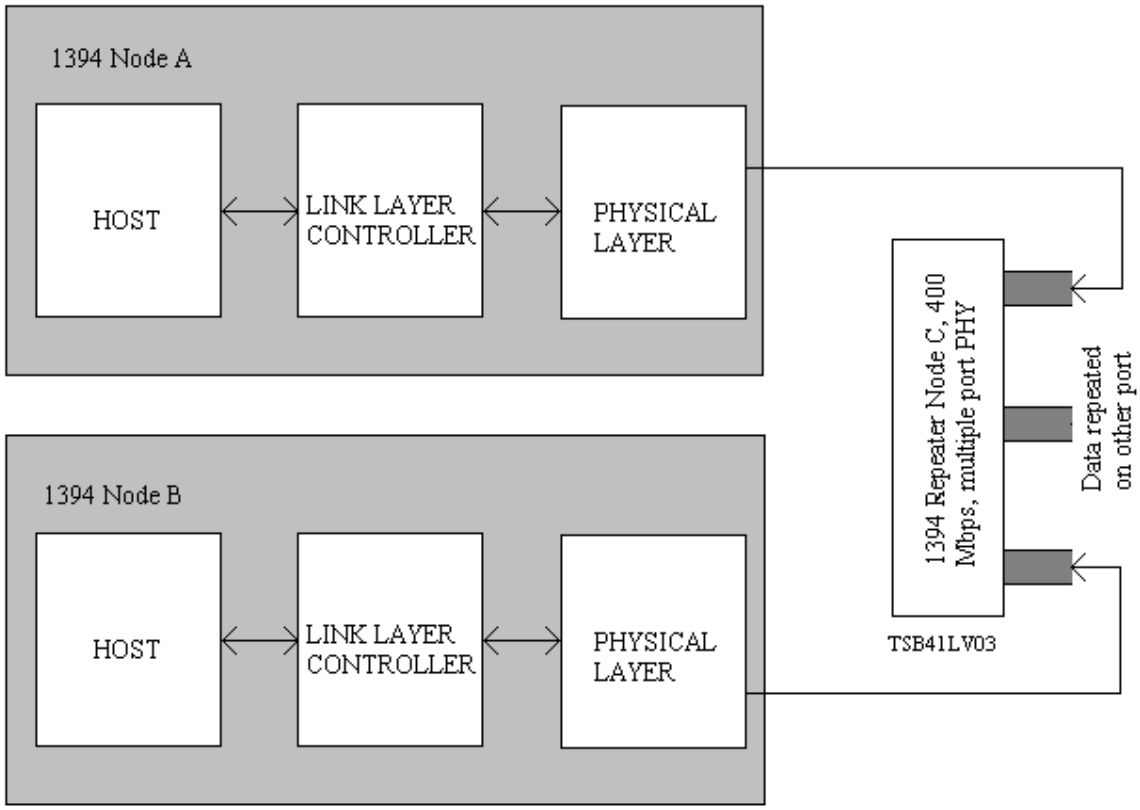
Introduction

The TSB41LV03 provides the digital and analog physical layer functions needed to implement a multiple port node in a cable-based IEEE 1394-1995 network. Each cable port incorporates two differential line transceivers whose functions include determining connection status, initialization and arbitration, packet reception and packet transmission. The TSB41LV03 normally interfaces with a Link Layer Controller (LLC), such as the OHCILynx, TSB12LV21A, TSB12LV31,TSB12LV01, etc. In the cable environment the Physical Layer can communicate with other Physical Layer Devices and perform as a repeater, as shown in Figure 1.

Figure 1. Physical Layer Performing as a Repeater



In Figure 1 Nodes “A” and “B” are fully capable IEEE1394 nodes with a Link layer, Physical layer and other electronics. Node C is a repeater node with only a 1394 physical layer & supporting circuitry. It does not have a link layer.

The cable environment is a network of nodes inter-connected by point-to-point cables called physical connections. The physical connection consists of a port on each node's PHY and a cable between them. A PHY can have multiple ports, which allows a branching multi-hop interconnect as shown in Figure 2. The primary restriction is that nodes must be connected together as an acyclic graph (no closed loops).

The cable PHY translates the physical point-to-point topology into a virtual broadcast bus expected by higher layers. The cable PHY does this by taking all data received on one port, synchronizing it to its local clock, and repeating out the received data on all of its other active ports. Additional peripherals or user end products can be attached to any available open ports and will be able to communicate via the repeater PHY. In such cases the PHY functions as a hub terminal where one can plug in other devices. Whenever a multi-port node is not the source of a packet it performs the function of repeater. Therefore all multiple port nodes present on a serial bus in the cable environment will function as repeater nodes. This is the minimum capability required and consists of an active physical layer. The PHY may be powered from the bus (via the power/ground pair in the serial bus cable) or from some other source. Repeater nodes shall:

- have an active physical layer
- function as an accurate signal repeater to propagate the signal state from the PHY port conditioned for reception to all other ports conditioned for transmission
- participate in the cable initialization and normal arbitration phases
- be capable of functioning as the root of a Serial Bus, and
- reconfigure their operational characteristics in response to PHY configuration packets

The remainder of this application note will describe how the TSB41LV03 may be configured to operate as a repeater.

Figure 2. Branching Multi-hop Interconnect

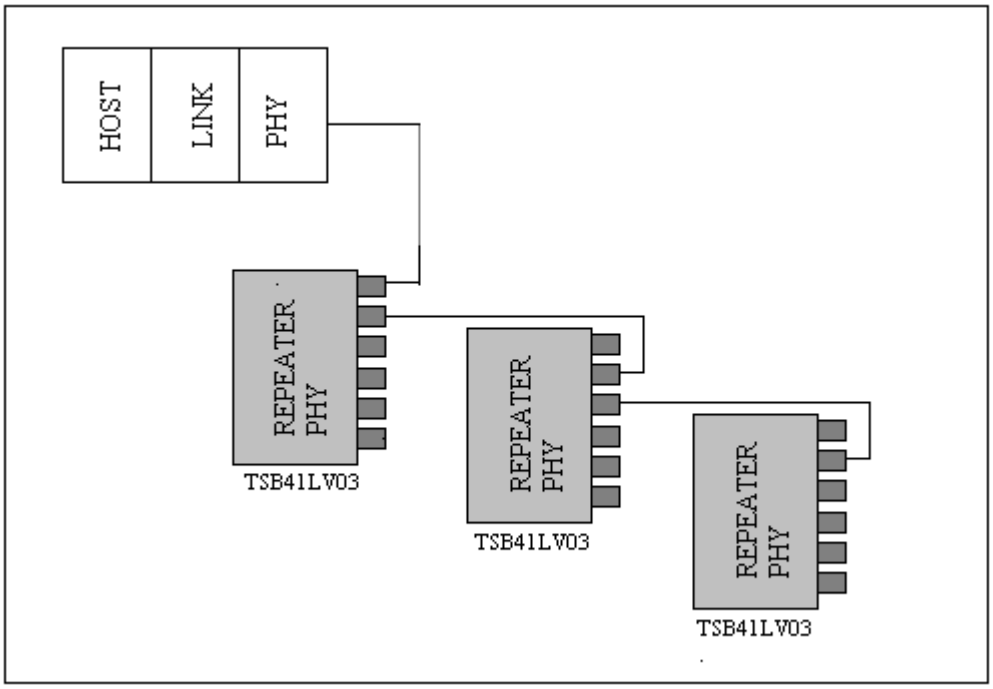
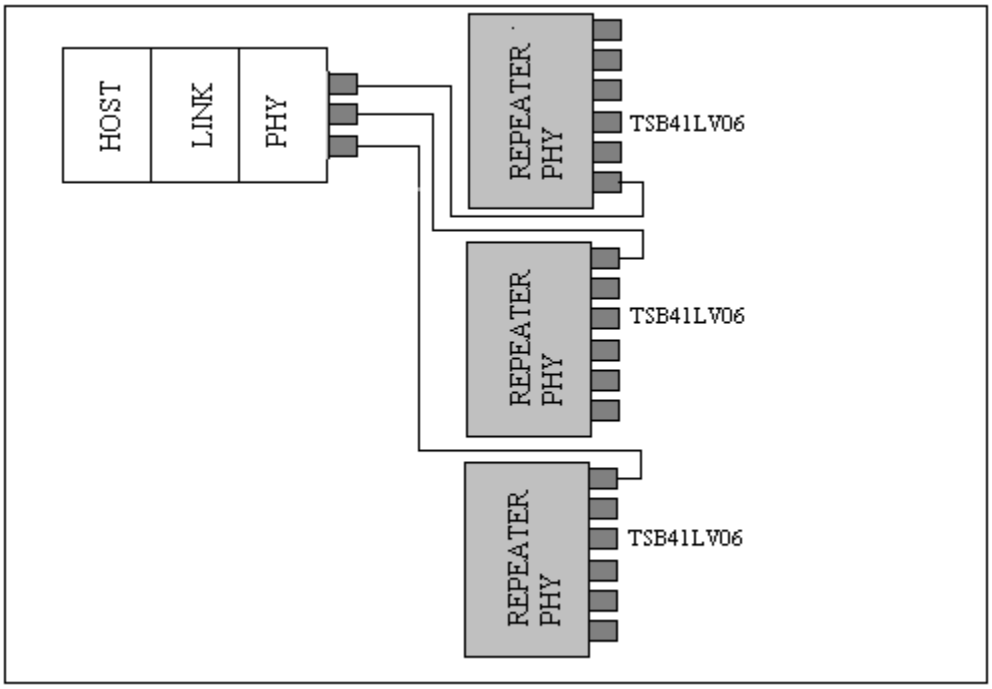


Figure 3. Port Multiplier Interconnect



Hooking up a TSB41LV03 as Repeater

The goal of a repeater node is simply to repeat packets further down the bus. It may not be a contender for Isochronous Resource Manager (IRM) or Bus Manager (BM). It should use the minimal amount of power and require a minimal amount of support circuitry. Specifically it does not require a link layer and microcontroller. The table below describes the connections required for a physical layer to be configured as a repeater only. Any terminal not included in this table is connected normally. Where the connections are the same as a normally connected PHY, the reader is referred to the data sheet terminal functions.

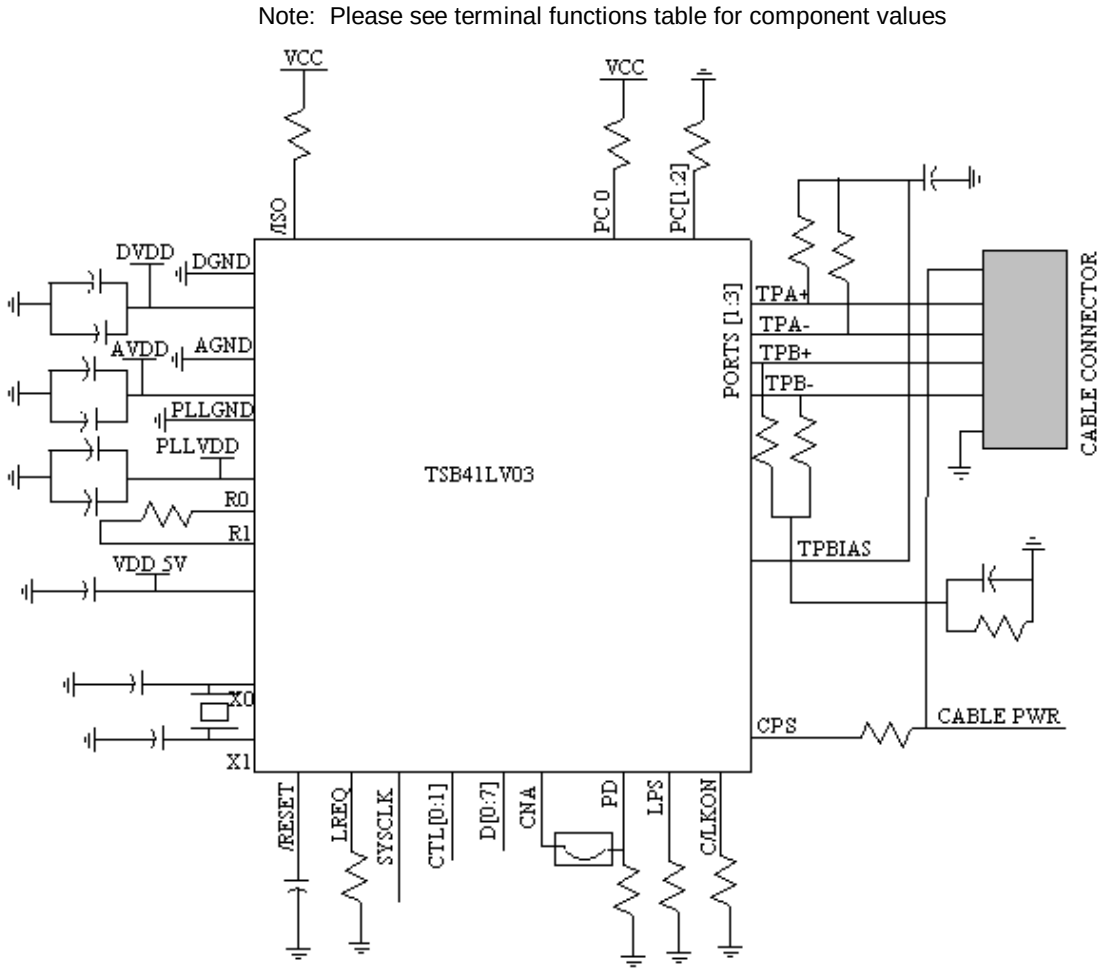
Table 1. Configuring a Physical Layer as a Repeater Only

Name	Pin Type	I/O	Description
DGND	Supply	-	Normal Connection.
AGND	Supply	-	Normal Connection.
PLLGND	Supply	-	Normal Connection.
DVDD	Supply	-	Normal Connection.
AVDD	Supply	-	Normal Connection.
PLLVDD	Supply	-	Normal Connection.
VDD-5V	Supply	-	Normal Connection.
R[0:1]	Bias	-	Normal Connection.
X0,X1	Crystal	-	Normal Connection.
/RESET	CMOS	I	Normal Connection.
LREQ	CMOS 5V tol	I	LLC Request input. This pin should be tied to ground through a 1KΩ resistor. The PHY does not require data from the link when it is a repeater. For prototypes, the PHY-Link Interface pins should be brought out to test points which should be arranged with sufficient grounds such that by changing the state of LPS a link may be attached to read the PHY registers. If the state of the LPS pin will always be low, this pin may be left unconnected.
SYSCLK	CMOS	O	System clock output. For prototypes, the PHY-Link Interface pins should be brought out to test points. These test points should be arranged with sufficient grounds such that by changing the state of LPS a link may be attached to read the PHY registers. After testing is complete, this pin may be left unconnected.
CTL[0:1]	CMOS 5 V tol	I/O	Control I/O's. For prototypes, the PHY-Link Interface pins should be brought out to test points. These test points should be arranged with sufficient grounds such that by changing the state of LPS a link may be attached to read the PHY registers. After testing is complete, these pins may be left unconnected.

Name	Pin Type	I/O	Description
D[0:7]	CMOS 5 V tol	I/O	Data I/O's. For prototypes, the PHY-Link Interface pins should be brought out to test points. These test points should be arranged with sufficient grounds such that by changing the state of LPS a link may be attached to read the PHY registers. After testing is complete, these pins may be left unconnected.
CNA	CMOS	O	Cable not active output. This pin may be left unconnected. If reduced power consumption is desired, this pin may be tied directly to the Power Down (PD pin 18) by a jumper. This will reduce power consumption when no cables are plugged into the repeater PHY.
PD	CMOS 5 V tol	I	Power down input. This pin should be pulled down using a 1KΩ resistor. If desired, this pin may be tied directly to CNA by a jumper. This will reduce power consumption when no cables are plugged into the repeater PHY.
LPS	CMOS 5 V tol	I	Link Power Status input. This pin should by default be pulled down with a 1 KΩ resistor. The user should provide a test point to enable the pin to be pulled high for testing.
C/LKON	CMOS	I/O	Bus Manager Contender input and Link-On output. This pin is tied low through a 10 KΩ resistor since with no link connected, the node can not act as IRM or BM.
PC[0:2]	CMOS	I	Power Class input bits. Used as inputs to set the default value of the 3-bit "pwr" field (bits 23:25) in the transmitted self_ID packet. They may be connected to a 10KΩ pull up or pull down or tied directly to PHY VCC or PHY GND. For a repeater mode that does not supply power, the power class is 4, (100 binary). See table 4-29 in IEEE Std. 1394-1995.
/ISO	CMOS	I	Normal Connection.
CPS	CMOS	I	Normal Connection.
TPA[1:3]+	Cable	O	Terminate the cable ports with the normal termination network.
TPA[1:3]-	Cable	O	Terminate the cable ports with the normal termination network.
TPB[1:3]+	Cable	O	Terminate the cable ports with the normal termination network.
TPB[1:3]-	Cable	O	Terminate the cable ports with the normal termination network.
TPBIAS[1:3]	Cable	O	Normal Connection.

Repeater Schematic Layout

Figure 4. TSB41LV03 Configured as a Repeater



If the TSB41LV03 is being used with one or more of the ports not being brought out to a connector, the twisted pair terminals must be terminated for reliable operation. For each unused port the TPB+ and the TPB- terminals must be pulled to ground. This may be done by tying them together and tying them directly to ground or by tying them to ground through the 5KΩ resistor of the normal termination network, thus disabling the port. The TPA+, TPA-, and TPBIAS terminals of an unused port may be left unconnected.

Power Management

In the cable environment the cable itself can supply modest amounts of power to connected nodes. Along with this benefit comes the requirement that the distribution of power be managed in some fashion. The bus manager may implement a power management scheme that performs this function. In the absence of a bus manager, the necessary power may originate from a power source associated with the node or it may be taken from the cable. If the node sources cable power to the bus, it must be done in compliance with the IEEE 1394 Trade Association Cable Power Distribution Specification.

TI 400 Mbps physical layers support the 1394a suspend/ resume functionality. Whenever an individual port of a node is not plugged into another port, it will be suspended, saving power. Plugging another node into the suspended port will resume the suspended port. The suspend/resume functionality may also be controlled by remote PHY packets across the 1394 bus. Please see P1394a version 2.0 or later for more information on suspend/resume and remote PHY packets.