Understanding the TSB12LV4x Bulky Data Interface

APPLICATION REPORT: SLLA017A

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Understanding the TSB12LV4x Bulky Data Interface

Abstract

This document describes the operation and features of the Bulky Data Interface (BDIF) of the TI TSB12LV4x 1394 Link Layer Controller device family. The Bulky Data Interface provides a data transfer interface for use with high speed peripherals. The interface can provide sustained data rates up to 160Mbit/s. In addition, the BDIF has access to an 8Kbyte FIFO which supports isochronous, asynchronous and MPEG2 /DV data transfers. This interface supports bidirectional transmit and receive of DSS/DVB/DV formatted data on 1394 as defined by the IEC61883 specification (depending on individual device capability). Asynchronous and non IEC61883 formatted isochronous data transmit and receive are also supported by this interface.

This document assumes the reader is familiar with the hardware and terminology of the IEEE 1394-1995 standard and the TI TSB12LV4x family of devices. Further information and data sheets can be obtained via the Internet at http://www.ti.com/sc/1394.

Product Support

Related Documentation

Further information and data sheets can be obtained via the Internet at http://www.ti.com/sc/1394.

The following documents are available via links from the TI 1394 external web page:

- Errata List for TSB12LV21, TSB12LV21A, TSB12C01A, TSB11C01, TSB11LV01, TSB21LV03, TSB21LV03A, and TSB14C01.
- Data sheets for all TI 1394 devices.
- Information on designer kits, including TSBKPCI, TSBKPCITST, TSKBGPLYNX, TSBKBACKPL, TSBKPRPHRL, TSBKMPEG2.

The IEEE 1394-1995 standard is available for purchase at http://standards.ieee.org/catalog/index.html

World Wide Web

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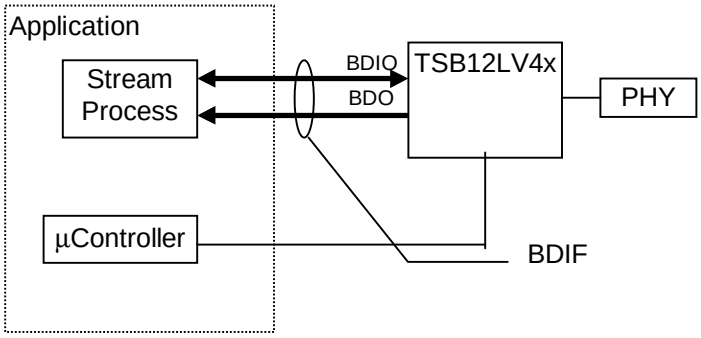
The URL specifically for the TI 1394 external web site is http://www.ti.com/sc/1394. On this page, one can subscribe to 1394TImes, which periodically updates subscribers on events, articles, products, and other news regarding 1394 developments.

Introduction

The Bulky Data Interface or BDIF is a pair of ports supported by the TSB12LV4x Link Layer controllers. The BDIF is the physical medium by which autonomous streams of different types are piped to an application that uses the TSB12LV4x. A system diagram is shown below:

Figure 1. Bulky Data Interface (BDIF) System Diagram



Since the BDIF has two ports, data can be full duplex. One port is bidirectional and the other is output only. Each port has its own independent clock, control signals, and modes of operation. The ports can operate in asynchronous clock domains.

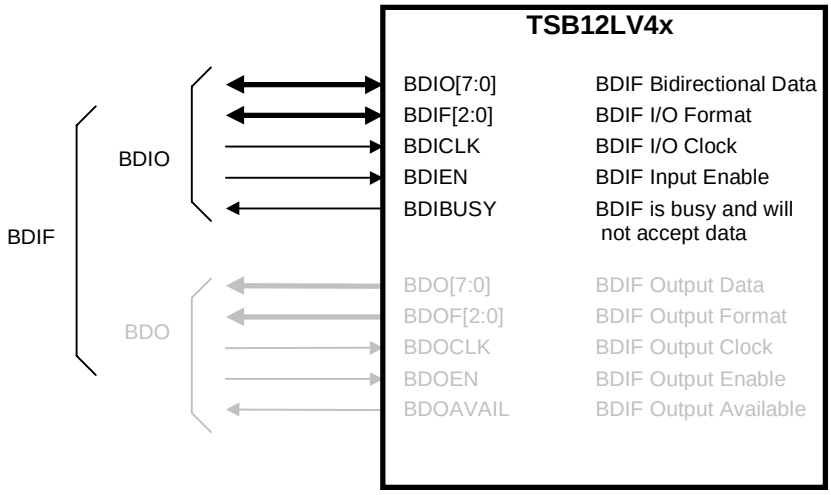
The BDIF handles three stream types:

1) Asynchronous
2) Isochronous
3) MPEG2(DVB)/DSS/DV (a special Isochronous type, capabilities depend on individual device)

A Format bus bound to each of the ports identifies these stream types. The encodings on the Format bus also frame packets within the stream. BDIF[2..0] is the Format bus for BDIO and BDOF[2..0] is the Format bus for BDO.

A more detailed look at the BDI's signaling is in order. Even though the two ports (BDIO and BDO) have some control signal and clock dependencies, we first look at them separately.

Figure 2. BDIO Port

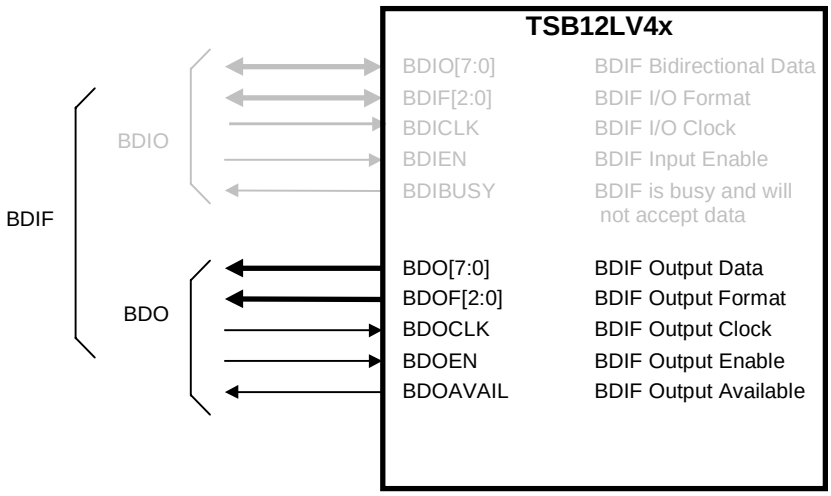


The signals of the bidirectional port (BDIO) have the following characteristics.

Table 1. Bidirectional Port (BDIO) Signal Characteristics

BDIO Signal Name	Driver Type	Description
BDIO[7:0]	I/O	Bidirectional BDI port (can be configured for input only). BDI[7] = MSB and BDI[0] = LSB.
BDIF[2:0]	I/O	Bidirectional BDIO Format (can be configured for input only). 000 Reserved 001 A byte of an MPEG2/DSS/DV cell 010 A byte of an unformatted Isochronous packet 011 A byte of an Asynchronous packet 100 Idle 101 First byte of an MPEG2/DSS/DV cell 110 Last byte of an unformatted Isochronous packet 111 Last byte of an Asynchronous packet
BDICLK	I	BDIO data input clock
BDIEN	I	BDI Enable: Qualifies BDIO port for writes. Read or write enable for BDIO port in bi-directional mode.
BDIBUSY	O	Signals busy condition on BDIO for writes. This signal goes high when the FIFO being written to is full. When BDIBUSY is high, writing to the full FIFO is disabled.

Figure 3. BDO Port



The signals of the unidirectional output only port (BDO) have the following characteristics.

Table 2. Unidirectional Output Only Port (BDO) Signal Characteristics

BDIO Signal Name	Driver Type	Description
BDO[7:0]	O	Unidirectional BDO port. BDO[7] = MSB and BDO[0] = LSB.
BDOF[2:0]	O	Unidirectional BDO Format. 000 Reserved 001 A byte of an MPEG2/DSS/DV cell 010 A byte of an unformatted Isochronous packet 011 A byte of an Asynchronous packet 100 Idle 101 First byte of an MPEG2/DSS/DV cell 110 Last byte of an unformatted Isochronous packet 111 Last byte of an Asynchronous packet
BDOCLK	I	BDIO or BDO data output clock
BDOEN	I	BDO Enable: Qualifies data on BDO for reads Read/Write* control for BDIO when it is bidirectional
BDOAVAIL	O	Signals data is available on BDO and/or BDIO for reads.

BDIF Control Register (Register D8h) Configuration: The BDIF is programmed by writes to the BDIF control register. This register is located at address D8h in the TSB12LV4x address space. The register format and bit definitions are shown below. The power-on default of this register is Bulky Data Mode A.

Figure 4. BDIF Control Register Configuration

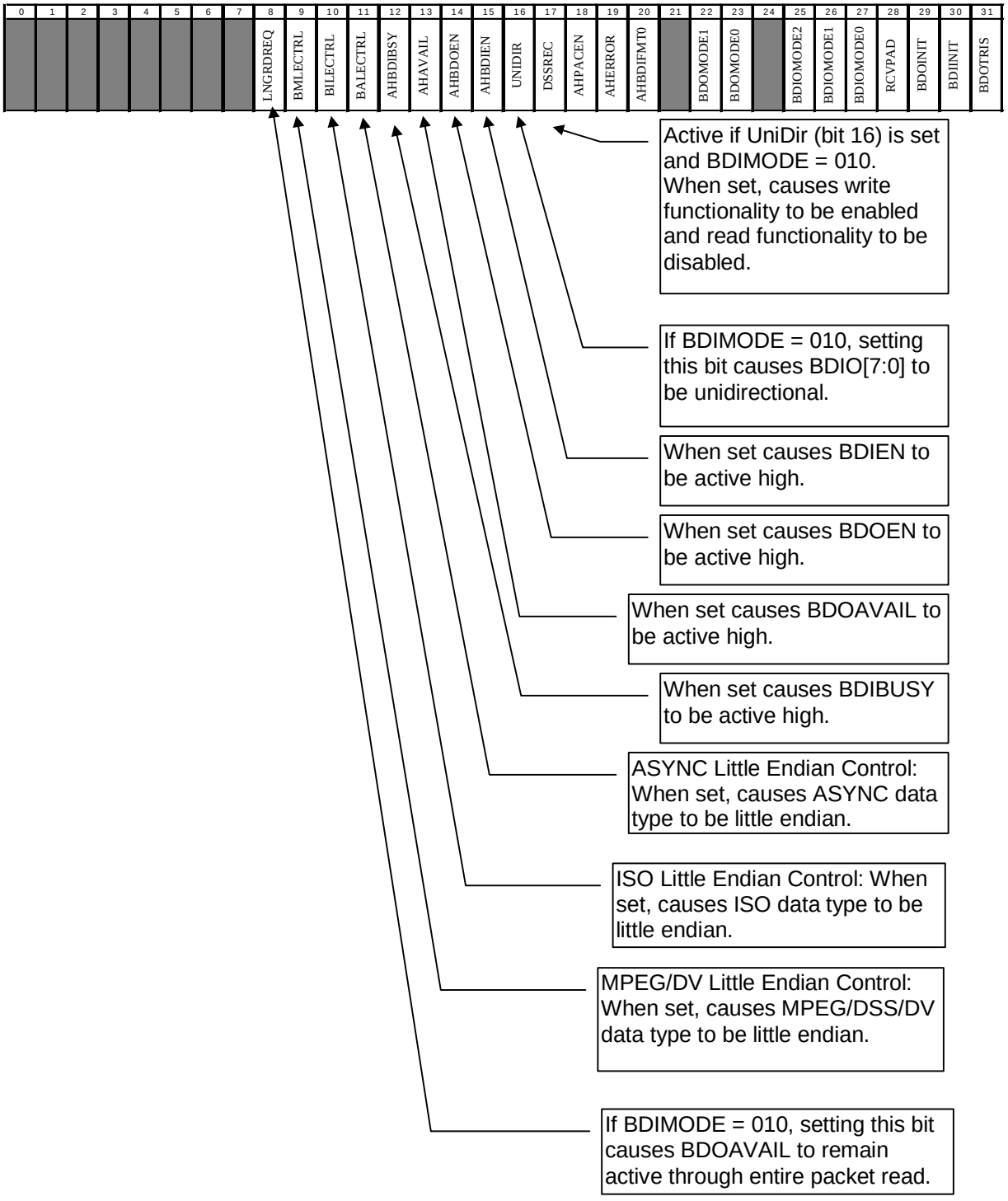
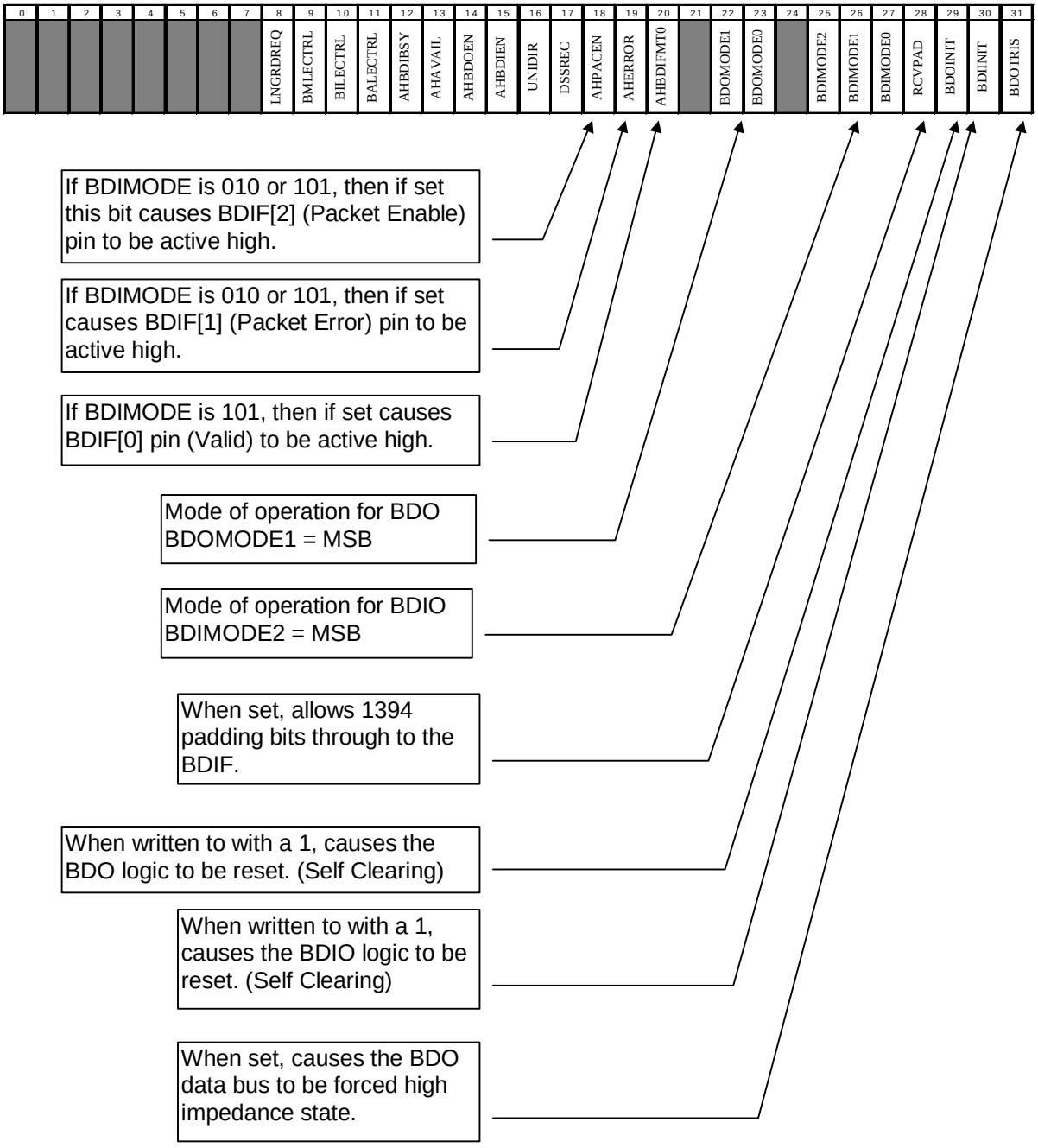


Figure 5. BDIF Control Register Configuration (cont'd)



Modes of the Bulky Data Interface (BDIF)

The BDIF has four valid modes of operation. These modes are selected using the BDIMODE and BDOMODE fields of the BDIF control register. The table below shows the basic features of each mode.

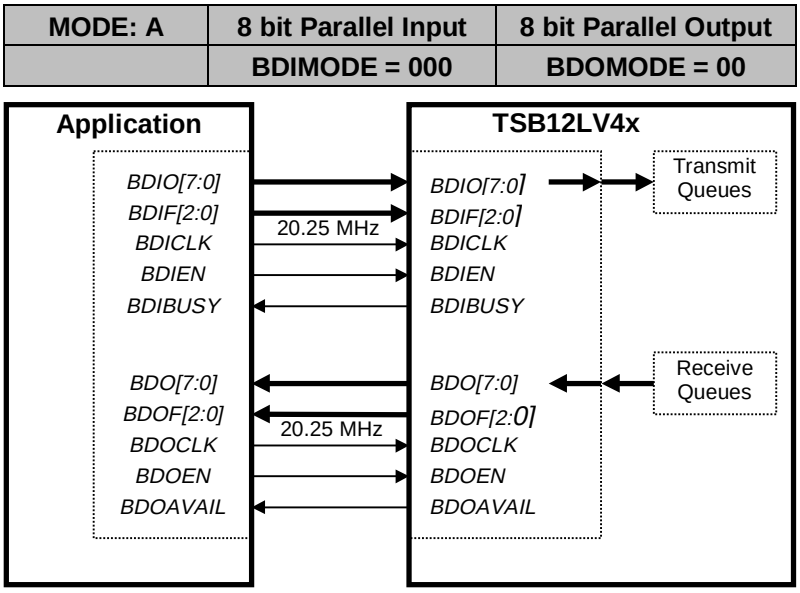
Table 3. Modes of the BDIF

MODE	A	B	C *	D
BDIMODE	000	000	101	001
BDOMODE	00	01	11	00
Data Input	BDIO	BDIO	BDIO Asynchronous	BDIO Bi-directional
Data Output	BDO	BDO	BDO Asynchronous	BDIO Bi-directional
Data Bus	2	2	2	1
Duplex	full	full	full	half
Data Input Clock MHz	20.25	20.25	NClk	20.25
Data Output Clock MHz	20.25	20.25	NClk	20.25
Data Throughput Mbyte/sec (max)	20 Write 20 Read	20 Write 20 Read	10 Write 10 Read	20.25
Control Signals Used:				
BDIEN	✔	✔	✔	✔
BDIBUSY	✔	✔		✔
BDOEN	✔		✔	✔
BDOAVAIL	✔	✔	✔	✔

* The asynchronous mode supports formatted isochronous data only (MPEG2(DVB)/DSS or DV).

Detailed descriptions of each mode are contained in the sections that follow.

Figure 6. Mode A Application Block Diagram



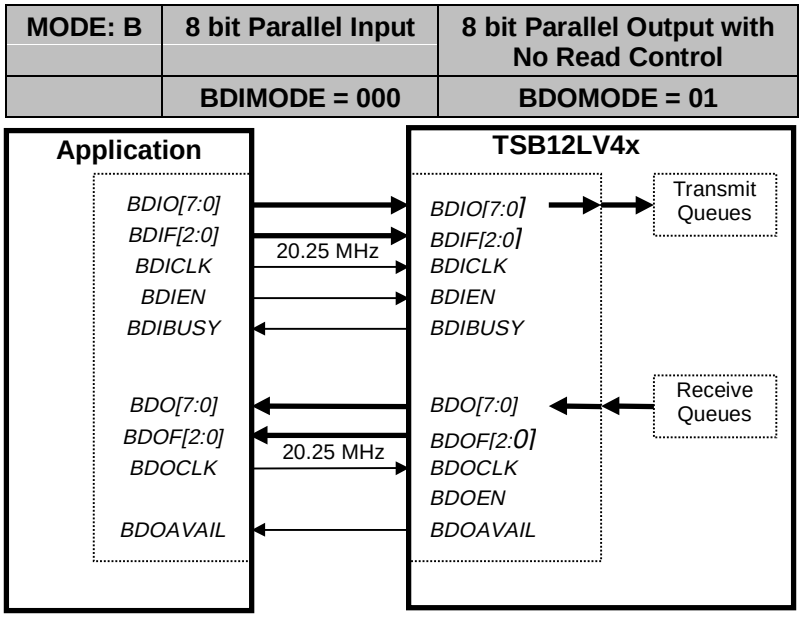
In this mode, the BDIO bus is input only. The BDO bus is output only. The BDIF operates in full duplex mode. It can receive data at the BDIO port and transmit data from the BDO port simultaneously.

Both the input and output buses operate synchronously to the BDICLK and BDOCLK. The maximum throughput of both the BDIO and BDO ports is 20Mbytes/sec. If the BDIF expects new data every clock cycle, then the data input clock (BDICLK) and data output (BDOCLK) clock run up to 20.25 MHz. The BDICLK/BDOCLK can be operated up to 40.5MHz if data is presented at the BDIF every other clock cycle.

BDIEN qualifies data on the BDIO port for writes. BDIBUSY signals a busy condition to the application on BDIO for writes. When BDIBUSY is activated, the TSB12LV4x will not accept any more data from the application.

BDOEN qualifies data on the BDO port for reads. BDOAVAIL signals the application that data is available on the BDO port for reads.

Figure 7. Mode B Application Block Diagram

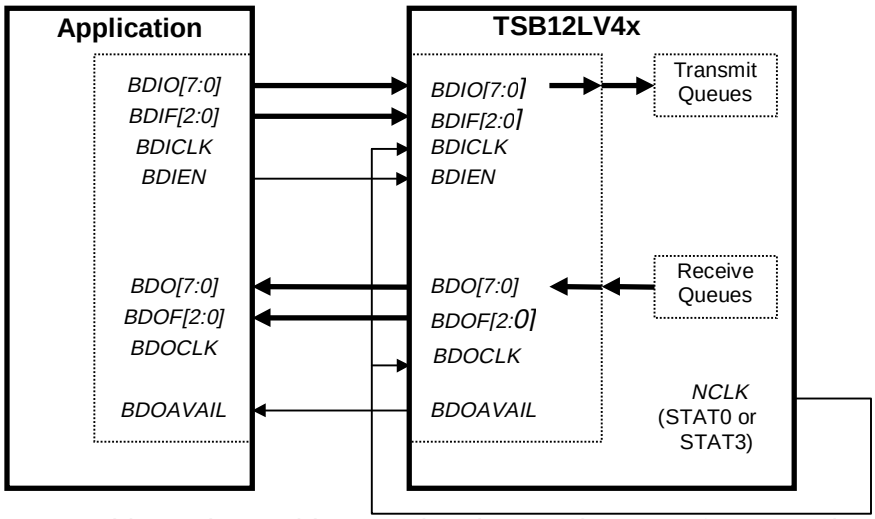


The data input and output for this mode are similar to Bulky Data MODE A. The BDIO port is input only. The BDO port is output only. The clock speeds, data rates, and full duplex capability are similar to MODE A.

The difference between this mode and MODE A is the absence of BDOEN, the Bulky Data output enable, for read operations. Since MODE B does not use BDOEN to read data out of the TSB12LV4x FIFOs, data is continuously output to the host whether or not it can accept it. The main advantage of this mode is that no signal is required by the host for receive. However, if the host FIFO can not handle the data output from TSB12LV4x, then data may be lost.

Figure 8. Mode C Application Block Diagram

MODE: C	8 bit Parallel Input (Asynchronous)	8 bit Parallel Output (Asynchronous)
	BDIMODE = 101	BDOMODE = 11



This mode provides two data buses: the BDIO for transmit and BDO for receive. The data at both the BDIO and BDO ports in this mode is resynchronized internally with the clock provided at the BDICLK/BDOCLK pins. This clock can be either NCLK (supplied by TSB12LV4x) or an external clock. This mode operates in full duplex.

NCLK may be used to sample both the BDIO and BDO ports. This clock rate is 24.576 MHz, or SYSCLK/2. NCLK is available at STAT0 or STAT3 and programmable at register 30h. For correct operation, NCLK must be physically attached to the BDICLK or BDOCLK pin. The BDICLK or BDOCLK may also be driven with an external clock. The maximum frequency of this external clock is 40MHz.

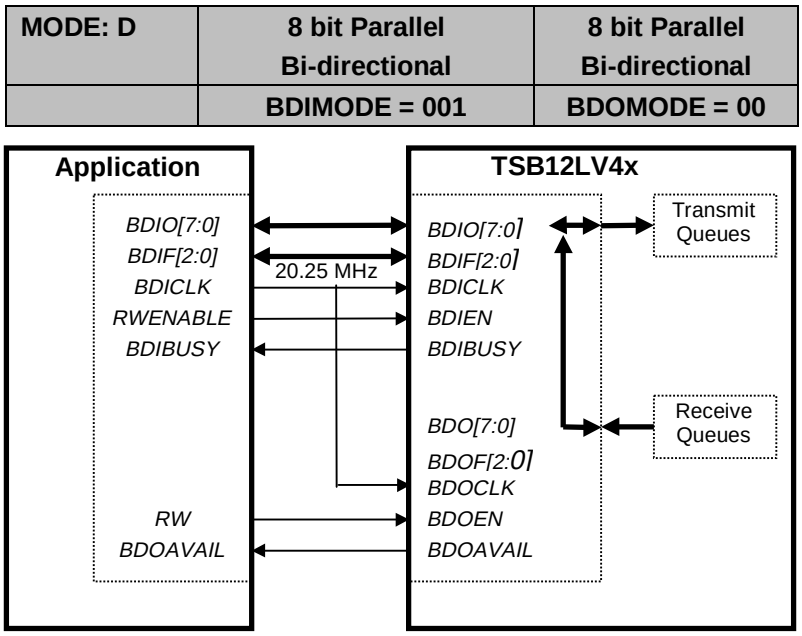
This mode has a maximum data throughput capability of 10Mbyte/s for a write and 10Mbyte/s for a read. Read and write operations can occur every fourth NCLK clock cycle. There must be at least one inactive BDIEN/BDOEN cycle between read or write operations. The host is responsible for meeting this timing requirement.

There is no BDIBUSY signal available in this mode. This means that during a write operation, there is no way for the TSB12LV4x to signal to the application that it is busy and can not accept any more data.

NOTE:

Only MPEG2(DVB), DSS, or DV data is supported in the asynchronous Bulky Data mode.

Figure 9. Mode D Application Block Diagram



This mode is the Bulky Data bi-directional mode. The device in this mode operates in half duplex. The read and write operations share the BDIO port.

In the bi-directional mode, BDIEN serves as the Read/Write enable on the BDIO port. BDOEN serves as Read/Write* on the BDIO port. The BDIF[2-0] serves as the format bus for both the read and write operations.

For bi-directional mode, BDICLK and BDOCLK must have the same frequency. The maximum data throughput for the bi-directional mode is 20.25Mbytes/sec. If the TSB12LV4x expects data on every clock cycle, then the maximum BDICLK/BDOCLK rate is 20.25MHz. If the TSB12LV4x expects data on every other clock cycle, then the maximum BDICLK/BDOCLK rate is 40.5MHz.

BDIBUSY signals the application when the TSB12LV4x BDIO port is busy and will not accept any more data during a write operation. BDOAVAIL signals the application when the TSB12LV4x BDIO port has data available for reading.