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SN75976A Channel Differential Transceiver Thermal Analysis

Application Report

September 1998 Advanced Analog Products

SLLA029

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ABSTRACT

The purpose of this paper is to analyze the power consumption and the junction temperatures of the SN75976A1DL, SN75976A2DL, SN75976A1DGG, or SN75976A2DGG 9-Channel Differential Transceivers in typical applications.

1 Power Dissipation

Power is dissipated within the silicon from three primary sources: the steady-state quiescent power, ac or switching power, and dc or resistive losses in the output drivers.

1.1 Steady-State Quiescent Power

The current necessary to bias the circuits of SN75976A with all nine channels enabled as differential drivers is typically 39.7 mA with a maximum test limit of 60 mA. When the device is enabled to nine differential receivers, I_{CC} becomes 25.2 mA typically with a maximum limit of 45 mA. These values are from statistical characterization of seven different wafer lots over a supply voltage range of 4.75 V to 5.25 V and a case temperature range of 0°C to 125°C.

Driver quiescent power:

$$P_{DCC} = I_{CC} \times V_{CC}$$

$$= 39.7 \text{ mA} \times 5.0 \text{ V} = 198.5 \text{ mW average}$$
$$< 60.0 \text{ mA} \times 5.3 \text{ V} = 318.0 \text{ mW maximum}$$

Receiver quiescent power:

$$P_{RCC} = I_{CC} \times V_{CC}$$

$$= 25.2 \text{ mA} \times 5.0 \text{ V} = 126.0 \text{ mW average}$$
$$< 45.0 \text{ mA} \times 5.3 \text{ V} = 238.5 \text{ mW maximum}$$

1.2 Switching Power

The average increase in the normal I_{CC} for an unloaded driver of the SN75976A was measured on four representative samples. The average increase was 4.88 mA/channel when switching at 10 MHz (20 MXfers/s), a 50% duty cycle, and a V_{CC} of 5 V. At a V_{CC} of 5.25, the single largest measured increase was 5.3 mA/channel.

One driver's switching loss at 10 MHz:

$$P_{DAC} = I_{CC} \times V_{CC}$$

$$= 4.9 \times 5.0$$
$$= 24.4 \text{ mW/channel typical}$$
$$< 27.8 \text{ mW/channel maximum}$$

A receiver, switching at the same frequency and duty cycle with unloaded outputs, consumed an additional 2.0 mA/channel above steady state on average. The maximum was 2.5 mA/channel on one sample at a V_{CC} of 5.25 V.

One receiver's switching loss at 10 MHz:

$$P_{RAC} = I_{CC} \times V_{CC}$$

$$= 2.0 \times 5.0$$
$$= 10.0 \text{ mW/channel typical}$$
$$< 13.1 \text{ mW/channel maximum}$$

1.3 D C Losses

The output stage losses vary with the magnitude of the output voltages, the output transistor saturation or drain-to-source voltages, and the load conditions. Table 1 is derived from the solution of the equivalent circuit of a differential SCSI bus. No further proof is included in this analysis.

The typical single-ended output voltages of the SN75976A driver have been characterized with a SCSI load test circuit with the following results:

Table 1. SN75976A Output Voltages with a SCSI Load

Parameter	Typ†	Max‡	Unit
VO, Positive SCSI line voltage when asserted	1.5 V	1.3 V	V
VO, Positive SCSI line voltage when negated	3	3.7	V
VO(-), Negative SCSI line voltage when asserted	1.6	1.5	V
VO(-), Negative SCSI line voltage when negated	3.3	3.9	V
VOD, differential output voltage when asserted	1.4	-2.2	V
VOD, differential output voltage when negated	-1.8	-2.6	V

† Typical is the statistical average of the measurements on 268 samples from seven wafer lots at a case temperature of 25°C and a V_{CC} of 5 V.

‡Worst case is the maximum differential output voltage measured on 268 samples from seven wafer lots at a case temperature of 125°C and a V_{CC} of 5.25 V.

Solution of the circuit with the SCSI test load and the voltages in Table 1 resulted in a typical power dissipation in the output transistors of 117 mW when asserted and 60 mW when negated. The worst case power is 167 mW asserted and 113 mW negated.

Driver output dc losses:

$P_{(DOH)}$ = 117.0 mW/channel typical
< 167.0 mW/channel maximum

$P_{(DOL)}$ = 60.0 mW/channel typical
< 113.0 mW/channel maximum

At an I_{OL} of 8 mA, the typical receiver V_{OL} is 0.6 V with a maximum test limit of 0.8 V. At -8 mA, the typical V_{OH} is 4.5 V with a minimum limit of 2.4 V.

Receiver output dc losses:

$P_{(ROH)}$ = IOH x (VCC - VOH)

= 8 mA x (5 V - 4.5 V)
= 4.0 mW/channel typical
< 8 mA x (5.3 V - 2.4 V)
< 23.2 mW/channel maximum

$P_{(ROL)}$ = IOL x VOL

= 8 mA x .6 V
= 4.8 mW/channel typical
< 8 mA x 0.8 V
< 6.4 mW/channel maximum

The components of the power dissipation in the SN75976A are summarized in Table 2.

Table 2. Components of Power Dissipation

Parameter		Typ	Max	Unit
$P_{(DCC)}$	Steady-state quiescent power for 9 drivers	198.5	315	mW
$P_{(DAC)}$	Switching power for 1 driver at 10 MHz	24.4	27.8	mW/ channel
$P_{(DOH)}$	Driver output power loss when asserted	117	167	mW/ channel
$P_{(DOL)}$	Driver output power loss when negated	60	113	mW/ channel
$P_{(RCC)}$	Steady-state quiescent power for 9 receivers	126	238.5	mW
$P_{(RAC)}$	Switching power for 1 receiver at 10 MHz	10	13.1	mW/ channel
$P_{(ROH)}$	Receiver output power loss when asserted	4	23.2	mW/ channel
$P_{(ROL)}$	Receiver output power loss when negated	4.8	6.4	mW/ channel

2 Device Power Dissipation

The operation of the device and its power component contributions must be evaluated to determine the total power that will be dissipated in the package. The steady-state quiescent power is a constant, but the switching power and output stage power will depend upon the data being transmitted or received and the duration of the transfer.

Three cases will be analyzed:

1) Nine channels continuously with one transmitting random data to a Fast-20 SCSI bus
2) Nine channels continuously receiving random data from a Fast-20 SCSI bus
3) The unlikely assertion of all nine bits continuously. (Continuously is defined here as at least three-device thermal time constants or approximately 15 seconds.)

Since the assumption in case 1) and 2) is random data, the probability that any one bit on the bus is asserted or being negated is equal. With equal probability and a long observation period relative to the data transfer period, the mean power in an output stage will be the average of the high-level and low-level values. Assumptions for the three cases for nine channels include:

1) $P_{(DO1)} = (P_{(DOH)} + P_{(DOL)})/2 \times 9$
2) $P_{(RO2)} = (P_{(ROH)} + P_{(ROL)})/2 \times 9$

The driver outputs are continuously asserting the bus so, $P_{(DO3)} = P_{(DOH)} \times 9$

The circuit switching losses, $P_{(DAC)}$ and $P_{(RAC)}$, were measured with the switching loss occurring on every cycle. Because the state of the output is random and undeterministic, the probability that the driver output changes state on the next cycle is equal. Again, over a long observation period, the mean switching power for each operating case is:

1) $P_{(DAC)}1 = P_{(DAC)}/2 \times 9$
2) $P_{(RAC)}2 = P_{(RAC)}/2 \times 9$
3) Where there is no switching power component, $P_{(DAC)}3 = 0$

The power dissipated in the package for the three cases is then:

1) $PD1 = P_{(DCC)} + (P_{(DOL)} + P_{(DOL)}2 \times 9 + P_{(DAC)}/2 \times 9$
2) $PD2 = P_{(RCC)} + (P_{(ROH)} + P_{(ROL)})/2 \times 9 + P_{(RAC)}/2 \times 9$
3) $PD3 = P_{(DCC)} + P_{(DOH)} \times 9$

Table 3. Device Power for Three Cases

Parameter	Typ	Max	Unit
PD1 Power dissipation when transmitting at 20 MXfers/s	1104.8	1700.2	mW
PD2 Power dissipation when receiving data at 20 MXfers/s	210.6	428.5	mW
PD3 Power dissipation when all drivers asserted	1251.5	1821.0	mW

3 Junction Temperature

Measurements of the SSOP-56 package and leadframe used on the SN75976ADL were performed on a 13.0 cm x 9.8 cm six-layer printed circuit board. The board was built with the ground and heat-sinking pins soldered to individual pads and connected to a second layer ground plane through 0.15 mm etch runs. There was one common via to the ground plane on each side of the package. The ground plane was 0.254 mm below the surface of the 1.6 mm thick board with 1 oz. copper layer. The results of tests on two samples were an average $R_{\Theta JA}$ of 49.7°C/W with 1 W of power dissipation and no airflow.

Measurements were performed on six TSSOP-56 packages and leadframes used on the SN75976ADGG. The test board was 13.7 cm x 8 cm x 1 mm thick with a ground and V_{CC} plane of 1 oz. copper. The ground and heat-sinking pins were soldered to individual pads and connected to the ground plane through 0.15 mm etch runs and one common via interconnect to the ground plane per side. The results of the test was an average $R_{\Theta JA}$ of 46.7°C/W at one Watt of power dissipation and no air flow.

Using a rounded 50°C/W for each package, the mean junction temperature rise above ambient can then be calculated. Table 4 shows the results for each case using the relationship TJ - TA = $R_{\Theta JA}$ x PD.

Table 4. Estimated Junction Temperature Rise Above the Ambient Still-Air Temperature

Parameter	Typical	Maximum	Units
T_{J1} Junction temperature rise when transmitting at 20 M xfer/s	55.2	85	°C
T_{J2} Junction temperature rise when receiving data at 20 M xfer/s	10.5	21.4	°C
T_{J3} Junction temperature rise with all drivers asserted continuously	62.6	90.9	°C

4 Conclusion

Most designs require two junction temperature restrictions:

1. Junction operating temperature should not exceed 150°C under worst case operating conditions

2. The mean operating junction temperature should be no more than 110°C

The junction temperature rise above the ambient still-air temperature is estimated in Table 4 for three operating conditions. The worst-case temperature rise is TJ3, applicable to requirement #1 above.

Solving for TA:

TA + TJ3 < 150°C
TA < 150°C - TJ3
TA < 150°C - 90.9 °C = 59.1°C

Evaluation of the mean operating junction temperature can vary a great deal based upon the assumptions of mean still-air temperature and transmit-to-receive duty cycles. In any case, the use of the typical values TJ1 and TJ2 are required. The following table calculates the projected mean junction temperature for various duty cycles and ambient air temperatures.

Table 5. Projected Mean Junction Temperatures vs. Duty Cycles and Ambient Air Temperature

		mean T_J °C		
Transmit	Receive	T_A = 25°C	T_A = 55°C	T_A = 70°C
100%	0%	80.2	110.2	125.2
67%	33%	65.4	95.4	110.4
50%	50%	57.9	87.9	102.9
33%	67%	50.3	80.3	95.3
0%	100%	35.5	65.5	80.5

Either SN75967A package meets the design requirements up to a maximum ambient still-air temperature of 60°C. This limit occurs, under a worst-case scenario of all nine drivers enabled, continuously assert the Differential SCSI test circuit. The test circuit represents a bus with attached 32 RS-485 loads.