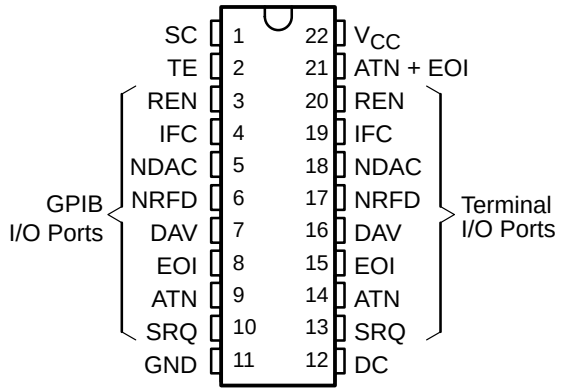
SLLS011A – OCTOBER 1985 – REVISED FEBRUARY 1993

- **8-Channel Bidirectional Transceiver**
- **Power-Up/Power-Down Protection (Glitch Free)**
- **ATN+EOI (OR Function) Output to Simplify Board Layout**
- **Designed to Implement Control Bus Interface for Multiple Controllers**
- **Low-Power Dissipation . . . 72 mW Max Per Channel**
- **Fast Propagation Times . . . 22 ns Max**
- **High-impedance PNP Inputs**
- **Receiver Hysteresis . . . 650 mV Typ**
- **Bus-Terminating Resistors Provided on Driver Outputs**
- **No Loading of Bus When Device Is Powered Down (V_{CC} = 0)**

N PACKAGE
(TOP VIEW)



NC – No internal connection

NOT RECOMMENDED FOR NEW DESIGN

description

The SN75164B eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a multiple-controller instrumentation system. When combined with the SN75160B octal bus transceiver, the SN75164B provides the complete 16-wire interface for the IEEE-488 bus.

CHANNEL IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC TE SC	Direction Control Talk Enable System Control	Control
ATN SRQ REN IFC EOI	Attention Service Request Remote Enable Interface Clear End or Identify	Bus Management
ATN + EOI	ATN Logical or EOI	Logic
DAV NDAC NRFD	Data Valid Not Data Accepted Not Ready for Data	Data Transfer

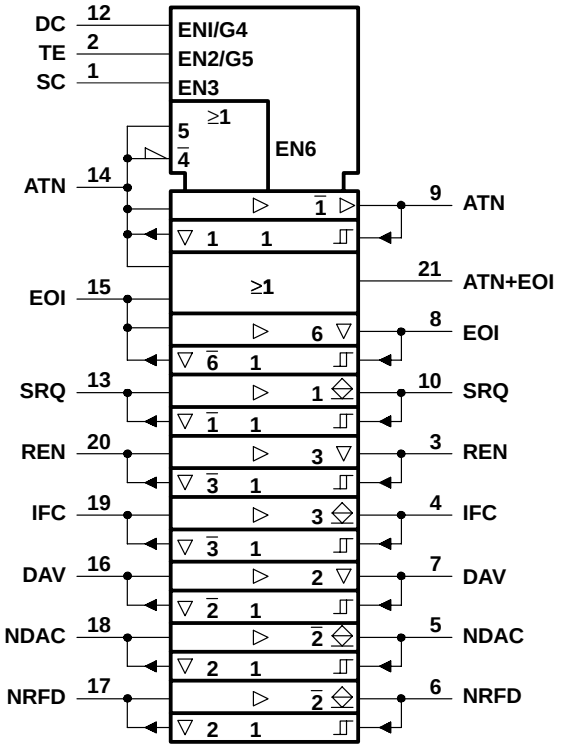
The SN75164B features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. All outputs are disabled (at a high-impedance state) during V_{CC} power-up and power-down transitions for glitch-free operation. The direction of data flow through these driver-receiver pairs is determined by the DC, TE, and SC enable signals. The SN75164B is identical to the SN75162B with the addition of an OR gate to help simplify board layouts in several popular applications. The ATN and EOI signals are ORed to pin 21, which is a standard totem-pole output.

description (continued)

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage V_{CC} is 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and an ensured hysteresis of 400 mV for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

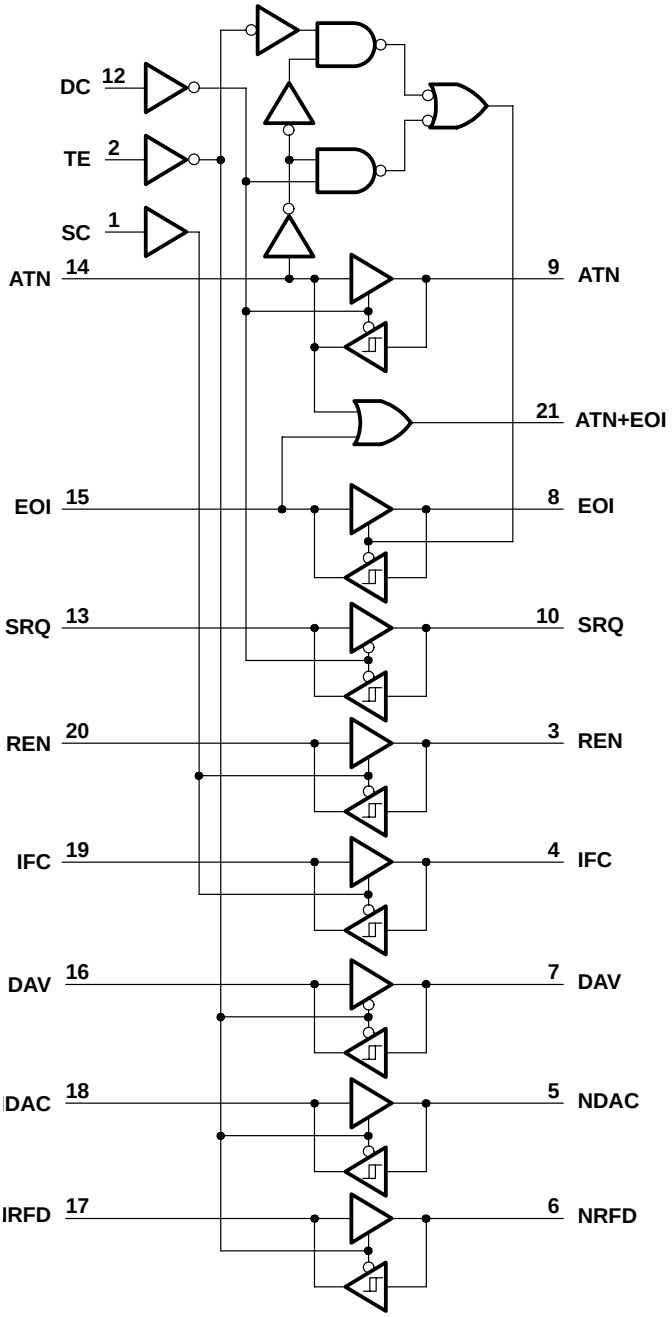
The SN75164B is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

logic diagram (positive logic)



RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS				BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN† (controlled by DC)	SRQ (controlled by DC)	REN (controlled by SC)	IFC (controlled by SC)	EOI	DAV (controlled by TE)	NDAC (controlled by TE)	NRFD (controlled by TE)
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

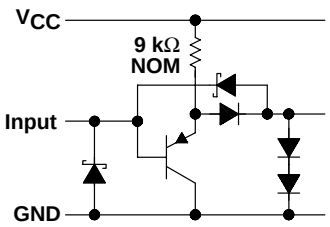
† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

ATN + EOI FUNCTION TABLE

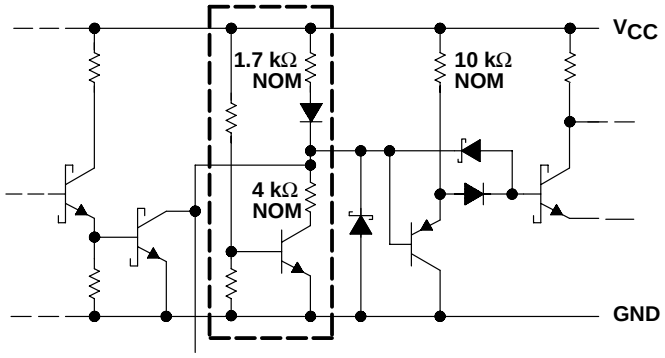
INPUTS		OUTPUT ATN+EOI
ATN	EOI	
H	X	H
X	H	H
L	L	L

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

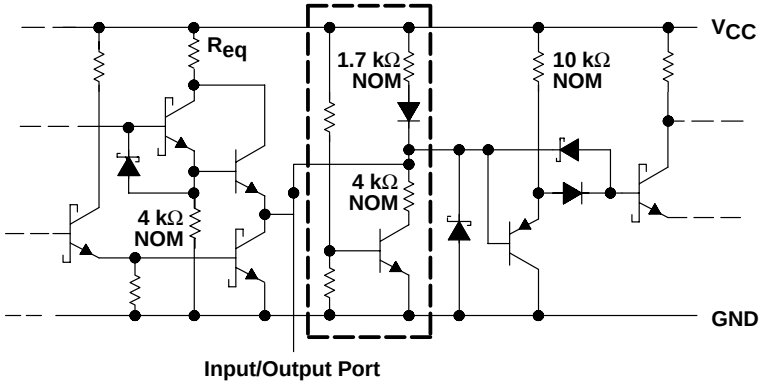


TYPICAL OF SRQ, NDAC, AND NRFD GPIB I/O PORT



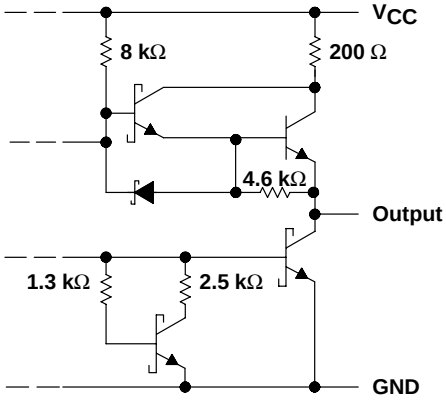
Circuit inside dashed lines is on GPIB I/O ports only.

TYPICAL OF ALL I/O PORTS
EXCEPT SRQ, NDAC, AND NRFD GPIB I/O PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on GPIB I/O ports only.

ATN+EOI OUTPUT



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1700 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the N package at the rate of 13.6 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level Input voltage, V_{IH}		2			V
Low-level Input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with 3-state outputs			–5.2	mA
	Terminal ports			–800	µA
	ATN+EOI			–400	
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
	ATN+EOI			4	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

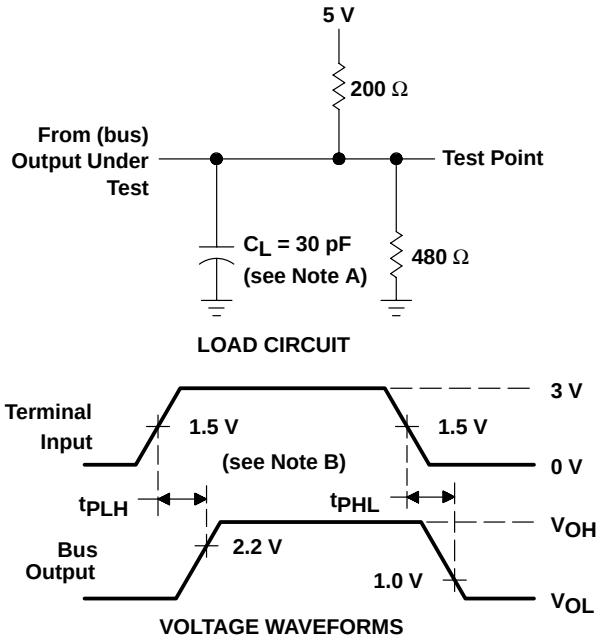
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA				–1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus	See Figure 8		0.4			V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = –800 µA		2.7			V
		Bus	I_{OH} = –5.2 mA		2.5			
		ATN+EOI	I_{OH} = –400 µA		2.7			
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA				0.5	V
		Bus	I_{OL} = 48 mA				0.5	
		ATN+EOI	I_{OL} = 4 mA				0.4	
I_I	Input current at maximum input voltage	Terminal§	V_I = 5.5 V				100	µA
		ATN+EOI	V_I = 5.5 V				200	
I_{IH}	High-level input current	Terminal, control	V_I = 2.7 V				20	µA
		ATN, EOI	V_I = 2.7 V				40	
I_{IL}	Low-level input current	Terminal, control	V_I = 0.5 V				–100	µA
		ATN, EOI	V_I = 0.5 V				–500	
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5		3.7	V
				$I_{I(bus)}$ = –12 mA			–1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = –1.5 V to 0.4 V	–1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		–3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5 –3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 V to 2.5 V			–40	µA
I_{OS}	Short-circuit output current	Terminal			–15		–75	mA
		Bus			–25		–125	
		ATN+EOI			–10		–100	
I_{CC}	Supply current		No load,	TE, DE, and SC low			120	mA
$C_{I/O(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0 V,	$V_{I/O}$ = 0 to 2 V, f = 1 MHz		30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{OH} applies for 3-state outputs only.
§ Except ATN and EOI terminal pins

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

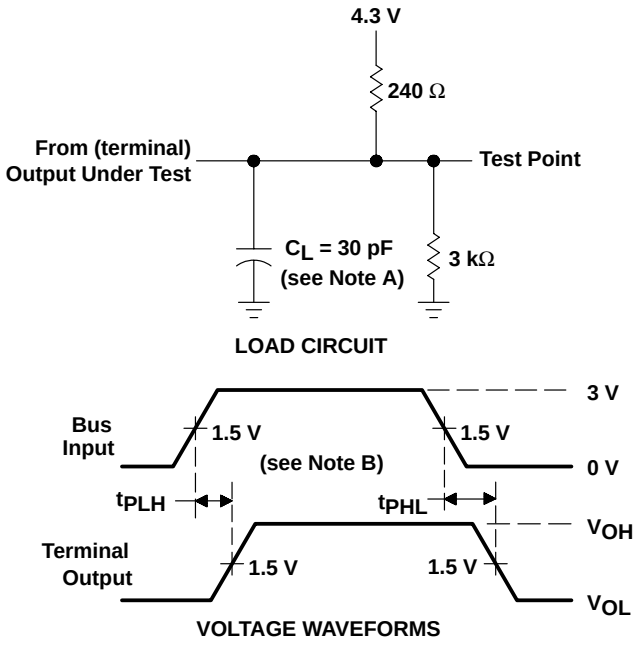
PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	Terminal	Bus	C_L = 30 pF, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high-to-low level output					14	20	
t_{PLH}	Propagation delay time, low-to-high level output	Terminal	Bus (SRQ, NDAC, NRFD)	C_L = 30 pF, See Figure 1		29	35	ns
t_{PLH}	Propagation delay time, low-to-high level output	Bus	Terminal	C_L = 30 pF, See Figure 2		10	20	ns
t_{PHL}	Propagation delay time, high-to-low level output					15	22	
t_{PLH}	Propagation delay time, low-to-high level output	Terminal ATN or Terminal EOI	ATN+EOI	See Figure 3		14		ns
t_{PHL}	Propagation delay time, high-to-low level output	Terminal ATN or Terminal EOI	ATN+EOI	See Figure 3		14		ns
t_{PZH}	Output enable time to high level	TE, DC, or SC	Bus (ATN, EOI, REN, IFC, and DAV)	See Figure 4			60	ns
t_{PHZ}	Output disable time from high level						45	
t_{PZL}	Output enable time to low level						60	
t_{PLZ}	Output disable time from low level						55	
t_{PZH}	Output enable time to high level	TE,DC, or SC	Terminal	See Figure 5			55	ns
t_{PHZ}	Output disable time from high level						50	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						55	

PARAMETER MEASUREMENT INFORMATION



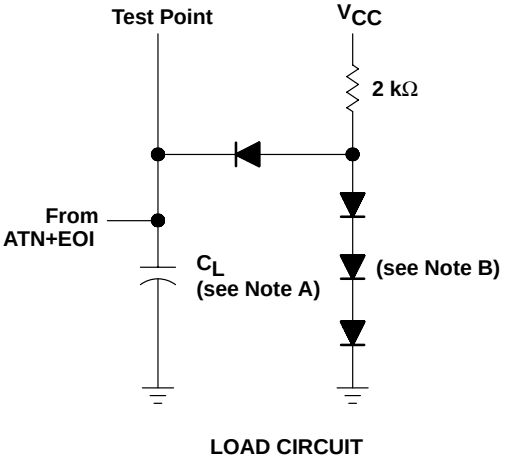
NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ ns, Z_O = 50 Ω.

Figure 1. Terminal-to-Bus Load Circuit and Voltage Waveforms



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ ns, Z_O = 50 Ω.

Figure 2. Bus-to-Terminal Load Circuit and Voltage Waveforms



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.

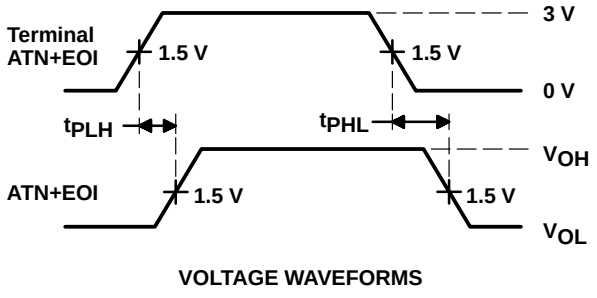
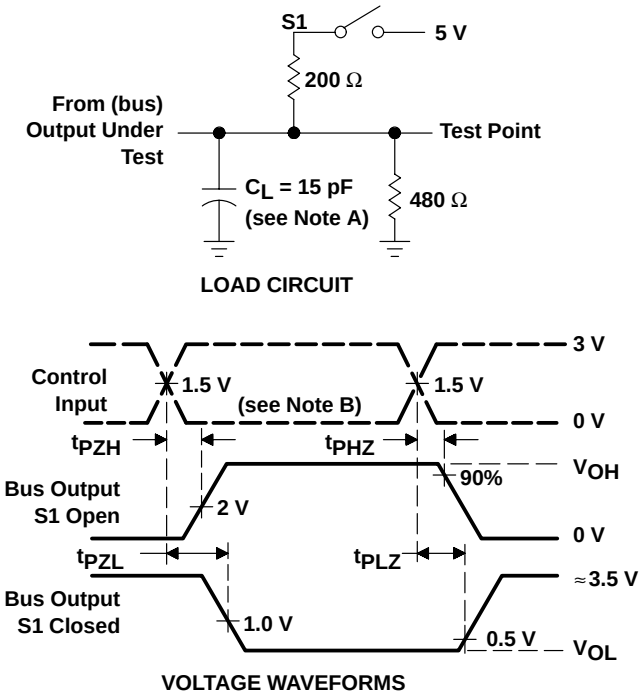


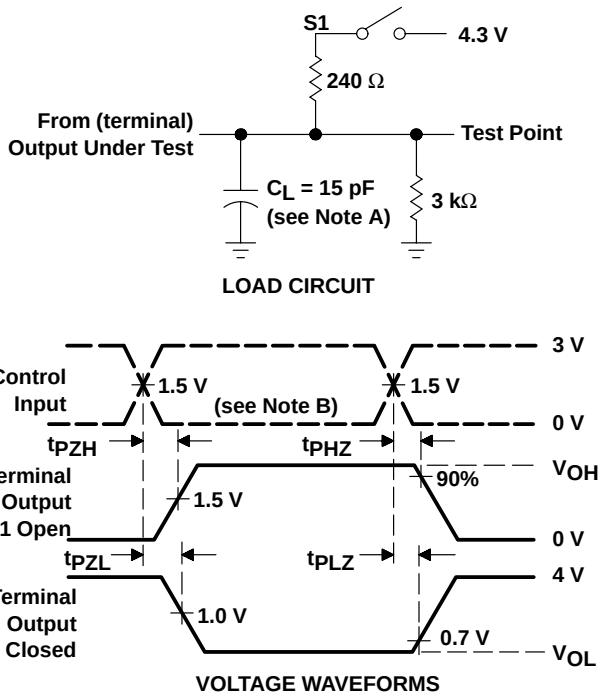
Figure 3. ATN+EOI Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 4. Bus Enable and Disable Times Load Circuit and Voltage Waveforms



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 5. Terminal Enable and Disable Times Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

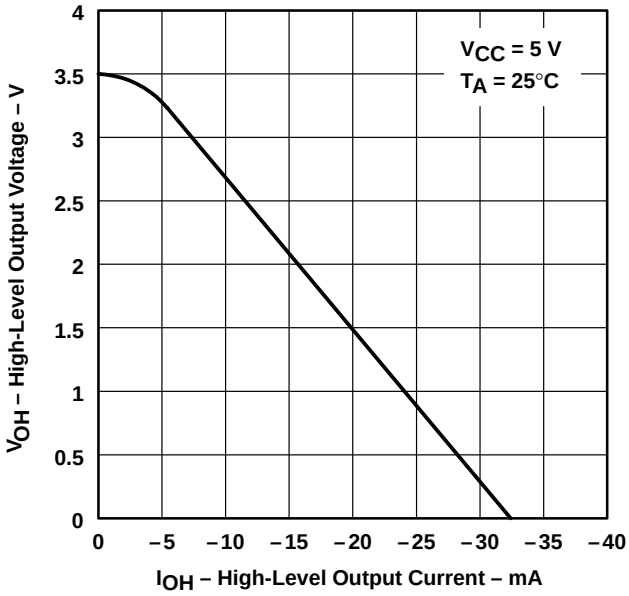


Figure 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

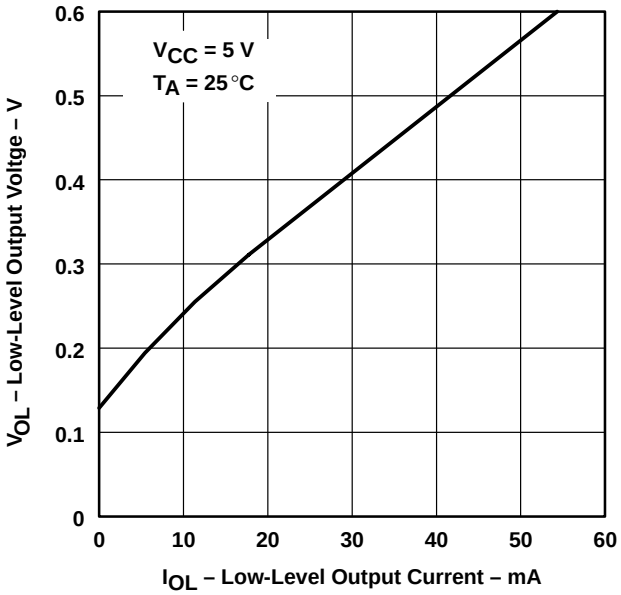


Figure 7

TERMINAL OUTPUT VOLTAGE vs BUS INPUT VOLTAGE

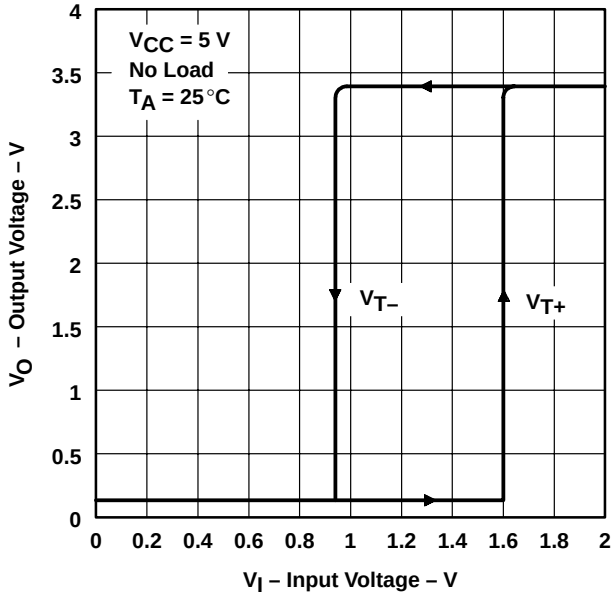


Figure 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

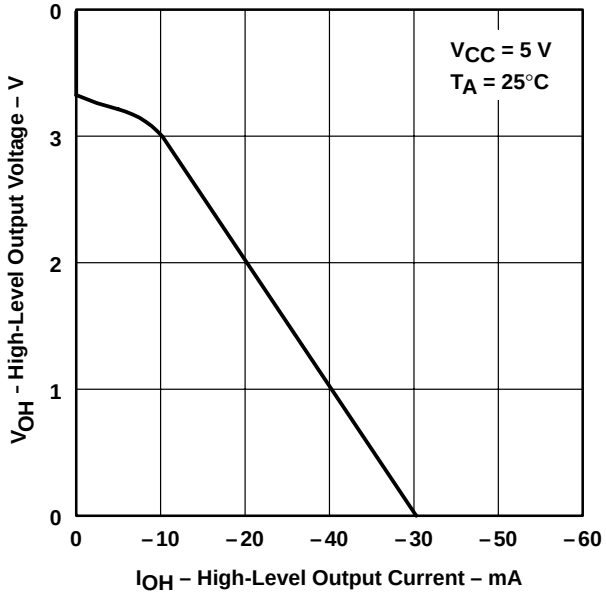


Figure 9

BUS LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

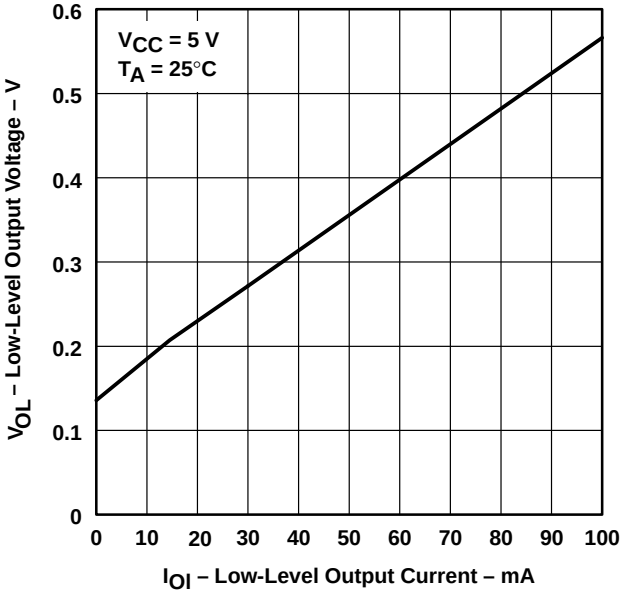


Figure 10

BUS OUTPUT VOLTAGE vs THERMAL INPUT VOLTAGE

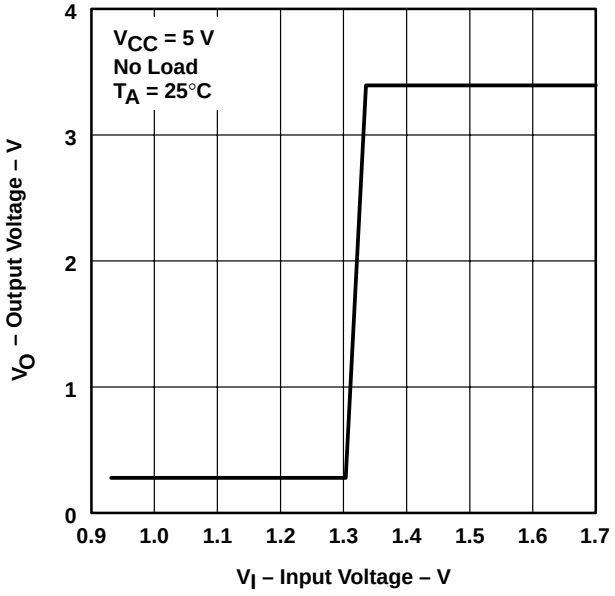


Figure 11

BUS CURRENT vs BUS VOLTAGE

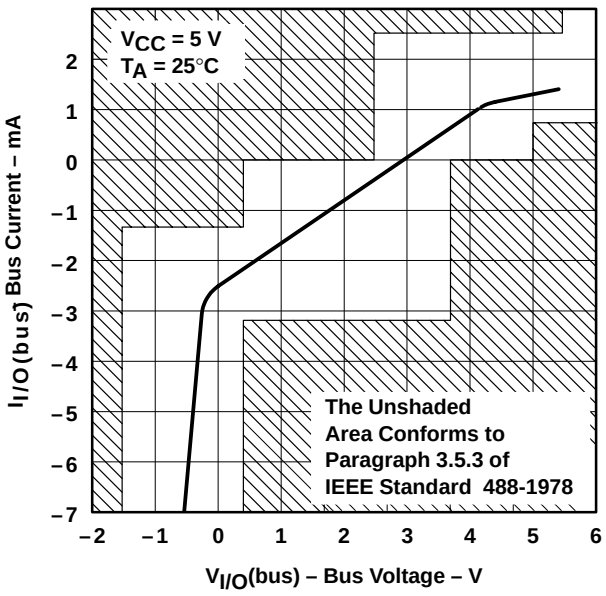


Figure 12

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